# A 600-W Enhancement-Mode GaN Multi-Level Dynamic Converter for Supply Modulated PAs

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***Abstract*— A high power multi-level supply modulator (SM) for phased array applications using E-mode GaN HEMTs is presented. The switching device selection and circuit considerations are discussed, as well as the required electromagnetic (EM) modeling of the output trace to accurately predict the output waveforms. The SM experimentally demonstrates switching up to 10 MHz between four discrete output voltages from 10 V to 20 V, delivering peak powers of 600 W at 92.6% efficiency.**

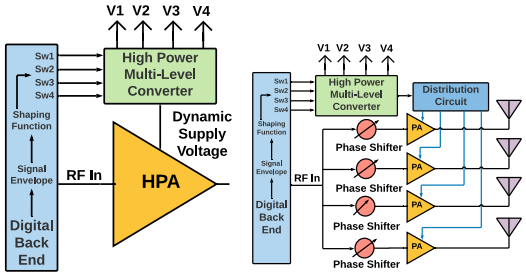
***Keywords*— Phased array, Power amplifier, Supply modulation**

## I. Introduction

RF and microwave systems for communications and electronic warfare need to transmit signals with high peak to average power ratios (PAPRs). Power amplifiers (PAs) are inherently inefficient at lower power levels. A possible efficiency enhancement method is supply modulation, also referred to as envelope tracking (ET), where the supply voltage of a transistor or amplifier dynamically follows the envelope of the input signal [1]. This technique is traditionally used to enhance the back-off efficiency of a PA, but has also been shown to improve gain flatness or linearity [2].

A supply-modulated PA requires a dynamic power supply, which we refer to as a supply modulator (SM). There are two significant challenges related to the SM design for wide bandwidth signals: high slew rate or fast-switching speeds; and simultaneous high efficiency so that the composite power-added-efficiency (CPAE) of the SM and PA is not degraded compared to the efficiency of the PA alone. A multi-level converter (MLC) architecture for the SM can address these challenges [3], [4], [5]. Instead of supplying a continuous range of output voltages, MLCs provide several discrete voltage levels, which track the envelope average. This significantly reduces the required switching speed of the MLC as compared to a continuous SM, thus enabling high bandwidths. Since switching losses scale with frequency, the efficiency of a MLC is higher as compared to a standard buck converter [3], which would need to switch at about 10 times the signal envelope bandwidth for accurate tracking and is usually assisted with an inefficient linear amplifier [1].

There are a number of applications for a high-power SM, including a high-power PA or multiple power-combined PAs, Fig. 1. For example, in a transmit phased array, efficiency at the element level can be improved by adding a SM at each element [6] or simultaneously varying the supply on all array elements




(a) (b)

Fig. 1. Block diagram of (a) a high-power amplifier and (b) a transmit phased array with supply modulation using a high-power dynamic supply modulator. This paper details a High-Power Multi-Level Converter (HPMLC) used as the supply modulator.

using a single high-power multi-level converter (HPMLC). The SM in this paper is designed for 600 W of peak power, which could track as many as 20 10 W PAs with a maximum drain voltage of 20 V at 1.5 A at peak output power. Implementations of high power SMs exceeding 100 W have been demonstrated in [7], [8]. To the best of the authors' knowledge, the work presented here is the first experimental validation of a SM with a peak power of 600 W, and the design, simulations and measurements are presented below.

## II. Multi-Level Converter Architecture

The HPMLC described in this work is a discrete four-level converter, shown in Fig. 2a. Four dc voltages are provided to the HPMLC from an external supply, and one of the four GaN HEMT transistors is turned on at a time to connect this voltage to the output load represented by $R_{\mathrm{L}}$ and $C_{\mathrm{L}}$ through the block labeled "output trace". The geometry of the output trace is studied, and the final design minimizes output inductance and is discussed further in Section III.

Each capacitor bank in Fig 2a is built from components with values, packages, and number of elements per voltage line shown in Table 1. These bypass capacitor help to eliminate the effects of feed cable inductances that connect the external power supplies to the HPMLC board (Fig. 2b). By carefully selecting different packages and capacitance values with low equivalent series resistance (ESR) and low equivalent series inductance (ESL), the impedance magnitude seen by the switch devices presented from the capacitor bank remains below 50 mΩ from 300 Hz to 100 MHz.

The gates of the HEMTS are directly driven by commercially available drivers (Ti UCC21520ADW) which

Table 1. Capacitor, packages, and number of elements in each capacitor bank

| Value | Package | Material | Number |
|---|---|---|---|
| 33 nF | 0805 | C0G | 2 |
| 100 nF | 1210 | C0G | 2 |
| 10 µF | 1210 | X5R | 5 |
| 270 µF | Radial | Electrolytic | 3 |

provide a low output impedance for fast switching transitions and allow for individual gate voltage levels required in this SM topology. The drivers internally provide a capacitive isolator which eliminates the need for an external digital isolator. To turn on the enhancement mode (e-mode) switch devices, a gate source voltage of 5 V is required. The drive voltages are supplied from external instrumentation supplies and fed to the transistors through the gate drivers. The bit pattern generator (BPG) shown in Fig. 2a is a test instrument which outputs a programmable binary waveform that provides precise control over the switching frequency, dead time, and duty cycle of each of the voltage levels.

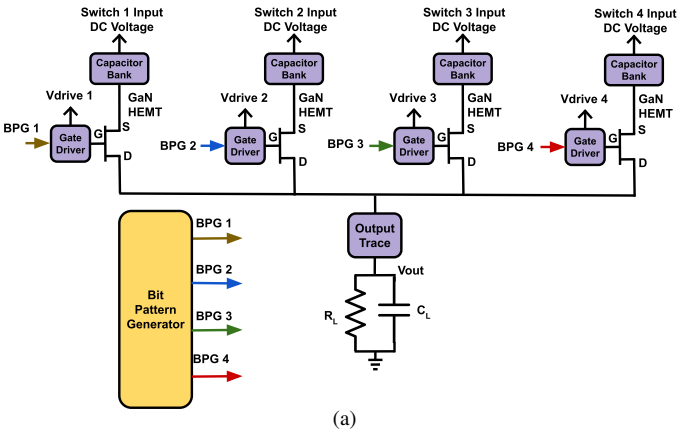
### A. *Device Selection*

Each of the switches shown in Fig. 2a is realized by using two e-mode GaN HEMTs (GaN Systems GS61008T) in parallel, reducing conduction losses. The devices have a breakdown voltage of 100 V and can handle up to 90 A of continuous current. They are chosen due to their low conduction resistance ($R_{\mathrm{on}} = 7\,\mathrm{m\Omega}$), as well as their low input and output capacitances, and fast rise and fall times.

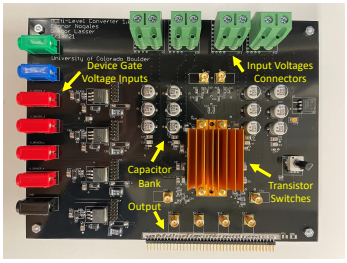
Unlike MOSFETs, GaN HEMTs do not have a parasitic body diode, which is a disadvantage in the MLC architecture. The output load is directly connected to all devices, and whenever any voltage level other than the lowest one is selected, a conduction path to the lower voltage rail would exist through the corresponding body diode. To circumvent this conduction path an external diode can be placed in series with the MOSFET devices. For low-current applications this is acceptable, but for high-current applications the series diodes significantly degrade the efficiency of a HPMLC.

The simulation circuit model capturing internal and external parasitics is shown in Fig. 2c where the capacitance values were obtained with $V_{\mathrm{ds}} = 10\,\mathrm{V}$ and $V_{\mathrm{gs}} = 0\,\mathrm{V}$. Note that the gate-to-source $C_{\mathrm{gs}}$ and gate-to-drain capacitances $C_{\mathrm{gd}}$ differ by a factor of 8.8. In the HPMLC, we therefore flip the HEMTs with the source contacts connected to the fixed input voltages, as shown in Fig. 2a. In regular orientation, the resonator formed by $C_{\mathrm{gs}}$ and the gate extrinsic inductances causes unwanted conduction and shoot-through. Simulations confirm that the flipped operation significantly reduces ringing due to the smaller $C_{\mathrm{gd}}$ capacitance.

For GaN devices, reverse conduction can be avoided by keeping the nominal gate voltage at or below the lowest output voltage. This avoids the use of an external diode and its associated losses. Unfortunately, GaN devices have a limit on the minimum gate to source voltage, which is $V_{\mathrm{gs,min}} = -10\,\mathrm{V}$




(a)

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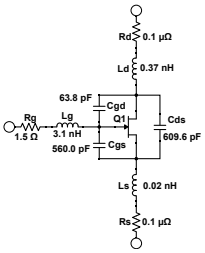



(c)

Fig. 2. Block diagram (a), and photograph (b) of HPMLC; device parasitics of the used e-mode GaN switching transistors (c).

for the devices used here. This enforces a limit on the range of output voltages based on the threshold voltage $V_{\mathrm{th}}$. The range of output voltages is limited to

$$\Delta V_{\mathrm{out}} = V_{\mathrm{out,max}} - V_{\mathrm{out,min}} \leq |V_{\mathrm{gs,min}}| + V_{\mathrm{th}}, \qquad (1)$$

where $V_{\mathrm{out,max}}$ and $V_{\mathrm{out,min}}$ are the maximum and minimum output voltages, repetitively. In this work we limit $\Delta V_{\mathrm{out}}$ to 10 V so the threshold voltage acts as a safety margin.

### B. *Switching Losses and Transistor Efficiency*

The primary sources of loss in the circuit are conduction and switching losses. The latter occur whenever a transistor is switched on or off. First, there are losses when the input and output capacitances are charged and discharged, although the output charge is in some cases recovered. The second hard-switching loss arises from the finite switching time of the devices while current flows through them.

The conduction and switching losses in a single switch transitioning between 20 V and 10 V are simulated in the time domain (LTSpice) and are shown in Fig. 3. The conduction losses are calculated by observing the voltage drop across the device during conduction, taking the self heating effects in the device into account. For the switching losses, the hard-switching loss as well as the energy required to charge the input and output capacitances are added to calculate the total switching loss. It is clear from Fig. 3 that at high frequencies, the switching losses dominate. Fig. 3 also shows the single transistor total efficiency, defined as the input powers provided by the dc supplies divided by the output power delivered to

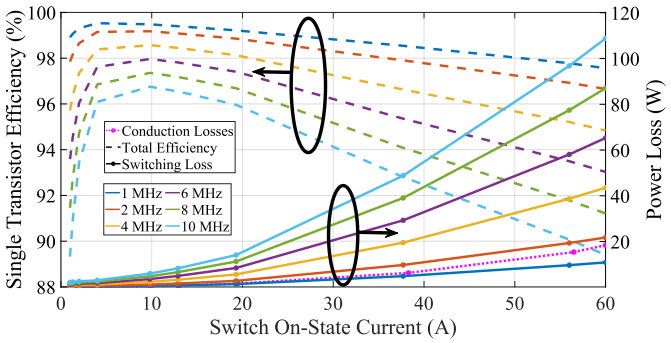
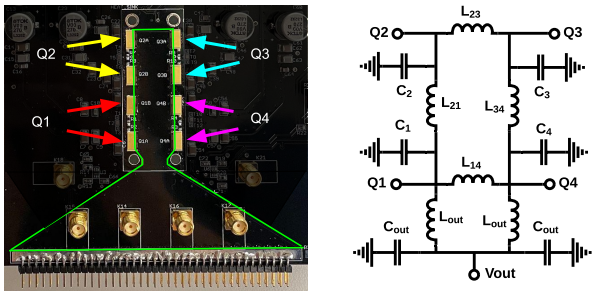



Fig. 3. Conduction and switching losses of a single transistor plotted as a function of device on current.




(a) (b)

Fig. 4. (a) Top view of the output trace. (b) Equivalent LC circuit of the output trace.

the load. For high currents and switching frequencies above 2 MHz, the hard-switching losses dominate and efficiency drops with increased current. For very low currents, the capacitive switching losses independent of the current draw dominate and cause the drop in total efficiency, especially for high switching speeds.

## III. Electromagnetic and Circuit Modeling

Spice models of the GaN devices are provided by the manufacturer and used to simulate the time domain switching waveforms. However, at high switching speeds, the parasitics of the circuit, particularly the output trace in the layout connecting the devices to the load, have a significant effect on ringing and feasible switching speed. The output trace needs to be a low-impedance interconnect over a broad frequency range (0 to 100 MHz), and is designed as a taper to a width of 100 mm. At the output connector, it has a characteristic impedance of approximately 1 Ω which is a compromise between the expected load resistance presented by the PA(s) and the physical width of the trace.

The top view of the output trace is shown in Fig. 4a, implemented on a four-layer printed-circuit board (PCB). The top and bottom layers are made with 2-oz copper and the two inner layers with 1.5-oz copper. The output trace is formed by the two top layers connected together by vias. The bottom two layers, which are connected with vias as well, form the ground plane. The trace was modeled in AWR and simulated with the full-wave AXIUM electromagnetic solver to obtain 5-port

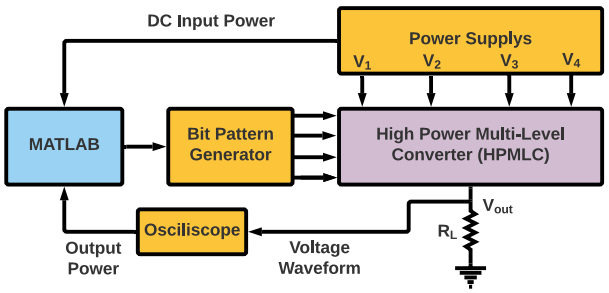



Fig. 5. Block diagram of the test setup used to characterise the HPMLC.

$S$-parameters. In addition to the output port, every switch location forms another port. An equivalent LC network shown in Fig. 4b is fitted to the $S$-parameters and used for subsequent LTSpice simulations. The effects in the output trace can be observed when comparing Fig. 6a that shows the simulated output voltage for a load of 0.67 Ω and uses the LC network model, and Fig. 6b where the same load is directly connected to the switching transistors without the LC network model.

## IV. Test Setup

The HPMLC was tested by switching between four voltage levels with equal duty cycle and a fixed dead-time using the bit pattern generator in the measurement setup shown in Fig. 5. The voltage levels were 20 V, 16.6 V, 13.3 V, and 10 V in that order. In this work we use the same continuously repeated 4-level waveform for simulations and measurements, since it contains both up and down switching transitions and the ringing on rising and falling edges is not the same. The switching period $T_{\mathrm{sw}}$ is defined as the pulse width of one of the voltage levels and the total waveform period $T$ is four times the switching period. The switching frequency is defined as $f_{\mathrm{sw}} = 1/T_{\mathrm{sw}}$. The output voltage is observed with an oscilloscope and used to compute the average output power over one period $T$

$$P_{\mathrm{out}} = \frac{1}{T}\int_0^T \frac{v_{\mathrm{out}}(t)^2}{R_{\mathrm{L}}}dt, \tag{2}$$

where $R_{\mathrm{L}}$ is the load resistance that is constructed on a separate PCB and connected to the HPMLC through the wide output connector (see Fig. 4a). The total efficiency of the HPMLC is computed by dividing $P_{\mathrm{out}}$ by the total dc input power from all supplies, including the power consumption from gate drivers, and digital circuitry on the board.

## V. Measurement Results

Fig. 6c shows the measured output voltage waveform for a switching frequency of $f_{\mathrm{sw}} = 4$ MHz and a load of $R_{\mathrm{L}} = 0.67\,\Omega$. While the measured ringing amplitude is slightly larger than predicted in simulations (Fig. 6a), the ringing frequency is predicted well, especially when compared to the simulation without modelling the output trace (Fig. 6b). The ringing improves with reduced load resistances, i.e. higher power levels. With a $R_{\mathrm{L}} = 0.67\,\Omega$ load the HPMLC is limited to a switching frequency of about 5 MHz since for higher

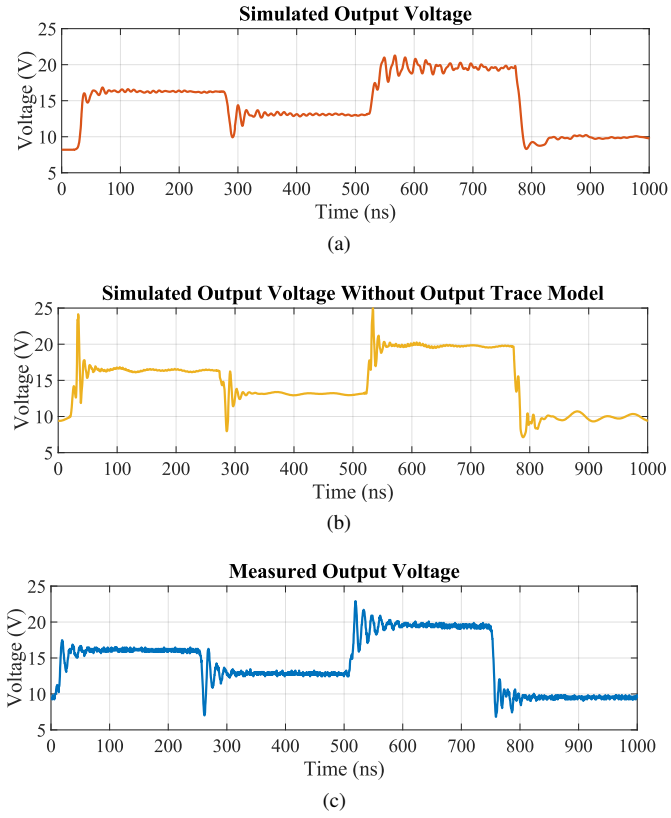



Fig. 6. Output voltage $V_{\mathrm{out}}$ waveforms with a load $R_{\mathrm{L}} = 0.67\,\Omega$ corresponding to 325 W average output power for $f_{\mathrm{sw}} = 4\,\mathrm{MHz}$. Simulation with output trace modelled as in Fig. 4b (a), Simulation neglecting output trace (b), measurement (c).

speeds the ringing occupies a significant part of the pulse. The use of snubber networks and special low inductance loads for testing will be investigated in the future.

The efficiency was measured at different switching frequencies as a function of the average output power as shown in Fig. 7. The measured efficiency is greater than 77.4% across all measured output powers and frequencies and greater than 89.4% for frequencies below 6 MHz. Due to limits of the available power supplies, measurements were only taken up to an average output power of 325 W. This corresponds to a load of $0.67\,\Omega$ and a peak instantaneous output power of 600 W.

At very low output powers the capacitive losses start to dominate, as discussed in Section II-B. At these power levels we also observe another effect due to the chosen circuit topology. The lowest 10 V supply rail is also used as the gate driver low voltage supply. Whenever a gate is turned off, the gate capacitance is discharged into that supply. This has the effect of recycling that energy and boosts the efficiency of the HPMLC. This effect is easily observed at high switching frequencies where the supply current in the 10 V goes to zero, being entirely powered by the recycled gate charge.

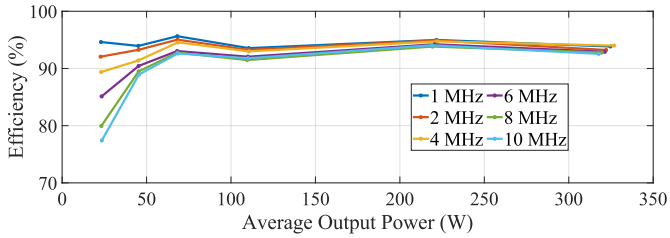



Fig. 7. Total measured efficiency of the HPMLC for different switching frequencies, using the same 4-level test signal switching from 10 V to 20 V as described in Section V. The load $R_{\mathrm{L}}$ is varied from $10\,\Omega$ to $R_{\mathrm{L}} = 0.67\,\Omega$ to achieve different output powers.

## VI. Conclusion

This paper presents a high-power, 4-level converter based on packaged e-mode GaN switches intended as a supply modulator for one or more RF power amplifiers and delivering 1 kW of peak power. Simulations of the total converter efficiency reveal the dominance of switching loss for switching frequencies exceeding 2 MHz. An $LC$ model found from EM simulations of the output trace geometry is used to predict the measured ringing after switching transitions. The HPMLC experimentally demonstrates operation at 10 MHz switching speed and 325 W of output power with an efficiency of 92.6%, which is to the authors' best knowledge the highest output power of a supply modulator reported to date.

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