Efficient X-Band Transmitter With Integrated GaN Power Amplifier and Supply Modulator

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***Abstract*— In this paper, we present a high-efficiency transmitter based on an integrated circuit (IC) supply modulator implemented in the same 0.15-μm gallium nitride (GaN)-on-SiC RF process as the power amplifier (PA) monolithic microwave IC. The X-band 10-W two-stage PA is designed for stable operation with minimal drain capacitance, which enables fast supply modulation. The multilevel supply modulator provides eight voltage levels with 3-bit digital control [(power digital-to-analog converter (pDAC)], achieving a state-of-the-art slew rate of 5 kV/μs. Characterization of the dynamic R_{ON} of the GaN switches allows the development of an efficiency model for the pDAC and an investigation of the effects of the pDAC internal resistance on the PA performance, resulting in a comprehensive efficiency model for the supply-modulated PA. The flexible compact transmitter consisting of the PA and pDAC ICs shows high efficiency in back-off for a variety of signals, both for radar and communications. Measured results for amplitude- and frequency-modulated radar pulses show a composite power-added efficiency (CPAE) of 44% with a peak power of 10 W at 9.57 GHz, with simultaneous spectral confinement and 52-dB improvement of the first time sidelobe. For a 20-MHz high peak-to-average ratio LTE signal, the CPAE increases from 11% to 32% compared to a fixed supply voltage transmitter, while linearity under dynamic supply operation is maintained through digital predistortion.**

***Index Terms*— Envelope tracking (ET), gallium nitride (GaN), microwave monolithic integrated circuit (MMIC), power digital-to-analog converter (pDAC), supply modulation (SM).**

I. Introduction

THE CHALLENGE of efficient amplification of high peak-to-average power ratio (PAPR) signals at microwave carrier frequencies has been addressed with a number of transmitter architectures, such as Doherty, outphasing, and envelope tracking (ET) [1]–[11]. In ET, Fig. 1, the average efficiency of the power amplifier (PA) is increased by keeping the transistors saturated through a dynamic supply, which is synchronized with the signal envelope through a shaping function. ET alone can be applied to Doherty [10], [12], Chireix outphasing [9], [13], and load-modulated balanced amplifiers [11], [14] for further efficiency enhancements.

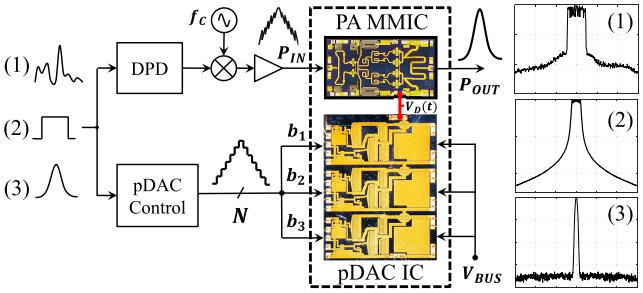

Fig. 1. Conceptual block diagram of the transmitter based on PA and supply modulator chips implemented in the same microwave 0.15-μm GaN process. This architecture allows efficient amplification of a variety of signals, either for (1) communications or (2) and (3) radars.

In envelope-tracking transmitters employing wideband signals, the required slew rate, tracking accuracy, and high efficiency become challenges for the dynamic supply. Several approaches to solving this problem are demonstrated for signals with tens of megahertz bandwidth: linearly assisted switching converters [4], [5], multiphase switching converters [15], and discrete-level supply modulators [7], [8], [16]. The high power density, high mobility, high breakdown voltage, and high-temperature operation make gallium nitride (GaN) technology attractive not only for RF PAs but also for supply modulators. Single [17], [18] and multiphase [15] high-frequency buck converters, using RF GaN processes, demonstrate efficiencies >90% at switching frequencies up to 400 MHz with 10-W power delivered to a resistive load. The main challenges are associated with the drive circuitry for noncomplementary devices [18], as well as the required off-chip filtering of the pulsewidth modulation (PWM) switching harmonics. Furthermore, the PA presents a dynamic nonlinear load, as discussed in detail in [19] and [20]. The values of the *LC* filtering components are reduced for multilevel supplies [7], [8], [16], making direct integration with PAs feasible. The multilevel solution with adaptive voltage commutation does not require the typical 10× ratio between switching rate and signal bandwidth required by PWM converters, thus switching losses are minimized for wideband signal tracking [7]–[11].

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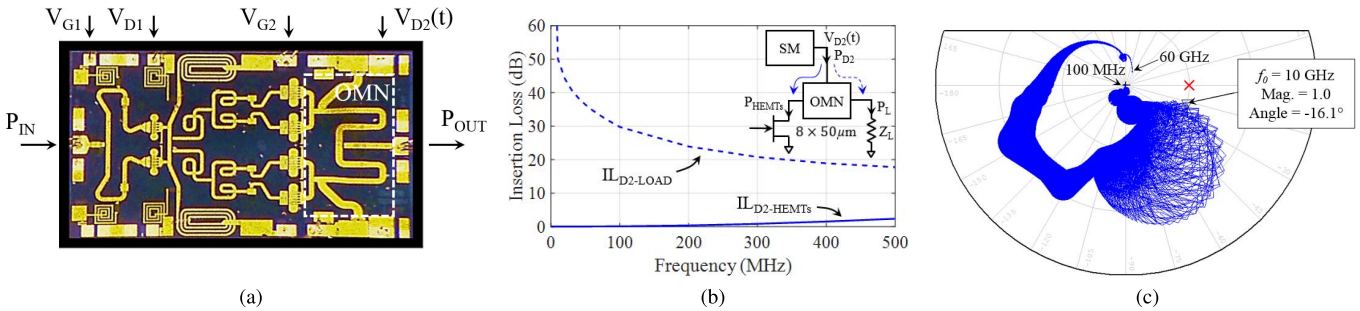


Fig. 2. (a) Photograph of the two-stage 10-W X-band GaN MMIC PA with the OMN of the second stage designed for fast SM. (b) Simulated insertion loss of the two paths of the OMN including supply and dc block capacitors. (c) Loop gain stability analysis from 100 MHz to 60 GHz over a range of HEMT parameters dictated by the fabrication process. The PA is stable with 16° phase margin for all complex passive output loads and supply line impedances in large-signal operation with swept input power.

This paper demonstrates the use of a high-performance Qorvo 0.15-μm GaN-on-SiC process to implement a microwave monolithic integrated circuit (MMIC) supply-modulated PA for a 10-W efficient and compact X-band transmitter. Its conceptual block diagram is shown in Fig. 1. Here, the two ICs are connected through a low-inductance board trace to enable fast supply modulation (SM) but allowing also separate characterization of both chips. One of the contributions of this paper is the codesign aspect of the transmitter, where a detailed efficiency model is presented for the supply-modulated PA. The individual static and dynamic contributions of the two chips are extensively characterized and used for predicting composite efficiency with modulated signals.

This paper is organized as follows. Section II describes the PA design specifically for ET, as well as the design of the eight-level supply modulator, referred as power-digital-to-analog converter (pDAC). Section III introduces a loss model for the pDAC along with a discussion of the limitations of a microwave GaN process for switching circuit implementations. This section also presents packaging and characterization results of the pDAC. Section IV covers the linearization and efficiency characterization of the entire transmitter, addressing the digital baseband portion, and additionally provides a comparison with a hybrid pDAC implemented with GaN-on-Si switching devices. Finally, experimental results with radar and communications signals are given in Section V.

II. X-Band GaN Transmitter Design

In this section, we provide the relevant design details of the two GaN chips, the PA and pDAC, both fabricated in the Qorvo 0.15-μm GaN-on-SiC process. Independent characterization of the two ICs is shown, but since the technology process is the same, this leads naturally to the possibility of a single-die supply-modulated PA.

A. GaN MMIC PA for Supply Modulation

The photograph of the two-stage GaN MMIC PA designed for SM is shown in Fig. 2(a). This MMIC was characterized in terms of trapping-related nonlinearities in [21], which enables us to perform a more accurate PA linearization, shown later in Section V. Here, we discuss the specific design approach

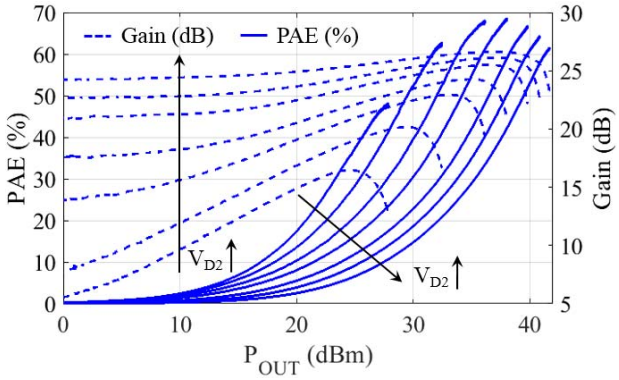


Fig. 3. Measured pulsed (10% duty cycle and 100-μs period) gain and PAE as a function of output power for seven discrete supply voltages from 3.2 to 20 V.

that allows wideband SM of the PA. For an RF output power exceeding 10 W and a saturated gain above 20 dB at 10 GHz, the first stage of the PA is realized with two 8 μm × 50 μm high-electron mobility transistors (HEMTs) and the second stage combines four 8 μm × 50 μm devices [22]. Load–pull simulations with the nonlinear models of the foundry suggest a deep class-AB bias point for the PA with a nominal drain supply of 20 V for both stages, and with quiescent currents of 55 mA for the first stage and 270 mA for the second stage.

To maintain efficiency for broadband, high PAPR signals, SM of the second stage is performed and this imposes special requirements on the dc block, output matching network (OMN), and drain bias line. Fig. 2(b) shows the simulated insertion loss up to 500 MHz from the supply pad to the HEMT drain ($IL_{D2\text{-}HEMTs}$) and from the supply pad to the load ($IL_{D2\text{-}LOAD}$). For broadband signal tracking, the total equivalent capacitance seen at the drain supply node in the output network cannot be too large because it will low-pass filter the dynamically varying envelope. This capacitance consists of the drain bypass, dc block, and equivalent capacitance of the OMN. These capacitances are minimized in the design so that the total drain capacitance in the output circuit is 36.4 pF. The bias line is designed to provide the broadband envelope power $P_{D2}(t)$ with low attenuation to the four transistors of the last stage, whereas low envelope power $P_{D2}(t)$ leaks to the load as a results of the small dc block capacitor.

While reducing the total drain capacitance in the bias network is desirable from a SM standpoint, stability issues may arise since it is not possible to utilize large on- and off-chip capacitors. In this design, the MMIC PA is designed to be stable with minimal on-chip drain capacitance and no external components when operating in large signal over a range of input power levels and supply voltages. The stability analysis shown in Fig. 2(c) shows loop gain simulations for varying loads and supply impedances from 100 MHz to 60 GHz. At 10 GHz, the PA presents 16.1° phase margin for all complex passive output loads and all complex drain supply line impedances. According to the foundry process guidelines, the device g_m, $C_{\rm GS}$, and $C_{\rm GD}$ were varied to reach the −40 °C values, by +30%, −30%, and +30%, respectively.

Fig. 3 shows the measured large-signal gain and power-added efficiency (PAE) for seven fixed supply voltages obtained with a low-resistance pulsed voltage supply, which also confirm stable operation of the PA with minimal drain capacitance. We note that the PA is designed to maximize PAE at 6-dB output power backoff when the supply voltage is within 12–15 V. The PA demonstrates 23.2-dB saturated gain with 41.7-dBm output power. At the maximum output power, the peak PAE is about 61.3% while it drops at 31.6% at 6-dB output power backoff. If SM of this PA is employed, the PAE improves almost 35.3 percentage points reaching 66.9%.

B. Integrated GaN Power-DAC Supply Modulator

The topology of the multilevel supply modulator is illustrated in Fig. 4(a). Three cascaded half-bridges are stacked and each half-bridge is composed of two power switches. The ith half-bridge is supplied by an isolated voltage, $V_{{\rm DD}i}$, with respect to a floating ground, GND_i. The half-bridge is controlled by a bit, b_i, and by its complement, $\bar{b_i}$, which are directly generated in digital baseband. During the commutation of the half-bridge, a deadtime (when both power switches are off) is introduced to avoid a short-circuit between $V_{{\rm DD}i}$ and GND_i, with the associated efficiency loss. During the deadtime, the low-side free-wheeling diode maintains the current flow to the load. When the high-side switch of the half-bridge is turned on, the voltage $V_{{\rm DD}i}$ is connected in series to the floating ground of the subsequent cell. When the low-side switch of the half-bridge is on and after the deadtime, the output of the half-bridge is zero. Therefore, the circuit resembles the operation of a DAC

$$V_{O,{\rm SM}} = \sum_{i=1}^{3} b_i V_{{\rm DD}i} \tag{1}$$

in which the output level is controlled by b_i. If the three isolated supply voltages are selected with a binary ratio of a given reference voltage V_R (e.g., $V_R/2$, $V_R/4$ and $V_R/8$), it is possible to synthesize a discrete waveform with eight voltage levels from only three input voltage supplies. Therefore, all the levels are uniformly distributed between zero and $V_{O,{\rm SM,MAX}} = 7V_R/8$, and the circuit resembles the functionality of a DAC, so we refer to it as a power-DAC (pDAC). This approach enables to improve the ideally continuous output voltage from an N-level resolution to 2^N levels by using a purely switching circuit.

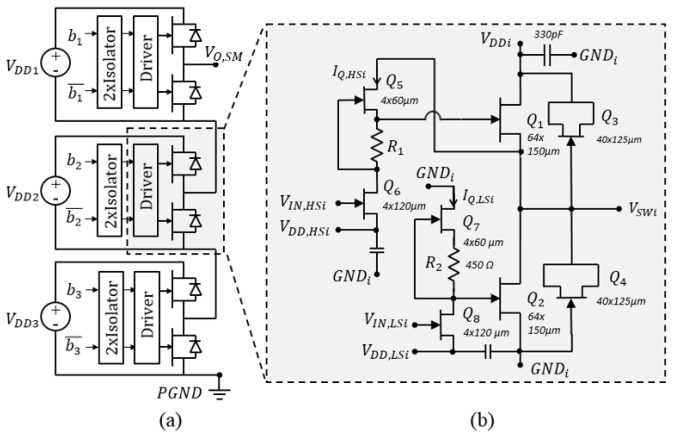


Fig. 4. (a) Multilevel topology of the pDAC. Three cascaded half-bridges are supplied by three isolated voltage sources $V_{{\rm DD}i}$ allowing the generation of eight voltage levels. (b) Schematic of the pDAC half-bridge with integrated driver.

TABLE I
pDAC HALF-BRIDGE OPERATION

b_i	$\bar{b_i}$	Q_8	Q_6	$I_{Q,LS}$	$I_{Q,HS}$	Q_2	Q_1	V_{SWi}
0	1	OFF	ON	0	8 mA	ON	OFF	0 V
1	0	ON	OFF	5 mA	0	OFF	ON	V_{DDi}

A hybrid pDAC using low-frequency GaN-on-Si switches and capable of tracking a 10-MHz LTE signal at L-band is demonstrated in [7]. Here, the same topology is implemented in a single chip with a 0.15-μm GaN-on-SiC process. This IC is briefly discussed in [13] in purely static operation. In the remainder of this section, the details on the design and characterization are given. The same Qorvo microwave 0.15-μm GaN process as that used for the PA is used, although this GaN-on-SiC process provides only n-type depletion-mode (normally *on*) HEMTs. The threshold voltage is −3.5 V and the device is on for $V_{\rm GS} = 0$ V and off for $V_{\rm GS} = -5$ V; the breakdown voltage exceeds 50 V [22]. The drivers are integrated with the power switches for compactness. In addition, integration minimizes gate-loop parasitics and enhances switching speed while reducing the risk of spurious retriggering at high switching frequencies [18]. With only n-type transistors, it is not possible to implement a fully complementary driver that does not dissipate dc power. A resistor can be employed as a simple pullup device, but this choice will introduce a stringent tradeoff between switching speed and efficiency [17]. In [18], an improved solution is demonstrated for the pullup network of the driver, referred to as *modified active pullup*. The integrated GaN pDAC adopts this solution, although it is still inferior to complementary transistor drivers that have almost no static power consumption [7].

Fig. 4(b) shows a single half-bridge with integrated driver. The pDAC control bits, b_i and $\bar{b_i}$, are generated in the digital baseband and are fed to the inputs of six high-speed digital isolators (Texas Instruments ISO721M). The supply voltage on the digital side is 3.3 V while the output side of the

isolators is fed with 5 V. The isolator outputs are connected to the high- and low-side driver input signals, $V_{\mathrm{IN,HS}i}$ and $V_{\mathrm{IN,LS}i}$. $V_{\mathrm{IN,HS}i}$ is switched by the isolators between -8 and -13 V, while $V_{\mathrm{IN,LS}i}$ commutates between -5 and -8 V. As shown in Fig. 4(b), the source terminals of the input transistors, Q_6 and Q_8, are biased with $V_{\mathrm{DD,HS}i} = -8$ V and $V_{\mathrm{DD,LS}i} = -5$ V, respectively, and this enables the isolator to turn the input transistors on and off.

The operation of a single half-bridge is summarized in Table I. When b_i ($\hat{b_i}$) is low, the driver pulldown Q_8 (Q_6) is off, while Q_7 (Q_5) is on, and the corresponding power switch Q_2 (Q_1) is on, since its $V_{\mathrm{GS}} = 0$ V. On the other hand, when b_i ($\hat{b_i}$) is high, both Q_8 and Q_7 (Q_6 and Q_5) are on, and Q_2 (Q_1) is off. In the latter case, the driver is dissipating static power since a current path is created through Q_7 and Q_8 (Q_5 and Q_6) [18]. Commutations of the power switches Q_1 and Q_2 are sped up by higher $I_{Q,\mathrm{HS}}$ ($I_{Q,\mathrm{LS}}$), at the expense of higher static losses in the driver. Thus, the sizes of the transistors and the resistors R_1 and R_2 of this modified active pullup network are chosen as a compromise between static loss and switching speed, resulting in the values given in Table I.

The high-frequency 0.15-μm GaN-on-SiC process is not optimized for low ON-resistances ($R_{\mathrm{ON}} = 2.1$ Ω/mm) [18], and conduction losses are minimized by selecting very large peripheries (64 $\times$ 150 μm) for the power switches, Q_1 and Q_2. A nonlinear HEMT model results in a simulated $R_{\mathrm{ON}} = 0.22$ Ω, but we expect a higher value in practice since it has been demonstrated that temperature and trapping effects deteriorate the dynamic ON-resistance [23]–[25].

The free-wheeling diodes, Q_3 and Q_4, in parallel with the power switches, are implemented by shorting the drain and source of an HEMT so that the gate is the anode and the drain–source is the cathode (see Fig. 4). The voltage drop across the conducting diode is about 1 V and the diode is dimensioned to carry a maximum average current of 40 mA, resulting in a 40 μm $\times$125 μm periphery. The IC is designed using Keysights ADS and Modelithics' nonlinear models, while the circuit layout is performed in National Instruments Microwave Office. The die size is 5.4 $\times$ 3.8 mm^2 and it is wire-bonded to a 48-pin 7 $\times$ 7 mm^2 QFN package with a transparent lid, shown in the photograph in Fig. 5, and mounted on a four-layer FR4 board. Thermal vias are placed directly underneath the package to provide heat spreading through the board metal layers. Since the isolator size is the same, but the driver switches are integrated on-chip, the pDAC IC is about 10 times smaller in area compared to the hybrid version of this circuit (5.5 $\times$ 28 mm^2) [7]. All required bias voltages are derived from a single 48-V supply.

III. Integrated pDAC Efficiency Model

In order to quantify the composite PAE of the supply-modulated transmitter, a loss budget model of the pDAC IC is next determined, accounting for conduction, switching, and driver losses. The model is validated first statically with a resistive load, and then with the PA MMIC as the load. We define the efficiency, η_{SM}, as

$$\eta_{\mathrm{SM}} = \frac{P_{O,\mathrm{SM}}}{P_{O,\mathrm{SM}} + P_{\mathrm{DISS}}} \tag{2}$$

where $P_{O,\mathrm{SM}}$ and P_{DISS} are the output and the dissipated powers of the supply modulator, respectively. Referring to Fig. 6(a), the output power $P_{O,\mathrm{SM}}$ can be calculated as a series of ideal voltage sources with the ON-resistance of the switches as shown in Fig. 6(b). The final equivalent circuit of the pDAC is shown in Fig. 6(c), resulting in the output voltage

$$V_{O,\mathrm{SM}} = \frac{R_L\,(b_1 V_{\mathrm{DD1}} + b_2 V_{\mathrm{DD2}} + b_3 V_{\mathrm{DD3}})}{R_L + 3R_{\mathrm{ON}}} \tag{3}$$

where R_L is the equivalent load resistance (i.e., drain terminal of the PA in static condition). The corresponding static output power $P_{O,\mathrm{SM}} = {V_{O,\mathrm{SM}}}^2/R_L$ can be calculated as

$$P_{O,\mathrm{SM}} = \frac{R_L\,(b_1 V_{\mathrm{DD1}} + b_2 V_{\mathrm{DD2}} + b_3 V_{\mathrm{DD3}})^2}{(R_L + 3R_{\mathrm{ON}})^2}. \tag{4}$$

The total dissipated power, P_{DISS}, can be expressed as the sum of conduction, driver, and switching losses [26]

$$P_{\mathrm{DISS}} = P_{\mathrm{COND}} + P_{\mathrm{DRV}} + P_{\mathrm{SW}}. \tag{5}$$

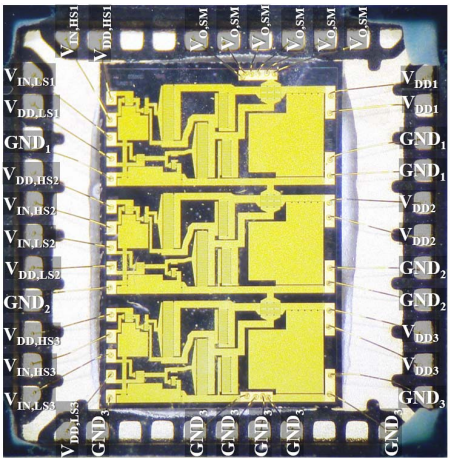


Fig. 5. Photograph of the pDAC GaN-on-SiC MMIC. The pDAC chip size is 5.4 $\times$ 3.8 mm and is wire-bonded to a 48-pin 7 mm $\times$ 7 mm QFN package with a transparent lid.

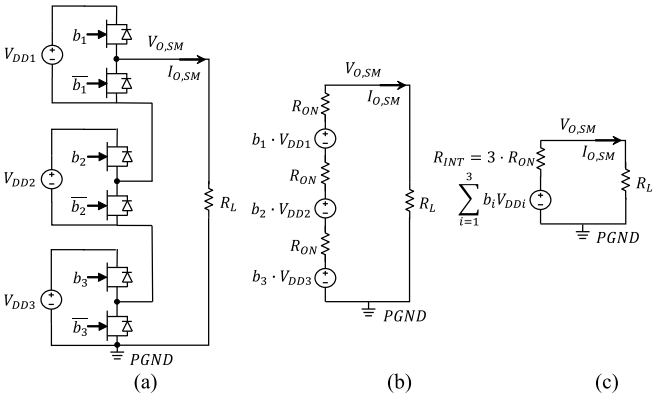


Fig. 6. (a) pDAC topology. (b) Static pDAC equivalent circuit with controlled voltage sources and switch resistances. (c) Equivalent circuit of the pDAC with resistance R_{INT} that models the total loss.

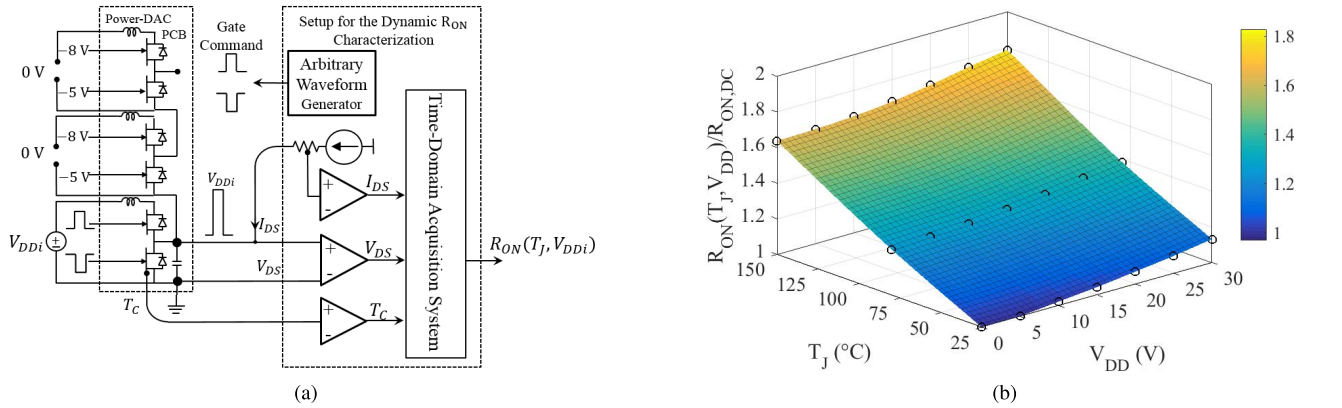


Fig. 7. (a) Setup used for the characterization of the dynamic $R_{\rm ON}$ of the power switches in the pDAC [24]. (b) Characterization results (black circles) of the dynamic $R_{\rm ON}$ in the pDAC; the maximum degradation (+80% increase on the $R_{\rm ON,dc} = 0.33\ \Omega$ at 25 °C) is observed at the maximum junction temperature (150 °C) and maximum voltage stress (30 V).

To estimate the conduction losses, we consider that all six power switches have the same periphery (9.6 mm) with the same nominal $R_{\rm ON}$. Since the half-bridges are connected in series, the current flowing through the load, $I_{O,\rm SM}$, is constant and independent on the control bit configuration [see Fig. 6(a)]. Therefore, the total internal resistance $R_{\rm INT}$ of the supply modulator is $3R_{\rm ON}$, as shown in Fig. 6(c), and the conduction losses become

$$P_{\rm COND} = R_{\rm INT} {I_{O,\rm SM}}^2 = 3R_{\rm ON} {I_{O,\rm SM}}^2 \tag{6}$$

where $I_{O,\rm SM}$ is the rms value of the current. The dc ON-resistance of the power switches at room temperature (25 °C) is measured with a multimeter to be $R_{\rm ON,dc} = 0.33\ \Omega$, in a good agreement with the simulations (0.22 Ω) when the approximately 75-mΩ resistance of the 1.5-mm-long 25-μm-diameter gold bond wires is taken into account. The GaN transistor resistance increases with junction temperature T_J and increases with the OFF-state drain–source voltage stress, $V_{\rm OFF}$ [23]–[25]. This voltage sensitivity is often associated with charge trapping, which increases the ON-resistance, and it follows [24]:

$$R_{\rm ON} = R_{\rm ON}(T_J, V_{\rm OFF}). \tag{7}$$

In [24], a test bench for measuring dynamic $R_{\rm ON}$ for several GaN technologies, including the Qorvo 0.15-μm GaN-on-SiC process, is presented. This test bench is used to characterize the dynamic $R_{\rm ON}$ directly within the final-circuit PCB of the pDAC with the connection shown in Fig. 7(a). This measurement includes additionally the bond-wire resistance and package pin resistance. Given that the three half-bridges are nominally identical and mounted in the same way, only the bottom half-bridge is considered. The measured dynamic $R_{\rm ON}$ is plotted in Fig. 7(b), where $R_{\rm ON}(T_J, V_{\rm DD})$ is normalized to the dc value and an interpolation surface is shown to highlight the dependence on each variables.

Once the dynamic $R_{\rm ON}$ of a power switch is characterized, we note that in this multilevel topology, both the high-side and low-side switches are alternatively on and off, and therefore, they are subject to the same $V_{{\rm DD}i}$ voltage stress (see Fig. 4), causing a similar trap-induced degradation of their ON-resistances. If we also consider that the supply voltages of the three half-bridges are $V_{\rm DD1} = 3.2$ V, $V_{\rm DD2} = 5.6$ V, and $V_{\rm DD3} = 11.2$ V, the dynamic $R_{\rm ON}$ values increase by +1.1%, +2.8%, and +3.8%, respectively. This results in a nonnegligible +7.7% increase of the total dc ON-resistance, $R_{\rm INT,dc} = 3\ R_{\rm ON,dc} \simeq 1\ \Omega$. Given the high thermal conductivity of the SiC substrate, a uniform temperature distribution assumption results in $T_{J,{\rm HS}i} \simeq T_{J,{\rm LS}i} \approx T_{J,\rm EQ}$. The switch ON-resistance model of (7) can be rewritten as

$$R_{\rm ON} \approx R_{\rm ON}(T_{J,\rm EQ}, V_{{\rm DD}i}). \tag{8}$$

The second contribution to the total dissipated power of (5) is static losses in the half-bridge drivers, $P_{\rm DRV}$, especially since the lack of complementary (p-type) transistors leads to a driver design that is suboptimal. The dissipated power by the drivers can be calculated as [18]

$$P_{\rm DRV} = \sum_{i=1}^{3} (-V_{{\rm DD},HSi} I_{Q,\rm HS} \bar{b_i} - V_{{\rm DD},LSi} I_{Q,\rm LS} b_i) \tag{9}$$

where $V_{{\rm DD},HSi} = -8$ V and $V_{{\rm DD},LSi} = -5$ V. The measured quiescent current of the driver is $I_{Q,\rm HS} = 8$ mA for the high side and $I_{Q,\rm LS} = 5$ mA for the low-side active pullup, as expected from simulations. The static driver dissipation can be calculated from (9) and ranges from 75 mW when all the control bits are "1" to 192 mW when all the bits are "0."

The third contribution to the total dissipated power of (5) is the switching losses, which are mainly due to switch capacitances and the free-wheeling diodes. Capacitive losses are due to the charge and discharge of $C_{\rm GS}$ and $C_{\rm DS}$ capacitors in the low- and high-side switches [18]

$$P_{{\rm SW},C} = \sum_{i=1}^{3} \frac{1}{2} (2C_{\rm DS} {V_{{\rm DD}i}}^2 + 2C_{\rm GS} {V_{\rm GS}}^2) \langle f_{b_i} \rangle. \tag{10}$$

Diode losses are only present in the low-side diode and are due to the overlap of the output current and the diode forward voltage. On average, we have

$$P_{{\rm SW},D} = \sum_{i=1}^{3} (t_{DT} V_F I_{O,\rm SM}) \langle f_{b_i} \rangle. \tag{11}$$

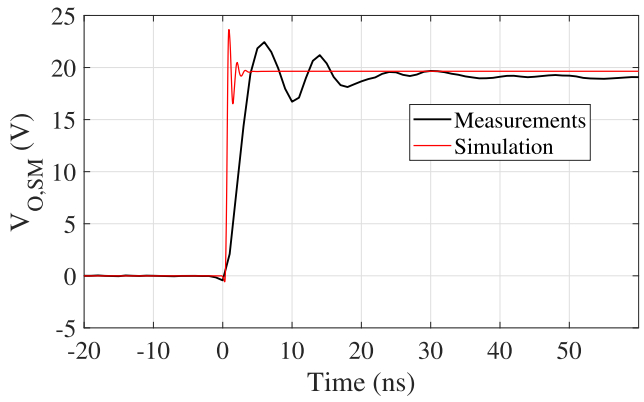


Fig. 8. Measured and simulated step response of the pDAC loaded by a 33-Ω resistor showing 5-kV/μs slew rate (limited by voltage probe); simulations predict a slew rate of 50 kV/μs.

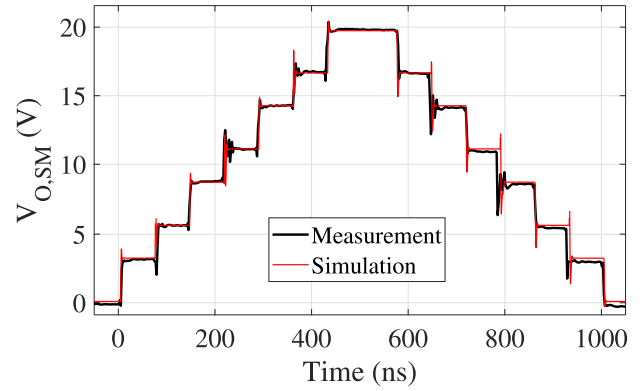


Fig. 9. Measured and simulated response of the pDAC to a staircase of 1 μs sweeping all the eight voltage levels.

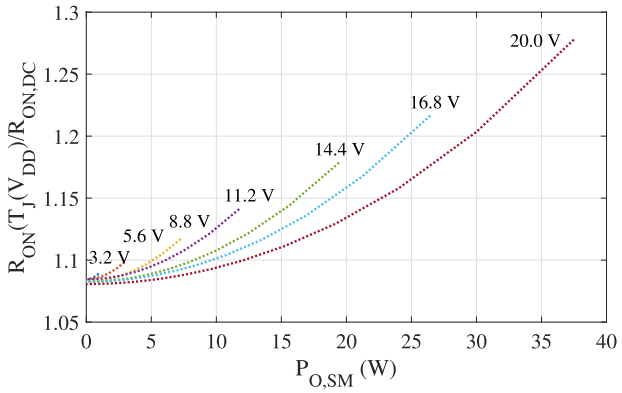


Fig. 10. Calculated dynamic R_{ON} variation with respect to $R_{ON,dc}$ due to the combined effects of self-heating and trap-induced degradation. A higher R_{ON} variation is estimated at increasing V_{DD} voltages and $P_{O,SM}$ power levels.

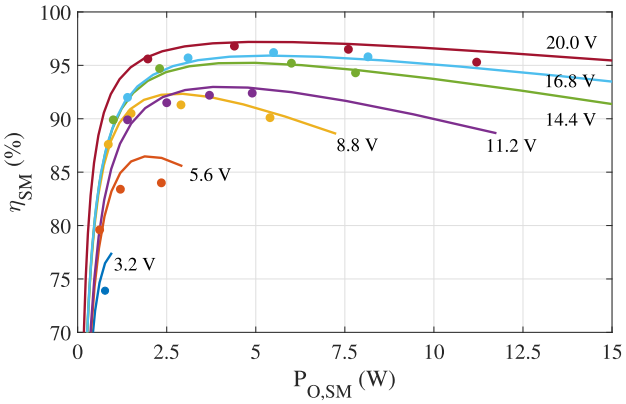


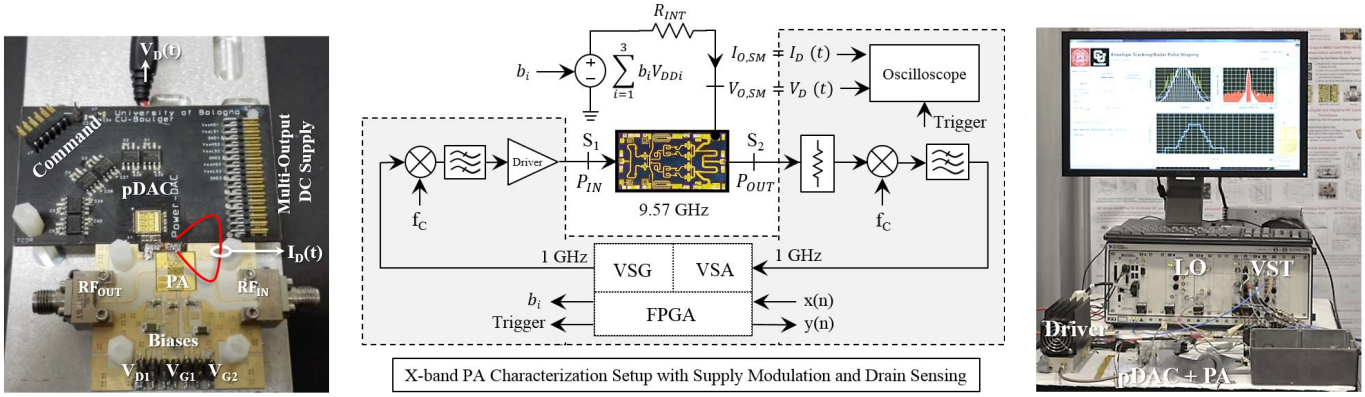
Fig. 11. Calculated (continuous line) and measured (dots) pDAC efficiency. At low output powers, the efficiency drops due to the static power losses in the drivers; on the other hand, at high output powers, the losses are dominated by the switch R_{ON}'s. At moderate output powers, a peak efficiency of 97% at $V_{O,SM} = 20$ V is measured.

However, the contribution of (10) and (11) can be neglected given the extremely low parasitics of the Qorvo 0.15-μm process ($f_T = 38$ GHz [22]) and the average switching frequencies achieved with the considered 20-MHz LTE signal. For the largest device used in the chip (9.6 mm), the input and output capacitances are $C_{GS} \simeq 14.4$ pF and $C_{DS} \simeq 3.8$ pF, while the gate commutation voltage is $V_{GS} = 5$ V. With the 20-MHz LTE signal, the average switching frequencies of the half-bridges are $\langle f_{b_1} \rangle = 1.8$ MHz, $\langle f_{b_2} \rangle = 7.1$ MHz, and $\langle f_{b_3} \rangle = 2.5$ MHz. For half-bridge supply voltages $V_{DD1} = 3.2$ V, $V_{DD2} = 5.6$ V, and $V_{DD3} = 11.2$ V, the switching losses due to the capacitors are found to be 8.7 mW. Regarding the free-wheeling diode losses, similar consideration apply: the diode forward voltage in this process is about $V_F = 1.2$ V and the deadtime $t_{DT} = 1$ ns is generated in the field-programmable gate array (FPGA) by using a secondary clock at 480 MHz and sampling during the rise and fall times. Assuming an average output current $I_{OUT} = 0.5$ A, these losses amount to 6.8 mW. If the capacitances of the process were higher or for higher average output currents, the contribution due to the switching losses could be neglected. A good comparison is the hybrid version of the pDAC [7], where $C_{GS} \simeq 300$ pF and $C_{DS} \simeq 150$ pF. In Section VI, a quasi-static PA-modulator efficiency characterization confirms this conclusion.

A. Power-DAC Characterization and Model Validation

The pDAC supply modulator is characterized in terms of slew rate, switching speed, and efficiency on various low-inductance resistive loads. The half-bridge supply voltages are $V_{DD1} = 3.2$ V, $V_{DD2} = 5.6$ V, and $V_{DD3} = 11.2$ V. The pDAC output voltage is measured with a 500-MHz passive probe (Agilent 1161A).

The output voltage, when all high-side switches are activated, is shown in Fig. 8 for a 33-Ω load. The measured slew rate of 5 kV/μs is surely limited by the probe performance; the simulation predicts 50 kV/μs. The measured and simulated converter response to a full voltage swing of a 500-ns ramp is reported in Fig. 9. By observing the 71.4-ns long steps, the longest settling time of the measured ringing is about 20 ns while the simulations predict about 5 ns. The longer settling time at the beginning of the 11.2-V level is due to the possible misalignment in the switching of the three half-bridges for the commutation 011 $\leftrightarrow$ 100.



(a) (b) (c)

Fig. 12. (a) Photograph of the fixture with the pDAC and PA. The output of the pDAC PCB is connected to the PA with a low-parasitics interconnect. During the characterization, a wire is added between the pDAC and PA to accommodate the current probe. (b) Setup block diagram. A frequency extension to X-band is employed and calibrated at the input S_1 and output S_2 of the PA. An FPGA controls the pDAC supply modulator while a synchronized oscilloscope acquires the drain voltage and current. (c) Photograph of the characterization setup.

The pDAC efficiency (2) can be measured by considering various loads R_L and output voltage levels. An important parameter that needs to be carefully estimated for an accurate prediction is the operating junction temperature $T_{J,\mathrm{EQ}}$. This can be evaluated with the thermal network

$$T_{J,\mathrm{EC}} = R_{\mathrm{JA}} P_{\mathrm{DISS}} + T_A \tag{12}$$

in which $R_{JA} = 17.5\,^{\circ}\mathrm{C/W}$ is the estimated junction-to-ambient thermal resistance and $T_A = 25\,^{\circ}\mathrm{C}$ is the ambient temperature. The calculated variation of the ratio of dynamic and dc R_{ON} is shown in Fig. 10. From such results, the pDAC efficiency of (2) can be computed as reported in Fig. 11. In this plot, we observe an efficiency drop at low output powers due to the fixed driver losses given by (9). As the output power increases, the losses are dominated by switch ON-resistances. The peak efficiency is reached at moderate output powers ($P_{O,\mathrm{SM}} = 4.8$ W) and at the maximum output voltage ($V_{O,\mathrm{SM}} = 20$ V), in which the combination of conduction and driving losses provides a peak efficiency of 97.2%.

This efficiency model is validated with measurements of the pDAC loaded by different R_L resistors from 12.5 to 200 Ω depending on the output power and voltage. The pDAC is controlled to generate the seven output levels and the voltage is measured with a multimeter. The output power is calculated as $V_{O,\mathrm{SM}}{}^2/R_L$ while the input currents of the three half-bridges and driver supplies are sensed with a current probe. The validation shows a good agreement with the model (Fig. 11).

IV. GaN Transmitter Characterization

Following the static characterization from the previous section, dynamic characterization of the pDAC connected to the PA is performed. The commutation rate of the pDAC is on the order of μs in these measurements, so that the modulator efficiency is still dominated by static losses. The PA MMIC presented in Section II is mounted on a CuMo fixture that is, in turn, mounted on a Rogers TMM10i substrate with SMA/3.5-mm connectors for the input–output RF paths and dc bypass capacitors in the gate and first-stage drain biases.

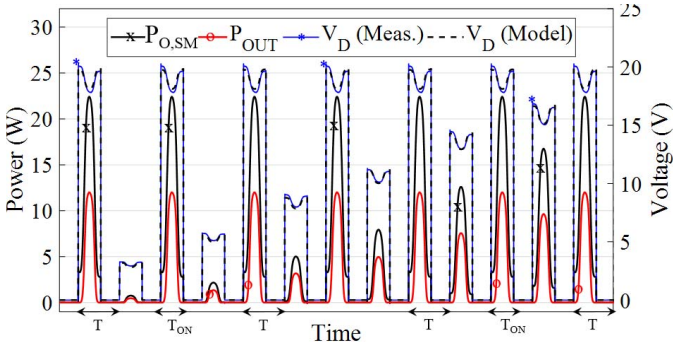


Fig. 13. Pulse train employed to extract the characteristics of the pDAC + PA. The pulse duration is $T_{\mathrm{ON}} = 10$ μs and the repetition period is $T = 100$ μs. The visible voltage drop in $V_D(t)$ is due to the internal resistance R_{INT} in the pDAC.

The drain of the second stage is directly connected to the pDAC supply modulator through a low-inductance interconnect. Simulations result in the layout shown in Fig. 12(a) in which a very short trace with an inductance of 5 nH connects the pDAC chip to the PA drain pad. The resonant frequency of the interconnect inductance and the 36.2 pF capacitance on the chip is 373 MHz, which is well outside the targeted LTE bandwidth of 20 MHz.

A. Characterization Setup

The block diagram and photograph of the characterization setup are shown in Fig. 12. This setup is described in [21] and is here briefly reported for completeness. An NI PXIe-5644R Vector Signal Transceiver (VST) is extended to X-band operation with custom-made upconversion and downconversion stages. The input I/Q signal, $x(n)$, is stored in the vector signal generator (VSG) and is first upconverted at 1 GHz within the instrument. An external mixer and a bandpass filter modulate an X-band carrier with the output of the VSG, and a broadband driver amplifies this signal to the nominal input power level (20 dBm). The output of the PA is then attenuated, downconverted, and sampled by the vector signal analyzer

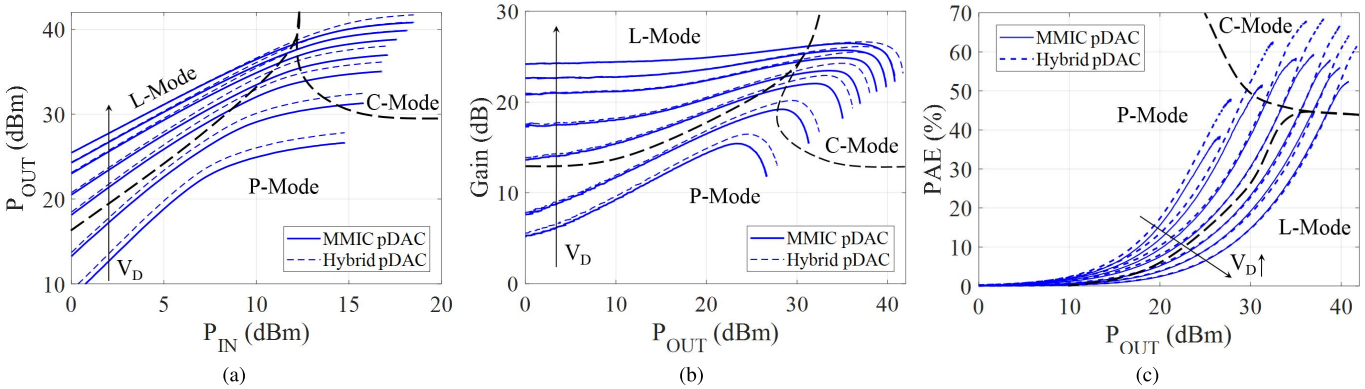


Fig. 14. Measured (a) input–output, (b) gain, and (c) PAE characteristics obtained with the PA connected to the pDAC (continuous line) and to the hybrid pDAC (dashed line). The PA performs better in P- and C-mode regions [6] when modulated with the hybrid low-resistance pDAC. In L-mode, no significant difference between the two pDACs is observed.

to generate the baseband I/Q signal $y(n)$. Simultaneously, an oscilloscope synchronously samples the PA drain voltage, $V_D(t)$, and current, $I_D(t)$. The time alignment between x, y, V_D, and I_D is software-controlled. The setup is verified for distortion showing minimal gain compression (0.1 dB) and flatness ($+/-0.2$ dB) over the 80-MHz bandwidth of the VST [21]. During the PA characterization phase, an additional wire is introduced between the pDAC and the PA as shown in Fig. 12(a) and clamped to a wideband current probe (Keysight 1147A). After the PA characterization, this wire is removed to restore the low-impedance connection between the PA and the pDAC.

B. RF Characterization Results

The PA is characterized at 9.57 GHz at different supply levels, V_D, generated by the pDAC, and with the pulse sequence shown in Fig. 13. Here, we employ a prepulsing characterization sequence in order to extract accurate efficiency and power characteristics of the PA [21]. In this sequence, a "prepulse" at the maximum supply voltage, $V_D = 20$ V, is employed to fully activate the trap capture in the PA transistors; afterward, a "measurement pulse" extracts the PA characteristics at variable amplitudes under controlled trap and thermal states.

In the prepulsing sequence (Fig. 13), the drain voltage experiences a remarkable drop at the times when RF output power peaks, caused by the pDAC internal resistance. At the PA peak output power, the peak current is 1.4 A, and this leads to a voltage drop of about 1.7 V, resulting in an internal resistance $R_{\mathrm{INT}} \simeq 1.2\ \Omega$ ($R_{\mathrm{ON}} \simeq 0.4\ \Omega$). We note that the PCB inductance of 5 nH does not contribute to the voltage drop given the negligible impedance (3 mΩ) at the fundamental frequency of the current pulse (10 μs). Along with the measured $V_D(t)$, Fig. 13 shows the predicted pDAC output voltage found from (3) showing a good agreement also under dynamic conditions.

The pDAC internal resistance penalizes the transmitter efficiency in two ways: on the one hand, it causes conduction losses in the supply modulator as in (6), thus reducing the supply modulator efficiency, η_{SM}. On the other hand, it affects the PAE of the amplifier. The former is demonstrated by

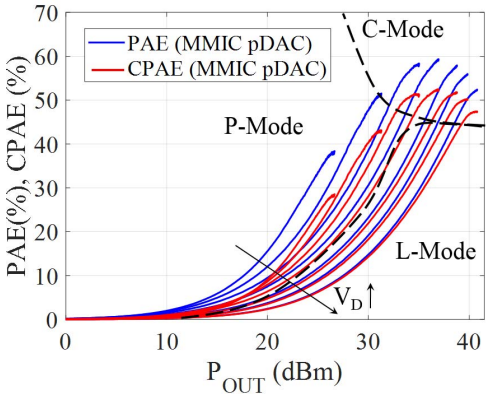


Fig. 15. Composite PAE (red line) of the pDAC and PA ICs obtained by combining the modulator efficiency with the measured PAE (blue line). The pDAC internal resistance degrades the CPAE in the P- and C-mode regions, whereas no difference is observed in L-mode.

comparing the performance of the PA connected to the hybrid version of the pDAC [7], which has an almost negligible internal resistance ($R_{\mathrm{INT}} \simeq 50$ mΩ) and is effectively a quasi-ideal voltage source at this current level ($I_{O,\mathrm{SM,MAX}} = 1.4$ A).

The input–output and gain characteristics of the PA, with the two supply modulators, are compared in Fig. 14, with three distinct operating modes identified: linear (L) mode, compressed (C) mode, and product (P) mode where the PA behaves as a mixer [6]. For high supply voltages and low RF powers, the PA operates in L-mode and the RF output power and gain are insensitive to the small voltage drop caused by the internal pDAC resistance. As the RF input power increases toward C-mode, the output power and gain become sensitive to the supply voltage, the peak power decreases from 41.7 (14.8 W) to 40.8 dBm (12 W) with the pDAC, and the large-signal gain reduces from 23.2 to 22.3 dB.

If the hybrid pDAC is assumed to be an ideal voltage source, the PA supply sensitivity, defined in [27], is found to be 1.5 W/V in C-mode for the supply levels "5," "6," and "7." This value is approximately independent of the supply modulator since it is an intrinsic characteristic of the PA in compression. For the remaining levels, this sensitivity drops from 1.2 to 0.3 W/V, respectively, at the level "4" and "1."

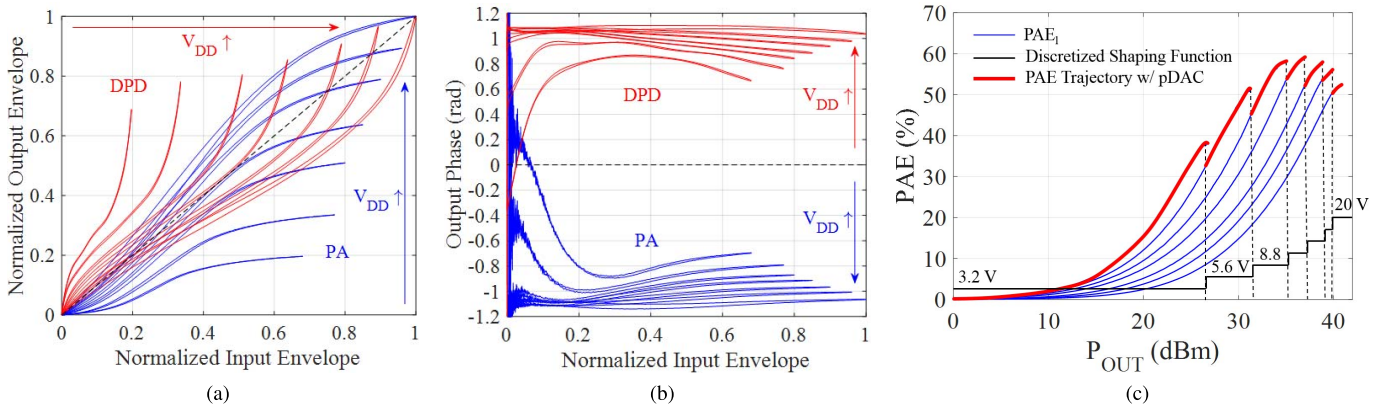


Fig. 16. (a) AM/AM and (b) AM/PM characteristics of the PA at V_{DD} voltage levels; the nonlinear characteristics with memory of the PA (blue) are superposed to the inverted nonlinear characteristics with memory of the DPD (red). (c) PAE characteristics and discretized shaping function (black continuous). Efficiency is maximized with SM following the trajectory highlighted in red.

For low supply voltages, the PA operates in P-mode in which the output power and gain are both sensitive to the supply voltage drop, and also to the input power, resulting in mixerlike operation. The PA gain in P-mode peaks at higher powers and is reduced at lower power. The transistors are operating in the triode region at low supply voltages and, therefore, with a very low transconductance, which is additionally degraded by the trap-induced "current collapse," as observed during prepulsing [21].

Next, the PA is characterized in terms of PAE both with the hybrid and the integrated version of the pDAC and the results are provided in Fig. 14(c). The PAE plane can be again qualitatively divided into L, C, and P modes to highlight the PA drop caused by the pDAC internal resistance. In C-mode and at the peak output power, the amplifier PAE reduces from 57.8% to 52.3% and similar degradation is observed for all the other supply levels. Only in the L-mode, the PAE remains unchanged with the pDAC IC. The relevant efficiency for a supply-modulated PA is the *composite PAE* (CPAE), defined as

$$\text{CPAE} = \eta_{\text{SM}} \cdot \text{PAE} \tag{13}$$

where η_{SM} is the pDAC efficiency defined and characterized in Section III, and PAE is the amplifier PAE when connected to the pDAC IC. Recall that the static pDAC characterization is valid with the PA in place of the resistor since the characterization is performed with narrowband pulses (10-μs pulse, 100-μs period). The calculated CPAE is shown in Fig. 15, where the PA efficiency degradation due to the pDAC IC is noticeable, but the CPAE is still high and reaches 47% at the peak output power of 40.8 dBm and is higher in backoff by design. At low output power, the CPAE is reduced due to the static power dissipation in the pDAC drivers; on the other hand, at high output power, the internal resistance in the power switches dominates. In some cases, the difference between PAE and CPAE can be as large as 10% points, while the same comparison using the hybrid pDAC shows a maximum difference of three points since its efficiency is always over 95% [7].

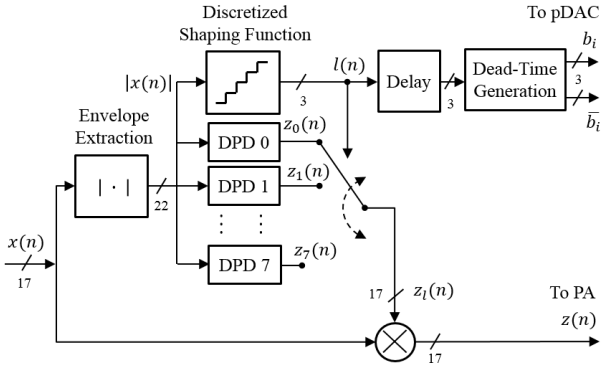


Fig. 17. Block diagram of the digital baseband. An envelope extraction block generates $|x(n)|$ and is followed by the discretized shaping function that generates an eight-level pDAC control and the switching between DPDs, which are applied to $x(n)$ with a multiplier.

C. Baseband Characterization and Linearization

The nonlinearities of the supply-modulated PA shown by the normalized AM/AM and AM/phase modulation (PM) characteristics [Fig. 16(a) and (b)] are affected by the pDAC internal resistance. Improved average efficiency is achieved when the supply voltage follows a discretized trajectory shown in Fig. 16(c). The thresholds of this shaping function are selected as the peak power at the lth voltage level that maximizes the PAE when the MMIC PA is connected to the pDAC IC. A vector-switched digital predistortion (DPD) [28] is chosen so that every region of this model corresponds to the inverted characteristics of the PA at a fixed supply voltage, as shown in Fig. 16. This approach has the same digital complexity as a typical DPD for a fixed-supply PA since the knowledge of PA behavior is only necessary in the discrete intervals defined by the discretized shaping function, with a small overhead of a multiplexer at the output of the DPD blocks.

A generalized memory polynomial (memory order 3, nonlinearity order 7) [29] is chosen to fit each region of the vector-switched DPD. The digital baseband of the transmitter, including the predistortion, is implemented in the FPGA

TABLE II
PERFORMANCE WITH DIFFERENT PULSE WAVEFORMS FOR RADARS

Amplitude Taper (PAPR)	Control Mode	-3 dB Bandwidth	1^{st} Time Sidelobe	Power per Pulse W (dBm)	IC pDAC PAE η_{SM} CPAE	Hybrid pDAC* PAE η_{SM} CPAE
Rectangular (0.00 dB)	Rectangular	4.5 MHz	-13.5 dB	10.5 (40.2)	54.4% 93% 50.6%	65.0% 96% 62.4%
Triangular (3.00 dB)	Rect. + DPD	1.6 MHz	-26.2 dB (ideal)	3.7 (35.7)	34.9% 90% 31.4%	35.1% 96% 33.4%
Triangular (3.00 dB)	**SM + DPD**	**1.6 MHz**	**-26.2 dB (ideal)**	**3.7 (35.7)**	**53.3% 85% 45.3%**	**58.9% 95% 55.9%**
Hanning (3.01 dB)	Rect. + DPD	1.9 MHz	-31.4 dB (ideal)	4.1 (36.1)	38.7% 90% 34.9%	40.2% 96% 38.6%
Hanning (3.01 dB)	**SM + DPD**	**1.9 MHz**	**-31.4 dB (ideal)**	**4.1 (36.1)**	**52.9% 87% 46.0%**	**59.3% 95% 56.3%**
Blackman (3.77 dB)	Rect. + DPD	1.5 MHz	-52 dB (ideal -58 dB)	3.3 (35.2)	35.8% 89% 31.9%	37.2% 96% 35.7%
Blackman (3.77 dB)	**SM + DPD**	**1.5 MHz**	**-52 dB (ideal -58 dB)**	**3.3 (35.2)**	**52.4% 84% 44.0%**	**58.1% 95% 55.2%**

* Efficiency results obtained in [30] with a similar PA (same maximum output power, but with 65% peak PAE vs. 61% of this PA).

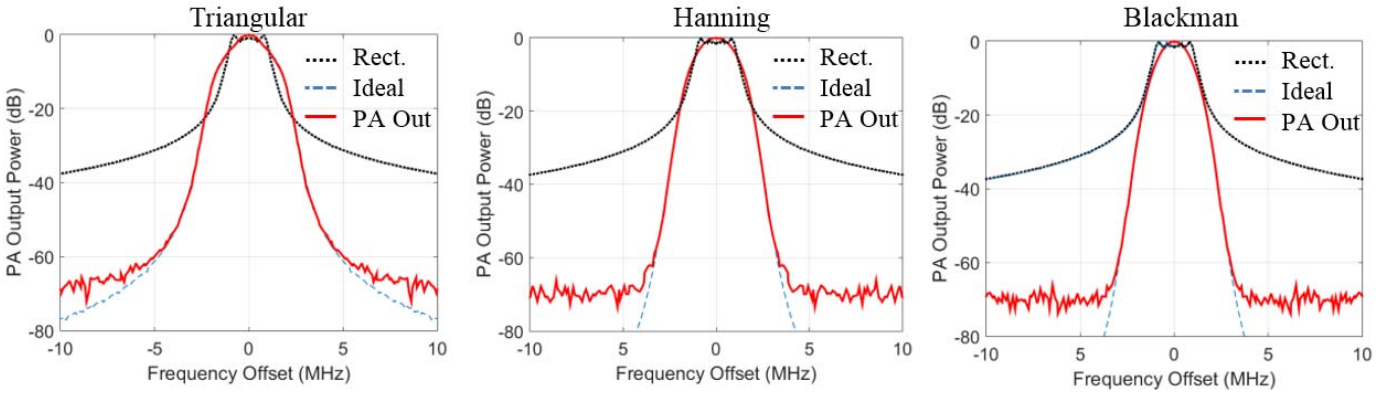


Fig. 18. PA output spectra with DPD enabled. The three weighting windows are compared with a rectangular chirped pulse (black dotted). Similar bandwidth (i.e., range resolution) can be obtained but with improved spectral confinement (red solid).

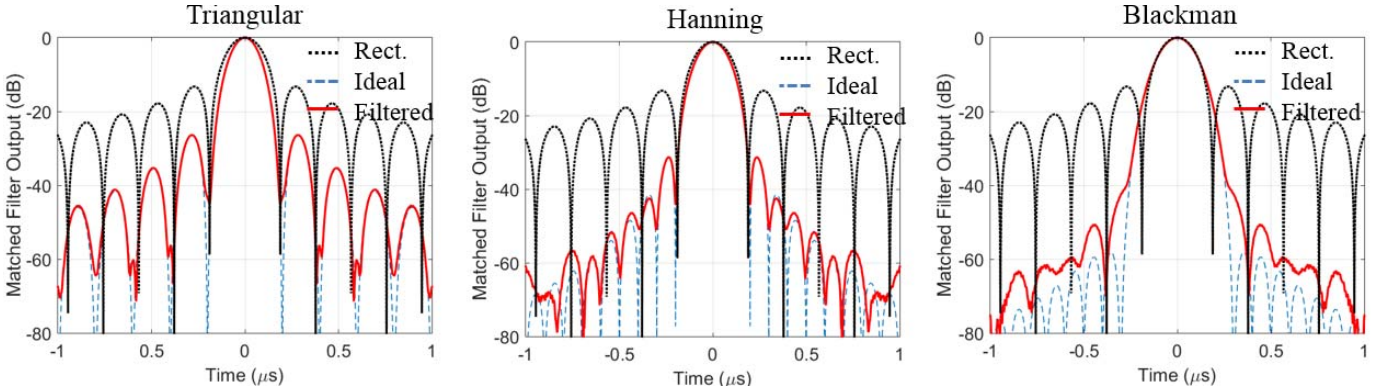


Fig. 19. Output of the matched filter in a pulse-compressed radar receiver utilizing linear frequency modulation. Lower temporal sidelobes are obtained by means of amplitude weighting of the transmitted signal.

within the VST (Fig. 17). The input I/Q sequence, $x(n)$, is used to generate the continuous envelope $|x(n)|$ extracted with a 22-bit resolution, quantized in eight levels by a discretized shaping function and coded with three bits to generate the pDAC control $l(n)$. Seven correction coefficients $z(n)$ (one is $V_D = 0$ V and does not require DPD) are fetched in parallel in the seven DPD lookup tables. The multiplexer selects the $z(n)$ value to apply to the original input $x(n)$.

V. GaN TRANSMITTER EXPERIMENTAL RESULTS

The transmitter is tested with two types of signals: radar-type amplitude- and frequency-modulated pulses and high-PAPR signals for high-capacity communications. In both cases, a dramatic improvement in CPAE is demonstrated while linearity is maintained. We note that in this efficiency calculations, the power consumption of the digital isolators is taken into account, while the efficiency of generating the input supply voltages $V_{\mathrm{DD}i}$ is not included.

TABLE III
PERFORMANCE WITH DIFFERENT LTE DOWNLINK CHANNELS

Bandwidth	PAPR	Control Mode	EVM	ACLR*	$P_{OUT,AVG}$	$P_{IN,AVG}$	P_{DD}	CPAE
1.4 MHz	9.3 dB	Fixed Supply + DPD	1.83%	52 dB	1.38 W	19.2 mW	7.04 W	19.4%
1.4 MHz	**9.3 dB**	**Supply Modulation + DPD**	**2.44%**	**46 dB**	**1.41 W**	**7.5 mW**	**3.50 W**	**40.1%**
10 MHz	11.3 dB	Fixed Supply + DPD	2.46%	49 dB	0.91 W	13.0 mW	6.22 W	14.4 %
10 MHz	**11.3 dB**	**Supply Modulation + DPD**	**3.93%**	**34 dB**	**1.02 W**	**5.1 mW**	**2.94 W**	**34.5%**
20 MHz	11.4 dB	Fixed Supply + DPD	2.90%	47 dB	0.74 W	10.5 mW	6.56 W	11.1%
20 MHz	**11.4 dB**	**Supply Modulation + DPD**	**5.24%**	**33 dB**	**0.85 W**	**4.1 mW**	**2.65 W**	**32.0%**

ACLR: defined as the ratio of the average power in the channel bandwidth and the average power centered in the next channel with the same bandwidth.

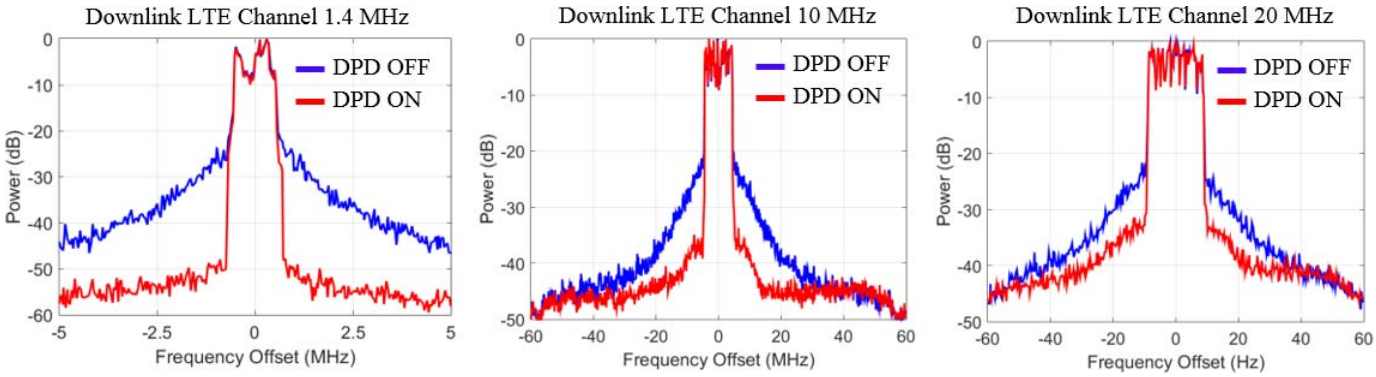


Fig. 20. Output spectra of the three LTE channels: 1.4 MHz (left), 10 MHz (center), and 20 MHz (right). The spectrum with DPD disabled is overlaid, showing spectral regrowth. The linearity performance with the 20-MHz signal is limited by the setup bandwidth (80 MHz).

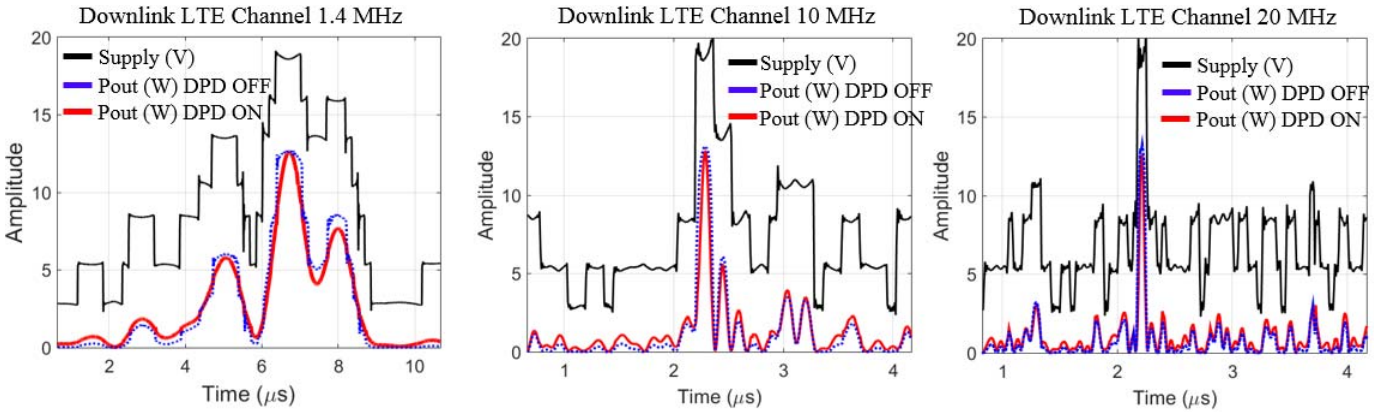


Fig. 21. PA output power with DPD enabled (red solid), DPD disabled (blue dotted), and drain voltage (black solid) of three LTE signals: 1.4 MHz (left), 10 MHz (center), and 20 MHz (right). The voltage supply ripple shows the effect of internal resistance in the pDAC IC.

A. Radar Signals

The range resolution of a radar is proportional to the bandwidth of the transmitted pulsed signal. Short pulses, however, reduce ranging capability, and pulse compression techniques overcome this tradeoff by frequency (i.e., chirping) or phase modulation (i.e., BPSK, Barker codes) with usually rectangular pulses [31]. Constant envelope pulses result in spectral spreading [30]–[34] and high time sidelobes (−13.2 dB) at the output of the matched filter in the receiver can obstruct the presence of a target or give false target detection. Introducing amplitude modulation to the pulse envelope can help with spectral confinement and significantly reduce sidelobes at the output of the matched filter in the receiver [31]. However, applying an amplitude modulation to the RF pulse envelope increases the dissipation in the PA, unless the PA supply voltage is modulated to track the efficiency peak [30].

To demonstrate this concept with this MMIC PA and supply modulator, we consider test signals with a pulse duration of 10- and 100-μs repetition period (10% duty cycle). The pulse envelope is shaped with three different windowing functions: triangular, Hanning, and Blackman [31]. Results are compared to the standard rectangular envelope pulse. Each pulse is frequency modulated with a 5-MHz linear chirp to increase the bandwidth while keeping the same pulse envelope and duration. Results of the three windowing functions are summarized in Table II. The output power spectra of

the three types of pulses are provided in Fig. 18, while the output of the matched filter on the receiver is shown in Fig. 19.

As expected, the rectangular pulse reaches the highest CPAE of 50.6% and the widest bandwidth of 4.5 MHz, with a very high first sidelobe at −13.5 dB. By tapering the pulse envelope with a Blackman window, it is possible to reduce the temporal sidelobes up to −52 dB. The efficiency improvement with the pDAC IC as compared to a pulsed constant supply is between 11% and 14% points. Table II also shows the efficiencies obtained with a similar PA and the hybrid pDAC [30], for only amplitude-modulated pulses. This comparison is included since the results are consistent with the efficiency characterization of both pDACs (Section IV). The hybrid pDAC + PA performs more efficiently due to lower internal resistance, leading to higher pDAC and PA efficiencies. It is interesting that the PA efficiencies are very similar with the two supply modulators for a rectangular drain pulse and input amplitude modulation, when the PA is operating most of the time in L-mode (and inefficiently) and so the impact of the supply modulator resistance in this operating mode is less evident, as also discussed in Section IV. When SM (SM + DPD case) is employed, the PA is operated in P- and C-modes; thus, the impact of the pDAC internal resistance penalizes the PAE, as also highlighted in Fig. 14(c).

B. Communication Signals

In this section we demonstrate the transmitter capability to efficiently amplify LTE channels of 1.4-, 10-, and 20-MHz bandwidth with PAPRs between 9.6 and 11.4 dB. For each signal, the transmitter performance for fixed supply voltage and modulated supply is compared, in both cases with DPD linearization. In-band metrics such as error vector magnitude (EVM), as well as out-of-band characteristics, such as the adjacent channel leakage ratio (ACLR), are evaluated. For these measurements, the short connection between the PA and the pDAC is reestablished and only the CPAE is measurable and reported in Table III. The RF input, $P_{\mathrm{IN,AVG}}$, and output average power, $P_{\mathrm{OUT,AVG}}$, are measured, as well as the total input dc power to the pDAC, P_{DD}, at the input of each half-bridge and driver of the pDAC. The DPD significantly reduces out-of-band distortion, as evident in Fig. 20. The time-domain drain voltage and RF output envelope for the considered signals are provided in Fig. 21 which also shows reduced discontinuities when DPD is employed. The nonperfect linearization of the 20-MHz LTE signal is most likely due to the bandwidth limitation constrained by the 80-MHz analog bandwidth of the VST-5644R; the nonlinear expansion of the DPD would require a bandwidth of 3−5 times the original bandwidth, exceeding the VST capabilities [1]. Nevertheless, the CPAE improves over 20 percentage points using SM as compared to the constant supply case while the supplied dc power is reduced more than 50%. The corresponding linearity performance is obviously somewhat deteriorated but still compliant with communication standards [35]. The CPAE variation from 40% to 32% for signals with 1.4 MHz versus 20 MHz bandwidth is likely due to the different PAPRs, i.e., 9.6 versus 11.4 dB, and does not depend on the signal bandwidth. Different PAPRs result in a different average RF output power (1.4 versus 0.85 W) that requires more power from the pDAC (about 2.8 versus 1.7 W, estimating a PA efficiency of around 50%). As can be observed in the characteristics shown in Fig. 11, this condition enables the pDAC to operate closer to its peak efficiency when the 1.4-MHz, 9.6-dB PAPR signal is considered.

VI. Conclusion

This paper details an X-band envelope-tracking transmitter with an MMIC PA and an integrated multilevel supply modulator (pDAC). The two chips are fabricated in the same 0.15-μm GaN-on-SiC depletion-mode process. Integrated transmitter performance is demonstrated within a very small footprint and shows a total composite efficiency (CPAE) improvement of 14% points for radar signals and 10 points for LTE signals over the constant supply case. One of the main contributions of this paper is detailed characterization of the losses in the overall transmitter, which includes the PA, dynamic supply, and drivers. Pulsed characterization is applied to extract the dynamic R_{ON} of the GaN switches in the pDAC, which affects the internal resistance of the supply modulator. An efficiency model of the pDAC with driving and conduction losses is developed and validated with measurements. The supply modulator demonstrates a slew rate of 5 kV/μs and a peak efficiency of 97.2% at 4.8-W output power.

The CPAE with a GaN IC pDAC is compared to that using a hybrid pDAC with enhancement-mode GaN-on-Si devices, showing the tradeoff in PAE and modulator internal resistance. The 0.15-μm microwave GaN process presents some drawbacks for the supply modulator integration as follows.

1) Only n-type devices are available, which makes it impossible to implement efficient fully-complementary drivers with zero static power dissipation.
2) The normally-ON devices are not ideal for power supplies since any failure in the driver supply produces a destructive short circuit of the power switches.
3) Additional bias voltages are required, with a consequent increased complexity of the external bias board and interconnections to the chip.
4) The relatively high R_{ON}/mm of this process and the further increase in dynamic R_{ON} due to trapping and thermal effects limit the maximum efficiency for high supply currents and impose the use of large periphery power switches (i.e., large chip area).
5) The significant internal resistance of the supply modulator not only impacts the efficiency of the supply modulator but also the performance of the PA by reducing its output power, gain, and efficiency.

Because of these issues and with the considered bandwidths, the integrated pDAC efficiency performance does not exceed that of hybrid pDAC implementations for radar and communication signals. However, the overall size of the pDAC integrated version is 10 times smaller than the hybrid pDAC with a higher power density. Further development of GaN technology, enhancement-mode power devices, and CMOS logic

will enable more efficient integrated solutions. In addition, the possibility of heterogeneous integration of CMOS and GaN technologies [36] would be ideally suited to a fully integrated and highly efficient transmitter using the architecture presented in this paper.

In conclusion, a 9.57-GHz 10-W 22-dB gain supply-modulated GaN transmitter with DPD is demonstrated on two signal types. An amplitude-modulated chirped pulse results in an average CPAE of 45%, showing 11%–14% points improvement over fixed supply operation, with a dramatic increase in linearity evidenced by up to 52 dBc first time sidelobe level. Furthermore, 1.4-, 10-, and 20-MHz LTE signals result in an overall efficiency between 32% and 40%, corresponding to an efficiency improvement of 20% points compared to the fixed supply case, with linearity recovered with DPD. The highly efficient performance obtained with two separate ICs shows the potential of a fully integrated PA-modulator chip.

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