Millimeter-wave GaN MMIC Integration with Additive Manufacturing

by

Michael Coffey

B.S., California State Polytechnic University, Pomona, 2010

M.S., University of Colorado, Boulder 2014

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical, Computer, and Energy Engineering

2017

This thesis entitled:
Millimeter-wave GaN MMIC Integration with Additive Manufacturing
written by Michael Coffey
has been approved for the Department of Electrical, Computer, and Energy Engineering

Zoya Popović

Michael DeLisio

Date

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Coffey, Michael (Ph.D., Electrical Engineering)

Millimeter-wave GaN MMIC Integration with Additive Manufacturing

Thesis directed by Zoya Popović

This thesis addresses the analysis, design, integration and test of microwave and millimeter-wave monolithic microwave integrated circuits (MMIC or MMICs). Recent and ongoing progress in semiconductor device fabrication and MMIC processing technology has pushed the upper limit in MMIC frequencies from millimeter-wave (30 - 300 GHz) to terahertz (300 - 3000 GHz). MMIC components operating at these frequencies will be used to improve the sensitivity and performance of radiometers, receivers for communication systems, passive remote sensing systems, transceivers for radar instruments and radio astronomy systems. However, a serious hurdle in the utilization of these MMIC components, and a main topic presented in this thesis, is the development and reliable fabrication of practical packaging techniques.

The focus of this thesis is the investigation of first, the design and analysis of microwave and millimeter-wave GaN MMICs and second, the integration of those MMICs into usable waveguide components. The analysis, design and testing of various X-band (8-12 GHz) thru H-band (170-260 GHz) GaN MMIC power amplifiers (PA or PAs), including a V-band (40-75 GHz) voltage controlled oscillator, is the majority of this work. Several PA designs utilizing high-efficiency techniques are analyzed, designed and tested. These examples include a 2^{nd} harmonic injection amplifier, a Class-E amplifier fabricated with a GaN-on-SiC 300 GHz f_T process, and an example of the applicability of supply-modulation with a Doherty power amplifier, all operating at 10 GHz. Two H-band GaN MMIC PAs are designed, one with integrated CPW-to-waveguide transitions for integration. The analysis of PA stability is especially important for wideband, high-f_T devices and a new way of analyzing stability is explored and experimentally validated.

Last, the challenges of integrating MMICs operating at millimeter-wave frequencies are discussed and assemblies using additive and traditional manufacturing are demonstrated.

Dedication

This thesis is dedicated to my mother Teresa, my girlfriend Caitlyn, and my dear old Granddad, for their help is how I got through it.

Acknowledgements

This thesis was made possible by the constant hard work of Zoya Popović to do her best as an educator, professor, and research advisor. Without her, there would be a lot less PhDs in the world, including my own. I would like to acknowledge the people I have worked with in this field who are my role models for hard work and persistence: Mike DeLisio, Chad Deckman, Miroslav Micović, Gregor Lasser, Mike Litchfield, Scott Schafer and Maxwell Duffy. I want to also acknowledge the people I worked with who made it a better experience in the lab and in Boulder: Andrew Zai, Sean Korhummel, Ignacio Ramos and Mauricio Pinto. The last year of the program had various deadlines and pressures of its own and my friend and neighbor Blaine Krumpe has to be credited for making me forget them often.

Contents

Chapter

Tables

Table

Figures

Figure

Chapter 1

Introduction and Motivation

Contents

Advances in MMIC design and fabrication have been the driver for continually improving performance in wireless systems such as cellular phone technology, satellite communications, military and automotive radar systems, electronic warfare, radiometers, and remote sensing technology. A MMIC is a monolithic microwave integrated circuit, such as the ones designed and fabricated in this work and shown in Figs. 1.2a - 1.2d. The monolithic part of the name refers to the fact that the circuit is fabricated on a single piece of semiconductor material, usually GaAs, GaN, InP or SiGe. The microwave part of the name refers to the fact that the circuit is operating between 300 MHz to 300 GHz [13]. The last important part of the name is integrated which refers to the fact that the MMIC does not contain a single transistor or device, but a mix of transistors, diodes, capacitors, inductors, transmission lines, integrated antennas, and RF and DC interface structures. Further integration, such as on-die power conversion and control circuits is an on-going research topic in this field. Similar to silicon developments, one day an entire RF system might be on a single chip (system-on-a-chip). The design of millimeter-wave MMICs, that is MMICs that operate above 30 GHz, is the main focus of this work.

MMIC design and fabrication is a relatively new field, the first MMIC was reported in 1976

in [14] and advances in output power, gain, operating frequency, and efficiency are continually being made. In Fig. 1.1 the output power, frequency of operation and year of reported result for various millimeter-wave MMIC PAs and oscillators is shown. There are few results before 1995. A summary of the technology progression is also shown in table form in Table 1.1.

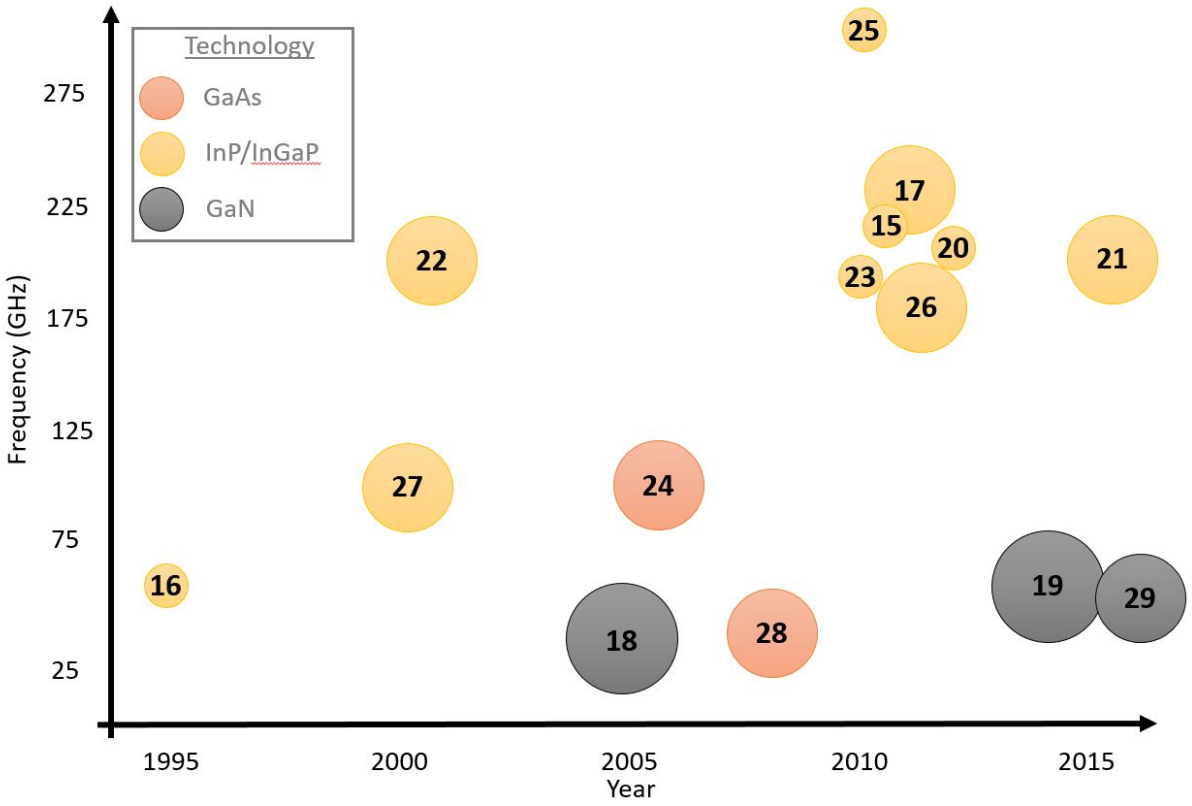
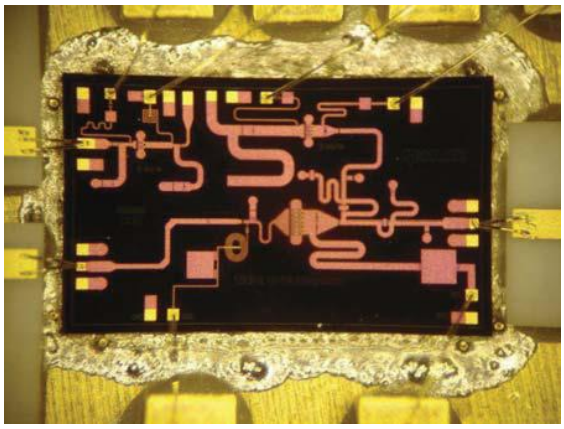


Figure 1.1: Millimeter-wave MMIC technology progression over the years with a variety of output power levels, operating frequencies and different fabrication technology. The three marker sizes represent <10 mW, between 10 mW and 1 W, and >1 W.

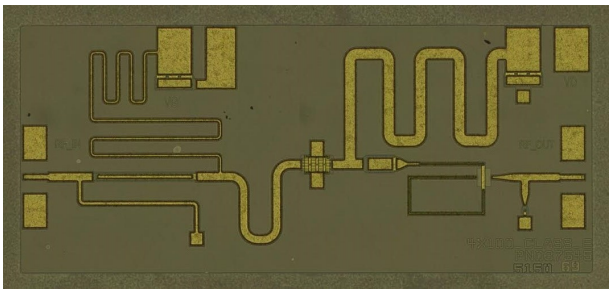
Table 1.1: Summary of results in the above MMIC technology figure.

$Freq.$ (GHz)	P_{out} (mW)	Tech.	Year	Ref.
220	10	InP	2010	[15]
60	8.128	InP	1995	[16]
220	50	InP	2010	[17]
28-34	4000	GaN	2005	[18]
70	1300	GaN	2014	[19]
220	0.724	InP	2011	[20]
200	220	InP	2015	[21]
205	250	InP	2001	[22]
192	7.94	InP	2009	[23]
90	267	GaAs	2005	[24]
324	1.3	InP	2008	[25]
195	100	InP	2013	[26]
90	427	InP	1999	[27]
46	151.35	GaAs	2007	[28]
70	800	GaN	2016	[29]

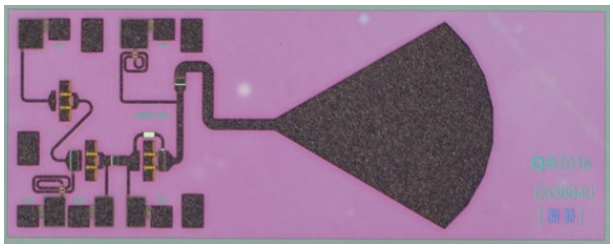
The goal of this thesis is to explore non-conventional circuit designs using advanced GaN MMIC technologies, with a focus on increasing operating frequency and output power. A summary of the MMICs designed towards this goal is shown in Figs. 1.2a - 1.2d. Starting from a 0.15 μm gate length commercial GaN process, the first harmonically-injected 10-GHz MMIC PA is successfully implemented and shows the possibility of achieving simultaneous high efficiency and linearity without analog or digital predistortion (DPD). The output harmonic injection MMIC PA demonstrated a PAE of 70% at 10.6 GHz with 3.6 W of output power in a 3.8 mm x 2.3 mm footprint. Next, a 10 GHz Class-E amplifier was designed and fabricated in a 20 nm gate length, $f_T > 300$ GHz, process to investigate the effects of gate geometry scaling on efficiency. f_T, the transition frequency, is the maximum frequency where a transistor can amplify. The Class-E amplifier achieved $> 55\%$ efficiency at 9 GHz with 8 dB of gain. The third design, Fig. 1.2c, is a U- and V-band (40-60 and 50-75 GHz respectively) VCO designed in a 90 nm gate length process. Last, in Fig. 1.2d, the same $f_T > 300$ GHz process was used to fabricate a power combined 235 GHz GaN MMIC.



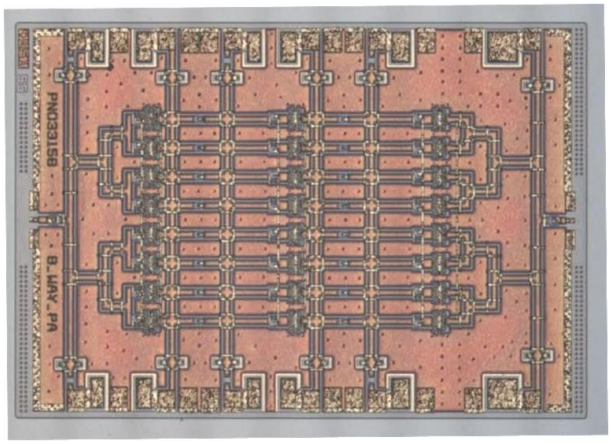
(a)



(b)



(c)



(d)

Figure 1.2: (a) 10 GHz output harmonic injection MMIC PA (b) 10 GHz Class-E amplifier MMIC PA (c) V-band VCO (d) 235 GHz 8-way combined MMIC PA.

Millimeter-wave applications require that the MMIC be packaged properly and typically interface to waveguide for test and integration. To investigate new methods of packaging and interfacing with millimeter-wave MMICs, the V-band VCO and 235 GHz power combined PA include microstrip-to-waveguide or CPW-to-waveguide transitions. While this work does not focus on the fabrication technology of these devices, the design of a MMIC inherently requires some knowledge of the relevant manufacturing terms and of how planar transistor layouts look. An overview of the important terms used in this thesis is given so that the reader can understand the concepts they relate to. Last, an overview of each thesis chapter is presented.

1.1 Introduction to MMIC Technology and Design

The work in this thesis revolves around access to high-frequency transistor technology and low-loss passive interconnects and component technology. The layout view of a typical high-frequency transistor used in this work is shown in Fig. 1.3. The important parameters are the number of gate fingers, the gate width, and the gate length. In Fig. 1.3, the transistor has a 75 μm gate width, 8 gate fingers and the gate length is 0.15 μm, which is not given from the layout view, but is a process dependent parameter.

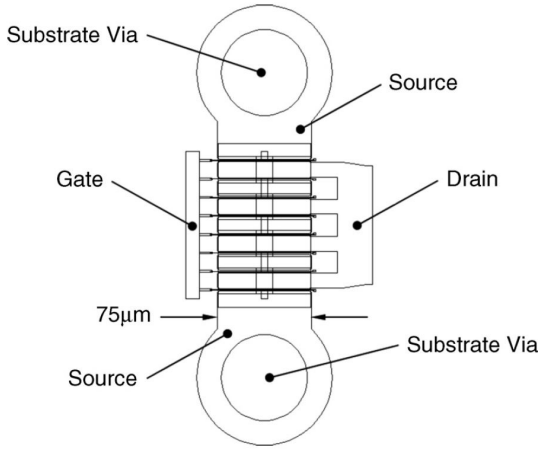


Figure 1.3: A typical FET layout cell. This device is 8x75 μm, for a total periphery of 600 μm. With a 3.4 W/mm output power density, this device has a potential output power of $>$ 2W. Source: [1]

Shrinking the gate length continues to be the primary method of achieving higher frequency operation in MMICs. The above example transistor would be referred to as a 8x75 μm device. By knowing the MMIC fabrication process power density limits and the single device (frequently called the unit cell) periphery, the total theoretical output power of a multi-transistor PA can be determined. Other terms used in this work are defined below:

- SiC substrate - All of the MMICs presented in this thesis are fabricated on silicon carbide (SiC) substrates. The transistor devices are all gallium nitride (GaN), so the processes used to fabricate the circuits are often called GaN-on-SiC. Several different SiC polytypes (crystal

structures that vary in one dimension from each other) are popular, with 4H and 6H being widely used. The use of different polytypes results in slightly different dielectric constants for the substrates, from $\epsilon_r = 9.7$ to 10. SiC substrates are used for high-power density microwave circuits because they have high thermal conductivities, from 390-490 W/m-K. Commercially available SiC wafers are currently sold in a variety of diameters, from 76 to 150 mm [30].

- HEMT - All of the transistor devices in this thesis are metamorphic high electron mobility transistors (HEMTs). The use of GaN HEMTs implies several characteristics that all the MMICs in this work share. First, the devices have a positive drain voltage supply in the range of 4 - 20 V, depending on the gate length. In general, shorter gate lengths result in higher frequency performance but lower breakdown voltages, V_{br} or $V_{breakdown}$. With the exception of very advanced processes, microwave HEMTs utilize a depletion mode topology, meaning the gate voltage that controls the flow of electrons or two dimensional electron gas (2DEG) in the device is negative in reference to ground. This means the devices must be biased with a negative gate voltage (pinched-off) before applying the drain supply voltage.

- T-gate and Γ-gate - These structures are important breakthroughs in device technology that allow GaN HEMTs to operate at high frequencies and/or with high output power. The T-gate from the process used in chapter 4 is shown in Fig. 1.4. The Γ-gate from the process used in chapter 3 is shown in Fig. 1.5. The Γ-gate is a modified T-gate that reduces the gate parasitics to allow for higher frequency operation and output power.

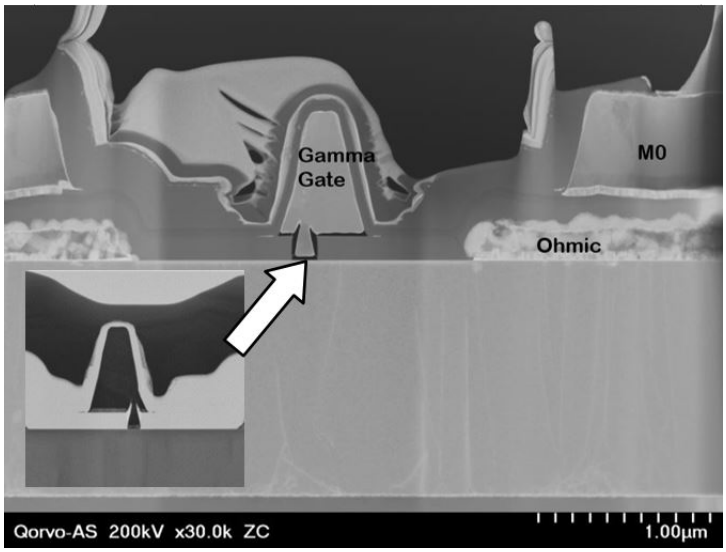


Figure 1.4: A SEM photograph of the gamma-gate used in Chapter 3. The transistors in this process exhibit $f_T > 72\,\text{GHz}$. Photograph: Qorvo

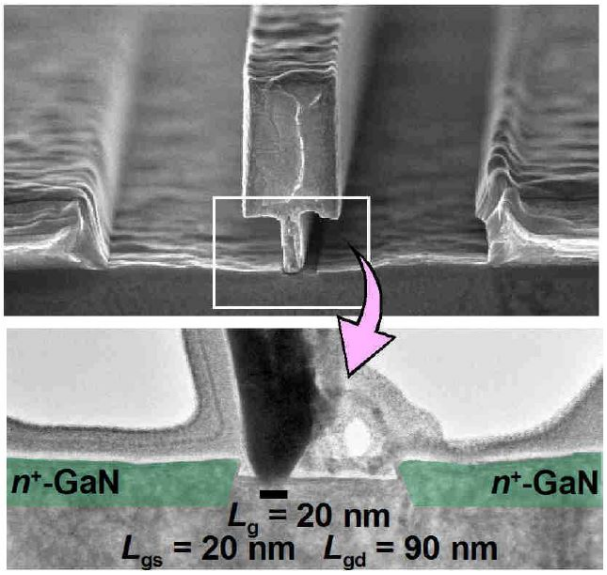


Figure 1.5: A SEM photograph of the T-gate used in Chapter 4. The transistors in this process exhibit $f_T > 300\,\text{GHz}$. Photograph: HRL Laboratories

The modeling of microwave transistors is an entire research topic on its own with associated theory and measurement techniques. Active and passive device simulation in a MMIC design

are two very different things. The predicted behavior of passive elements is generally accurate for MMIC designs because the entire network is eventually fully EM simulated, typically with a method-of-moments (MoM) technique. The predicted behavior of the transistor however is not simulated with a MoM technique, it is derived from S-parameters (small-signal behavior) or large-signal models that are capable of predicting the nonlinear relationship between input and output voltages and currents. It is useful, however, to know what models are commonly used in the design of MMICs, how those models are created and what can go wrong in the simulations using those models. The most important idea to keep in mind is that trusting a model to predict behavior outside of its validated operation range is very risky. Depending on the mode of operation of a PA, the fabricated device could oscillate, have greatly reduced power or efficiency or simply do nothing at all. For the designs in this work, Angelov or EEHEMT models were used.

The Angelov/Chalmers model exists in many forms and was published by Angelov in [31]. Several versions of it are named after individuals who contributed important improvements to the model such as Zirath, Rorsman and Angelov [32]. Because the work on the various forms of the model was performed at Chalmers University of Technology in Gothenburg, Sweden, the model is also called the Chalmers model. The model is known for being especially good at predicting the behavior of HEMTs, which at this point in time are the main device used in GaN MMICs. The current Angelov model has improved capacitance, breakdown, and noise modeling. It has a single-pole thermal circuit approximation to account for heating effects. The Chalmers/Angelov model is known to be particularly well suited for the modeling of GaN FETs.

The EEHMET model was developed by EEsof before being acquired by HP/Agilent/Keysight. The AC and DC behavior of the model is separated for simpler extraction. The temperature and self-heating effects are modeled through equations, not an electro-thermal approximation circuit. More information on this model is given in [33]. Other popular models are the Curtice model, the Root model, the Statz model and the Triquint-own-model (TOM) [13].

1.2 Introduction to Additive Manufacturing

This section describes some of the necessary background knowledge needed to further the understanding of the additive manufactured (AM) components discussed in the thesis. The AM components in this thesis are fabricated in two different ways:

Direct Metal Laser Sintering - is an additive manufacturing process that uses discrete metal particles in movable powder bed and a laser to form structures. The metal particles are deposited in a powder bed and the laser fuses the particles together with heat. A structure is built up layer by layer in the powder bed by an iterative process of fusing the metal particles, lowering the powder bed, and then sweeping a new layer of metal particles across the bed. A summary of the process is shown in Fig. 1.6. The layer thickness depends on the metal particle size and usually varies from 20 to 200 μm [34]. To fabricate structures with different surface finishes and feature sizes, the laser power and spot diameter can be varied for the particular component. More details about DMLS are given in chapter 6.

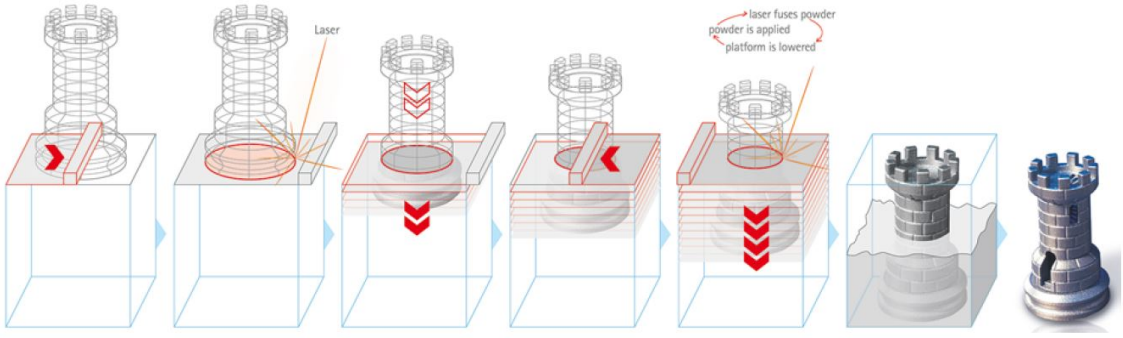


Figure 1.6: The DMLS process. The wire frame represents the design and the solid part is built up from individual layers of discrete metal particles fused together with a laser. Source: [2].

Sterolithography with Metal Coated Plastic - is an additive manufacturing process that uses a liquid, resin based photopolymer in a vat [34]. A UV-laser is used to initialize the photopolymerization process as the laser solidifies the liquid. Similar to DMLS, after the first layer is complete, the part is lowered into the vat and the next layer is fabricated. The layer thickness is determined

by the photopolymer density and in this work was 25 μm. The printed plastic part is then treated to allow for metal (Cu) plating. The chemical treatment is a proprietary process of the Swissto12 corporation [35]. Because the components are fabricated with a plastic skeleton, the parts are not as mechanically or thermally robust as solid metal counterparts [36].

1.3 Thesis Overview

The goal of this thesis is to explore non-conventional circuit designs using advanced GaN MMIC technologies, with a focus on increasing operating frequency and output power. To facilitate that goal, several MMIC designs with increasing operating frequency are performed and evaluated. The issues encountered with stability in wideband and very high-frequency designs are addressed with a new stability technique that is compared to established methods. Last, an investigation of packaging and thermal solutions is performed. A summary of the thesis chapters is given below:

- Chapter 2 - efficiency enhancement techniques for X-Band GaN MMIC PAs - discusses three different techniques for efficiency enhancement, output harmonic injection, a supply modulated Doherty power amplifier, and a Class-E amplifier in a 300 GHz f_T GaN-on-SiC process.

- Chapter 3 - analysis and design of a reverse-channel V-band VCO - discusses the design of a V-band VCO in a 90 nm GaN-on-SiC process that uses an integrated (on-chip) microstrip-to-waveguide transition and traditionally machined and AM split block waveguide housings. The active and passive technology, including the advanced 90-nm Γ-gate HEMT is summarized.

- Chapter 4 - analysis and design of 235 GHz GaN-on-SiC amplifiers - details the design of power combined multiple stage amplifiers in CPW. Active and passive technology needed to fabricate circuits at 235 GHz is summarized and measurements are made. A CPW-to-waveguide integrated transition is designed to eliminate parasitics from wirebonding and simplify future module integration.

- Chapter 5 - stability analysis in microwave circuits - presents a new way of analyzing stability in MMIC and microwave amplifier circuits. This chapter also contains a summary of modern stability analysis techniques and proof of concepts that validate the new technique.

- Chapter 6 - millimeter-wave component integration methods - contains a summary of results for W-band waveguide structures manufactured using currently available AM techniques. This chapter also contains a discussion on energy loss due to surface roughness effects. A FEM thermal analysis is performed and a AM heat pipe thermal solution is presented and experimentally validated.

Chapter 2

Efficiency-Enhancement Techniques for X-Band GaN MMIC PAs

Contents

2.1 Introduction

Modern spectrally-efficient communication signals, such as LTE-Advanced, use multiple sub-carriers resulting in high peak-to-average power ratios (PAPR) and large channel bandwidths [37]. Since the number of users, wireless devices and requested data rates will likely continue to grow,

new solutions in RF and digital hardware and communication protocols will continue to be researched and developed. The majority of current RF front end research is in investigating how to linearly amplify these spectrally-efficient signals in the low or sub-GHz range for the mobile handset, Internet-connected devices, and base station markets. The necessity of battery operation for handsets and wireless devices and overall efficiency for the base stations drives designers in these markets to maximize PA efficiency. The pressure of balancing the trade-offs between high efficiency, maximum output power, strict linearity, and bandwidth in the 350 billion dollar cellular market has led to new levels of performance utilizing ever more complex amplifier topologies [38], [39]. However, the efficiency enhancement techniques used in the low GHz range can also be applied to X-band amplifiers that are used as phased array unit cells, radar system amplifiers or as main amplifiers in the military and commercial SATCOM markets. This chapter investigates the application of three distinct efficiency-enhancement techniques: output harmonic injection, the Doherty power amplifier topology with supply modulation, and Class-E operation in a high f_T GaN-on-SiC process, all at X-band frequencies.

2.2 Output Harmonic Injection MMIC PA

The key challenge in microwave PA design is transmitting spectrally-efficient signals with large PAPRs efficiently while maintaining linearity, as highlighted in the introduction [40]. The commonly researched transmitter designs that address the linearity and efficiency constraints on PAs include Doherty, outphasing, and envelope tracking PAs [41]. This section presents a different approach which enables simultaneous high efficiency and linearity by active load modulation due to 2^{nd} $(2f_0)$ harmonic injection at the amplifier output. Because the $2f_0$ signal is generated separetely from the main amplifier and applied at the main amplifier's output, the technqiue is called output harmonic injection. Improved efficiency using this method has been demonstrated in hybrid amplifier topologies at 900 MHz and 2 GHz in [42]. An output harmonic injection amplifier system demonstrated simultaneous efficiency and linearity improvments at 2.45 GHz in [43]. The system block diagram of a simplified transmitter using a harmonically injected PA is shown in Fig. 2.1. In

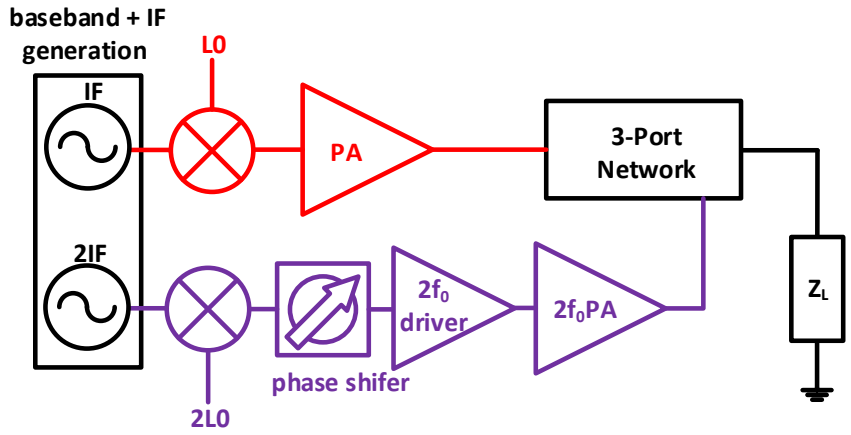


Figure 2.1: Block diagram of a HI power amplifier. The f_0 path is shown in red and the $2f_0$ path in purple.

this architecture, the IF signal is generated in digital baseband twice with one signal occupying twice the bandwidth at twice the IF. The IF and 2IF signals are then separately up-converted at the carrier and its second harmonic, with the possibility of generating the 2LO signal by frequency multiplication. For example, if the center frequency of the system is 10 GHz, then the IF and 2IF signals are centered around 1 GHz and 2 GHz respectively. Then, the LO and 2LO signals would be located at 9 and 18 GHz, resulting in 10 GHz and 20 GHz (upper side band) RF signals. The carrier-frequency amplifier is biased for Class-AB operation. The driver amplifier is biased in nearly Class-A because harmonic content generated by this amplifier is detrimental to the linearity of the system. The up-converted 2^{nd} harmonic signal is injected through a three-port diplexer network at the output of the carrier-frequency PA. The efficiency enhancement is achieved by $2f_0$ power injection into the main amplifier output (usually a FET drain), which shapes the current and voltage waveforms to minimize dissipation. The concept of optimizing the phase and amplitude of the $2f_0$ signal in order to increase the carrier PA efficiency was also shown in [44]. Because output harmonic injection shapes the output waveform without forcing the carrier-frequency PA to produce significant harmonic content, linearity is not only maintained but improved. The design and measurement of a 10-GHz harmonic injection PA is detailed in the remainder of this section.

2.2.1 Output Harmonic Injection MMIC PA Design

The design of an output harmonic injection amplifier consists of three components, the f_0 amplifier, the $2f_0$ amplifier and a three-port diplexer. An experimental version of the TriQuint 150 nm GaN-on-SiC process was used in this design. The process offers three metal interconnects (3MI), allowing air-bridges and plated lines that can handle 16 mA/μm current density. There are three different types of MIM capacitors, 240, 300 and 1200 pF/mm^2 as well as TaN and ohmic metal resistors. The layout view of the integrated amplifier system is shown in Fig. 2.2. In this design the carrier PA, a 12x100 μm GaN HEMT, is utilized and designed to operate in Class-AB at 10 GHz with 4 W of output power. Nonlinear load-pull simulations of the HEMT model were used to optimize output power, gain and efficiency. The optimal output impedance for maximum output power and small-signal gain in a Class-AB bias condition for the f_0 PA is found to be $Z_{opt} = 11 + j13\Omega$ and the matching network that presents this impedance at the drain port of the device is integrated into the three-port diplexer. The simulated impedances this circuit presents at the drain of the device at both fundamental and second harmonic frequencies are $Z(f_0) = 13.2 + j13.7\Omega$ and $Z(2f_0) = 19.2 + j15.6\Omega$. The output matching network with integrated diplexer is designed such that Z_{opt} is presented at both the fundamental and second harmonic frequency in order to maintain waveform symmetry. The three-port diplexer is designed in a non-50-Ω environment as a low-pass network (through path for f_0) in parallel with a high-pass network (injection path for $2f_0$), using microstrip lines and capacitors for minimal insertion loss and footprint. The simulated isolation between the through and injected paths is > 20 dB. The simulated insertion loss in the f_0 and $2f_0$ paths is 0.8 dB. DC-blocking capacitors are integrated within the lines at the device plane in both frequency paths along with a meandered section of line used for the RF choke. The simulated optimal power at the 2^{nd} harmonic required to achieve the maximum efficiency improvement at 1 dB compression is 10 dB below the fundamental output power, requiring that $P_{inj}(2f_0) > 26$ dBm. In order to achieve this power level at $2f_0$ and have a high efficiency PA in the injection circuit path, a 20 GHz driver PA is designed with a device periphery of 8x50 μm, achieving a maximum

output power of 29 dBm and $PAE > 50\%$. Shown in Fig. 2.3b are the two separate amplifiers and output matching network and diplexer. The $2f_0$ amplifier is fabricated as two separate amplifier stages, to later be cascaded.

2.2.2 Measurements and Discussion

The two PAs are measured separately using fixtures which interface the MMIC to coaxial connectors, shown in 2.3a and as presented in [45]. The 10 GHz carrier PA is measured without harmonic injection at a bias point of $V_{dd} = 20\,\text{V}$ and $I_{dq} = 70\,\text{mA}$ and the 20 GHz driver PA at a bias point of $V_{dd} = 15\,\text{V}$ and $I_{dq} = 20\,\text{mA}$. The output harmonic injection PA is then tested with 2^{nd} harmonic injection by optimizing the amplitude and phase of the injected $2f_0$ signal. The carrier PA is measured in Class-AB bias with a frequency sweep from 9.8 to 10.6 GHz without any harmonic injection.

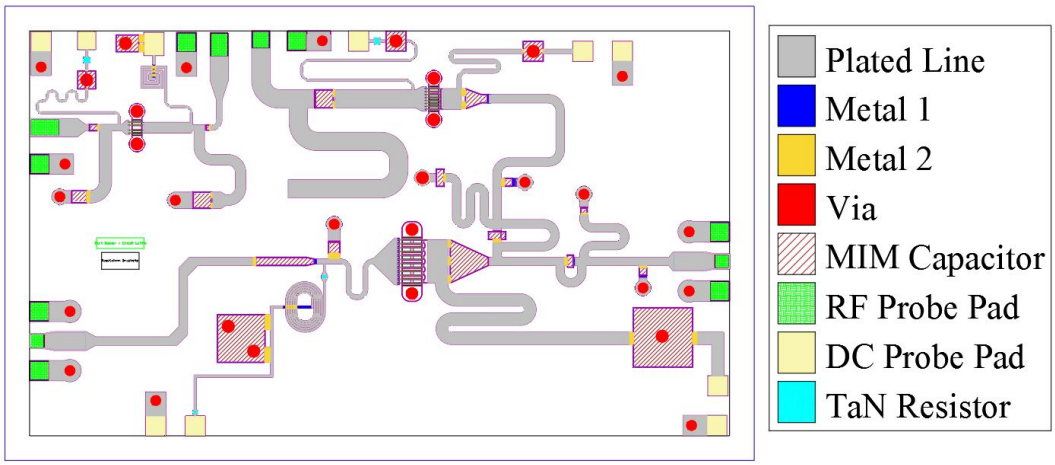
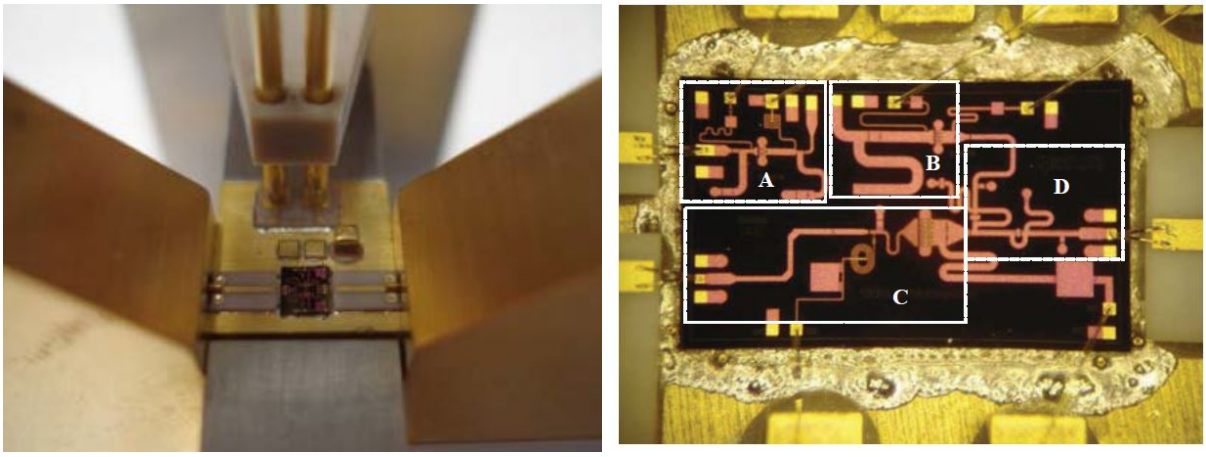


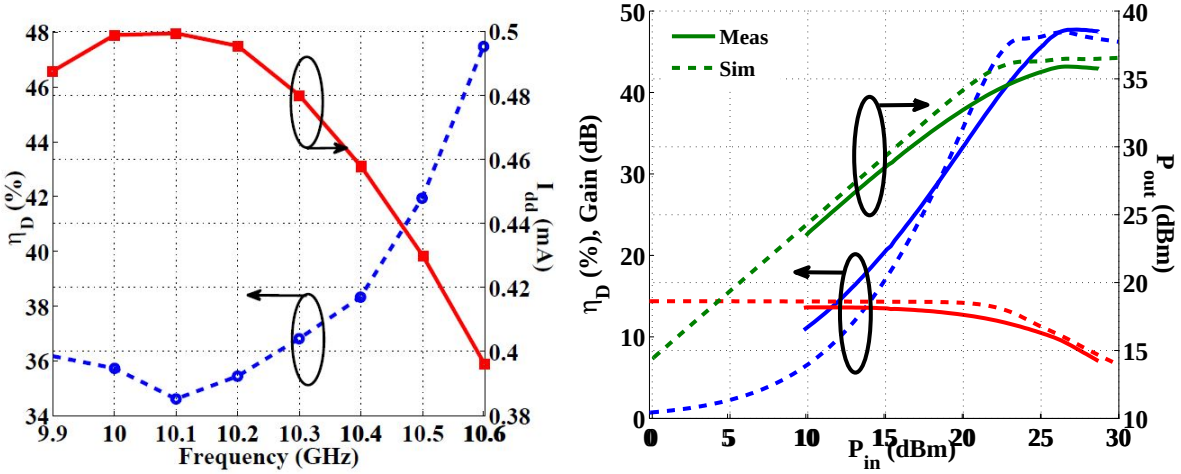
Figure 2.2: Layout of the harmonic injection amplifier. The legend shows metal layers, via, resistor, and capacitor locations, and DC and RF probe pads. Plated line refers to the combination of Metal 1 + Metal 2 to form a high current capacity transmission line.



(a) (b)

Figure 2.3: a) Fixture for RF and DC interface to MMIC. Spring-loaded pins (top) provide DC bias and supply and coaxial-to-microstrip transitions provide RF input and output b) the fabricated output harmonic injection PA with A and B highlighting the 2-stage $2f_0$ amplifier, C representing the main f_0 PA and D showing the output network with diplexer.

The measured results for drain current and drain efficiency at 1 dB compression show an upward frequency shift of 600 MHz (6 %) and are presented in Fig. 2.4a.



(a) (b)

Figure 2.4: (a) Measured drain efficiency (blue) and I_D (red) versus frequency. In (b) simulated (dashed) and measured (solid) η_D, gain, and P_{out} at 10.6 GHz.

At 10 GHz, the main PA without harmonic injection achieves a drain efficiency of 36 % with an output power of 36 dBm. However, the PA achieves a maximum efficiency of 48.5 % at $f_0 =$ 10.6 GHz with $P_{out} = 4W$ and a small signal gain of 14 dB which matches closely with the simulated results at 10 GHz. A comparison of the simulated vs. measured results for the f_0 PA is shown in Fig. 2.4b. The efficiency of the injection circuit plays a critical role in the calculation of the total efficiency of a harmonically injected PA (HI-PA) transmitter architecture. As shown in Fig. 2.1, the injection circuit consists of the up-conversion and phase adjustment circuit and a driver PA in order to create the magnitude and phase optimized $2f_0$ signal for injection into the main carrier PA. The total efficiency, η_{total} of the HI-PA can be calculated as:

$$\eta_{total} = \frac{P_{out}(f_0)}{P_{DC_1} + P_{DC_2} + P_{DC_{inj}}} \tag{2.1}$$

where P_{DC1} is the DC power dissipated in the carrier (f_0) PA, P_{DC2} is the DC power dissipated in the driver PA at $2f_0$, and P_{DCinj} is the DC power dissipated in the phase shifter and up-conversion mixer. If the $2f_0$ injection path has an efficiency, η_{inj}, and the driver $2f_0$ PA has a gain, G_2, then the output power from the injection circuit, $P_{in_{inj}}$, can be described as the ratio of injected power at the output of HI-PA, $P_{inj}(2f_0)$ and G_2. The DC power dissipated in both the driver up-conversion related components can then be expressed in terms of the total injected power, $P_{inj}(2f_0)$ as:

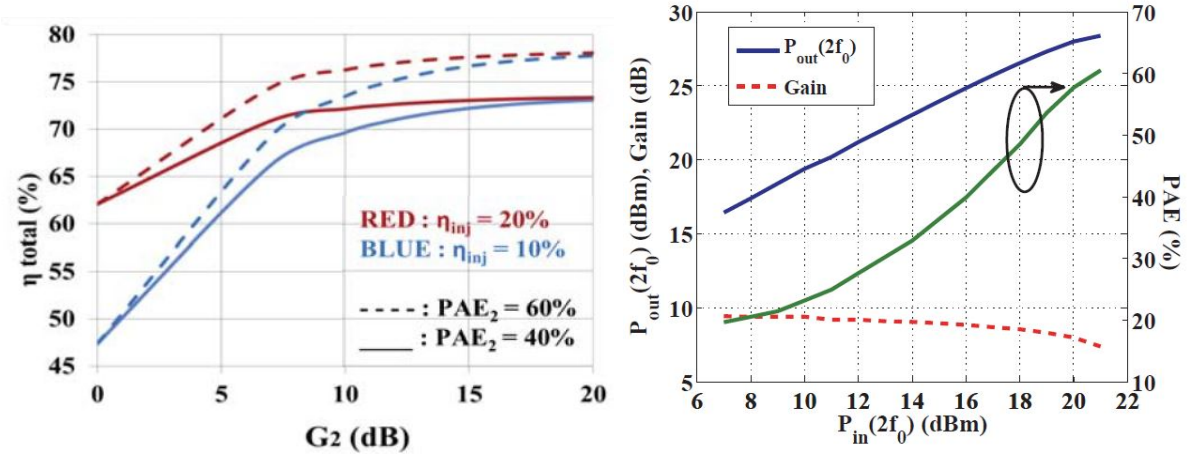
$$P_{DC_{inj}} = \frac{\frac{P_{inj}(2f_0)}{G_2}}{\eta_{inj}} \tag{2.2}$$

$$P_{DC_2} = \frac{P_{inj}(2f_0)(1 - \frac{1}{G_2})}{PAE_2} \tag{2.3}$$

where PAE_2 is the PAE of the driver PA at $2f_0$. Based on previous work presented in [6] and simulations of the X-band MMIC HI-PA presented here, it is assumed that the optimal $P_{inj}(2f_0)$ is 10 dB below $P_{out}(f_0)$ for maximizing the efficiency of HI-PA. Therefore, by substituting Eqn. 2.3 in Eqn. 2.1, η_{total} can now be expressed as:

$$\eta_{total} = \frac{1}{\frac{P_{DC1}}{P_{out}(f_0)} + \frac{(1-\frac{1}{G_2})}{10PAE_2} + \frac{1}{10G_2\eta_{inj}}} \tag{2.4}$$

It is shown in [43] that the efficiency of the injection circuit needs to be 40% or higher in order to significantly improve the total efficiency of the HI-PA at 1 dB compression. Since the injection circuit efficiency includes the up-conversion and phase adjustment circuit and the $2f_0$ driver PA efficiency, it is important to maximize efficiencies in both of these circuits. However, the impact of the up-conversion and phase adjustment circuit efficiency, η_{inj}, on η_{total} can be shown to be negligible if the driver PA at $2f_0$ has large enough gain. Therefore, it is important to design the driver PA at $2f_0$ to have maximum possible gain, G_2, and achieve $PAE_2 > 40\%$ when the HI-PA operates at 1 dB compression. Note that when the HI-PA operates in back-off, the optimal $P_{inj}(2f_0)$ also reduces even though it is 10 dB below $P_{out}(f_0)$. This results in the η_{total} being less sensitive to PAE_2 and η_{inj} in back-off. In Fig. 2.5a, η_{total} is plotted as a function of gain, G_2, of the $2f_0$ driver PA for several values of η_{inj} and PAE_2 assuming that the f_0 PA without harmonic injection has a maximum $\eta_D = 50\,\%$ [6].



(a) (b)

Figure 2.5: (a) Total calculated amplifier efficiency versus gain, G_2, for the 20 GHz driver amplifier for different η_{inj} and PAE_{2f_0}. (b) Measured gain, output power and PAE of the 20 GHz driver amplifier.

Practical values for the injection circuit efficiency, η_{inj} and PAE_2, when substituted in (3) show that as long as $G_2 > 6 - 7$ dB and the $PAE_2 > 40\%$, η_{total} increases by a minimum of 15 points.

Also, as seen in Fig. 2.5a, higher values of G_2 result in a minimal impact of η_{ltotal}. The $2f_0$ driver PA is designed for 20 GHz operation and measured with Class-AB bias with a maximum Pout = 27 dBm and $PAE = 59\,\%$ with a gain of 8 dB as shown in Fig. 2.5b. It is determined that the maximum $P_{inj}(2f_0)$ for optimal second harmonic injection at the output of HI-PA is 26.2 dBm. As seen from Fig. 2.5b, $PAE_2 > 50\,\%$ at this power level. The high efficiency of the 20-GHz PA reduces the degradation of overall efficiency due to other microwave component losses in the injection path. The designed X-band Class-AB PA is now measured with second harmonic injection at the output at $f_0 = 10$ and 10.6 GHz and $2f_0$ at 20 and 21.2 GHz, respectively. The total efficiency of the HI-PA is calculated from Eqn. 2.1 by taking into account the measured PAE_2 of the 20 GHz driver PA shown in Fig. 2.5b and the corresponding injected second harmonic power, $P_{inj}(2f_0)$. Note that the efficiency of the up-conversion and phase adjustment circuit is ignored due to test-bench setup and negligible impact on η_{total} from Fig. 2.5a. An input power sweep at f_0 from 12 to 27 dBm (linear to saturation) requires the optimal $2f_0$ injected power also to increase linearly from 17 to 27 dBm. For $f_0 = 10.6$ GHz, the total efficiency is calculated by assuming similar driver PA efficiencies at $2f_0 = 21.2$ GHz due to high process f_T [9]. In reality, this would mean a 2^{nd} MMIC run to correct the frequency shift. The HI-PA when tested at 10 and 10.6 GHz with 2^{nd} harmonic injection at an input drive level of 23 dBm (close to P1dB) results in a 15-point efficiency improvement along with a 60 mA reduction in the total drain current. At 1 dB compression, the maximum $P_{out}(f_0) = 35.79$ dBm with the drain current reduced from 0.49 A to 0.425 A at 10 GHz and 0.39 A to 0.33 A at 10.6 GHz. The injected $2f_0$ power required to achieve this 60 mA reduction in current is approximately 26.2 dBm. Therefore, the total efficiency of the main carrier PA is improved from 36% to 50% at 10 GHz and from 48% to 70% at 10.6 GHz by taking into account the $2f_0$ driver PA efficiency at the required $2f_0$ injection power as shown in Fig. 2.6. In order to design an efficient integrated HI-PA system on chip, a harmonic driver amplifier, as shown in Fig. 2.3b part A, and in the system block diagram, Fig. 2.1, is included to achieve high gain in the second harmonic injection path. Therefore, in a transmitter system, the circuit components of the up-conversion and phase adjustment circuit can operate in small-signal regime without affecting

the injection circuit efficiency. The 20 GHz harmonic driver is designed to have a gain of 17 dB using a 4x50 μm gate periphery. Therefore, a total gain of 25 dB can be obtained in the injection network path by taking into account the gains for the harmonic driver and main harmonic PAs at 20 GHz.

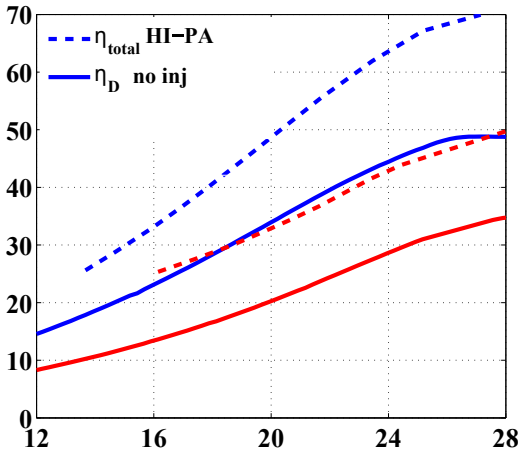


Figure 2.6: Calculated total η_D at 10 GHz (red) and 10.6 GHz (blue) with and without output harmonic injection (dashed and solid lines) based on measured f_0 and $2f_0$ PA data.

In summary, this section demonstrates a high-efficiency X-band MMIC HI-PA. The HI-PA with integrated injection circuit amplifier demonstrates a fundamental output power of 3.5 W at 10 and 10.6 GHz. The 20-GHz PA has a measured output of 27 dBm with 8 dB gain and $PAE =$ 59 %. The total efficiency of the HI-PA is increased from 36 to 50% at 10 GHz and 48 to 70% at 10.6 GHz by taking into account the injection PA efficiency and power at $2f_0$. These results represent a potentially new way of amplifying signals that is efficient, linear and simple to implement compared to traditional efficiency-enhancement techniques. The potential uses of this approach are widespread and contain any system that amplifies wireless signals and would benefit from increased efficiency. For the 2.45 GHz ISM band, a hybrid approach has already been demonstrated with supply modulation and the linearity was shown to be very good, [46], with greater than 30 dB improvements in IMD3 over the Class-AB operation of the main PA.

2.3 Doherty Power Amplifier MMIC PA with Supply Modulation

In this section an X-band Doherty power amplifier is measured and tested for use with supply modulation. The Doherty PA is fabricated using the TriQuint 0.15 μm GaN-on-SiC process. A K-Band Doherty PA is demonstrated in the same process with 25% PAE at 8 dB back-off in [47]. The main focus of this section is not to describe the design of the Doherty PA, which is already done in detail in [48], but to attempt to use a high-frequency MMIC Doherty PA in a supply modulation scheme for enhanced efficiency. Several other X-band efficiency-enhanced PAs have been demonstrated in the literature and are listed here for completeness, excluding other results from this chapter. In [49], a GaN MMIC PA combined with a supply modulator demonstrated a composite PAE=34.8%, G_{sat}=6.4 dB, and peak power of 36.5 dBm with a 18 MHz OFDM 11 dB PAPR signal. A similar result was achieved in the same MMIC process in [45]. An X-Band GaN envelope-tracking PA reported a 35.3% PAE and average output power of 1.096 W with a 60 MHz LTE-A, 6.6 dB PAPR modulated signal in [50]. Using GaAs technology, an X-band Doherty PA with 53% drain efficiency, 6.5 dB gain and 30 dBm output power with 6 dB power back-off is demonstrated in [51].

A summary of previous results and the current work is given below.

Table 2.1: Summary of X-band PA Performance

Topology	Max PAE (%)	P_{out} (dBm)	Gain (dB)	Ref
Supply-Modulated	59.9	41.14	20	[49]
Supply-Modulated	34.8	36.5	6.5	[45]
Envelope Tracking	35.3	37	7.6	[50]
Doherty	41	30	6.5	[51]
Doherty	47	36	9.2	This work

2.3.1 The Doherty PA

The conventional Doherty amplifier consists of two amplifiers in parallel as shown in Fig. 2.7a. The carrier amplifier (top), is biased such that it is always on and in Class-AB or Class-B mode.

The peaking amplifier (bottom), is biased in Class-C. The goal of the Doherty design is to select biases and a device periphery ratio such that the peaking amplifier is turned on when the carrier amplifier is saturating [52]. Load modulation between the carrier and peaking amplifiers assures that at higher power levels, the load of the carrier amplifier decreases, while that of the peaking amplifier increases, thus maintaining high efficiency over a large range of output power levels.

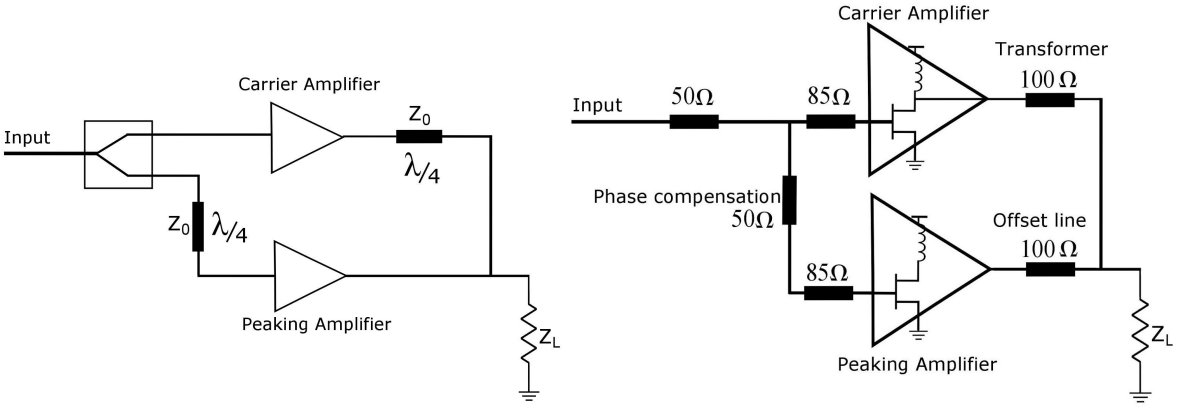


Figure 2.7: (a) Conventional topology of the Doherty power amplifier. (b) The Doherty architecture used in this work. The $\lambda/4$ transformer is replaced with a combined matching network and impedance transformer. The input is an unequal-power reactive divider that compensates the output phase offset.

2.3.2 X-band Doherty PA Design and Layout

The circuit in Fig. 2.7b is implemented as a MMIC and differs from the conventional Doherty architecture in Fig. 2.7a. The input divider is implemented without the typical coupler as detailed in [53]. The input divider network is an unequal power divider that changes the ratio of power delivered to each device as input power increases. This is due to the fact that the carrier and peaking amplifiers have drastically different changes in input capacitance (C_{in}) over input drive. The carrier amplifier C_{in} typically experiences a 10% increase while the peaking amplifier C_{in} experiences a 200% increase [53]. The increased C_{in} of the peaking amplifier reduces the load

impedance presented to the input divider network at the peaking amplifier port and therefore as input power increases, more power is directed to the peaking amplifier. This effect is desirable as the carrier amplifier is not overly saturated and kept in a high-efficiency region when input power is further increased. The output network does not employ a $\lambda/4$ impedance transformer but a matching circuit that transforms the dynamic load impedance seen by the carrier amplifier and simultaneously achieves optimal output power. The output transformer electrical length is compensated in the peaking amplifier input path by additional 50 Ω microstrip line. An image of the layout and fabricated MMIC is shown in Fig. 2.8 and Fig. 2.9

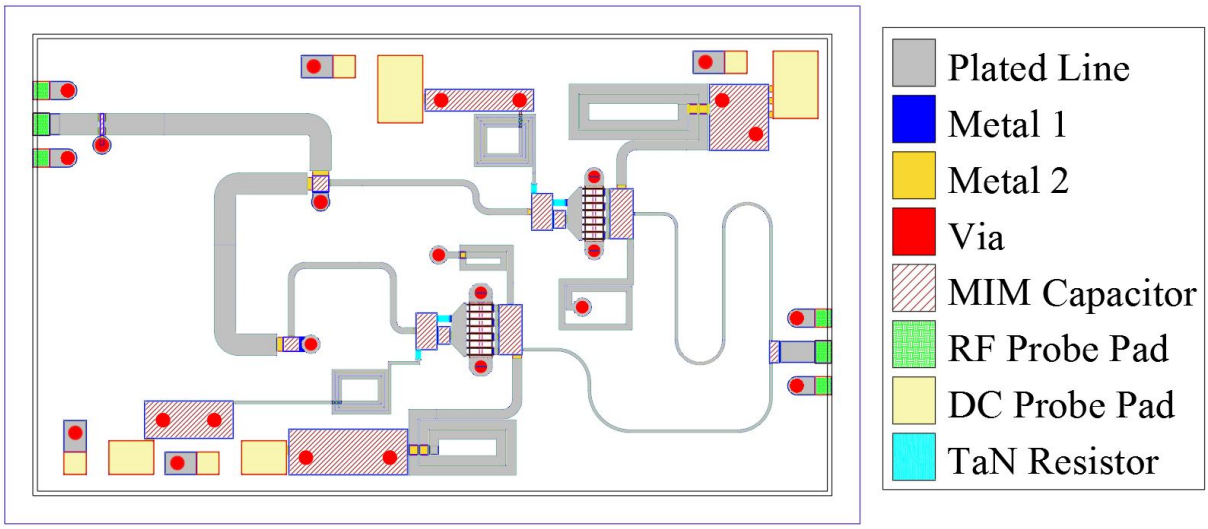


Figure 2.8: Layout of X-Band MMIC Doherty PA. Vias are visible in the capacitor-over-via bypass capacitors and in the ground pads for RF and DC probes. The legend shows important layers, similar to the HI-PA. The total die size is 3.8 mm x 2.3 mm.

The layout is performed using the same process development kit (PDK) as the output harmonic injection amplifier, with related design rules and an Angelov based nonlinear model. As shown in Fig. 2.8, each bypass capacitor is constructed as a capacitor over via. Substrate via dimensions are predefined for the specific substrate thickness and are circular with a 40 μm diameter. The input line is a 92 μm wide, 50 Ω microstrip connected to 50 μm pitch GSG CPW probe footprints at the input.

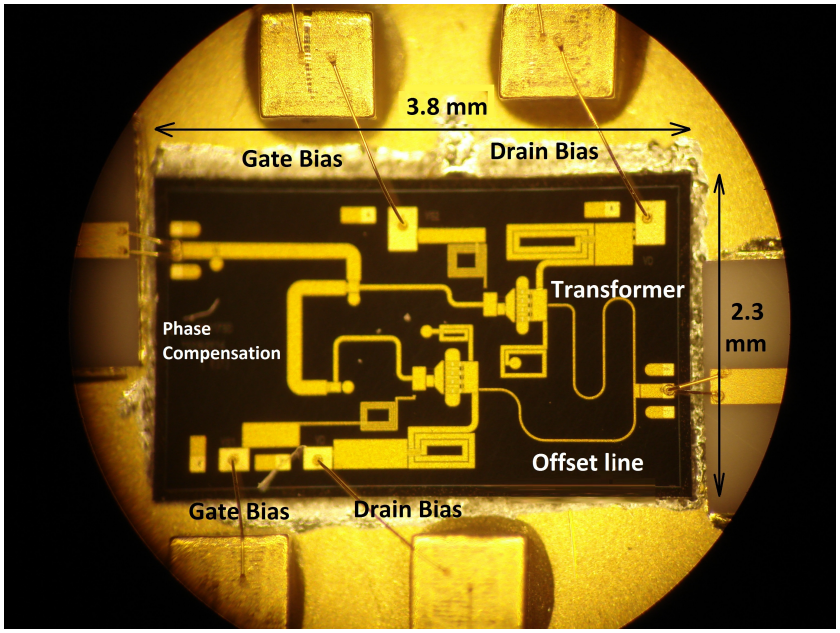


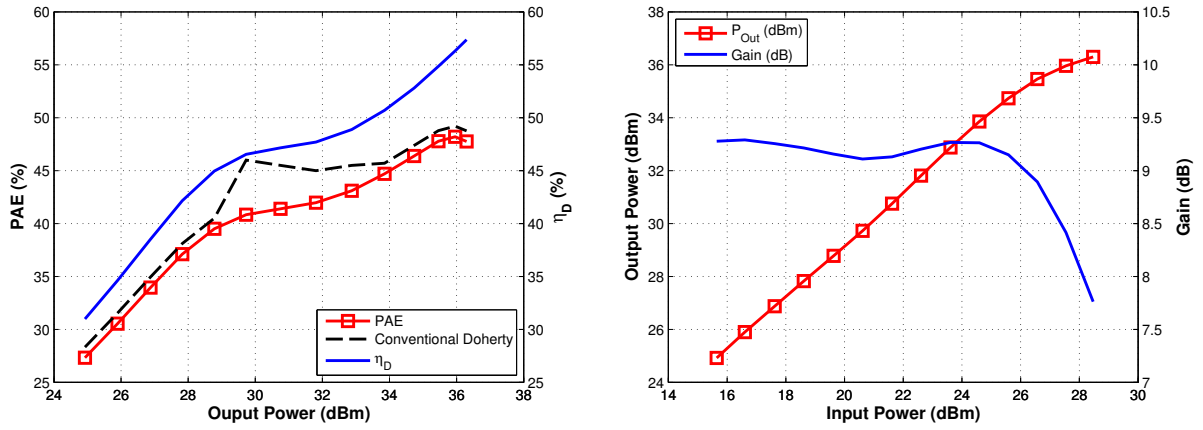
Figure 2.9: The MMIC DPA on a CuMo carrier with alumina microstrip interconnects as tested. 100 pF bypass capacitors are shown connected to drain and gate DC pads. The total die size is 3.8 mm x 2.3 mm.

This input line splits to the carrier and peaking amplifier and forms the unequal input divider. For the carrier amplifier path, the line is 25 μm wide and this corresponds to a 85 Ω line impedance. The carrier amplifier is designed to operate in moderate Class-AB mode and is biased at -2.7 V with a 20 V drain supply. The pinch-off voltage for these HEMT devices is near -4.0 V. After the expected output power and optimal load impedance was determined from nonlinear load-pull simulations, the output transformer and integrated supply and bias line network were designed. The drain supply is connected to the carrier amplifier with a 40 μm wide line as a planar inductor with a 23 pF capacitor-over-via bypass capacitor. The carrier amplifier device periphery is 8x80 μm. The carrier amplifier is connected to the amplifier output via a 100 Ω impedance transformer. Since this line needs to be such a high impedance, a 10 μm line width was implemented with multiple metal layers retaining the current handling capability of 160 mA. The DC drain current is never present on the output impedance transformer line as all drain current passes through the much wider 40 μm lines previously mentioned. Referring to Fig. 2.7b, the phase offset of the output impedance transformer

requires a phase compensation line on the input unequal power divider that is seen in the additional 50Ω line after the input power divider split. Inductance was added with planar inductors between the drain and ground vias for each device, to reduce the reactance and pre-match the devices to the transmission line transformers. A parallel RC was added to each gate to ensure stability.

2.3.3 Characterization with Supply Modulation

The die is mounted on a CuMo carrier and the pads are bonded to 50 Ω alumina lines. Probe station measurements are made with a drain supply of 20 V, a carrier gate bias of -2.7 V, and peaking gate bias of -5 V. The measured PAE of the Doherty is shown in Fig. 2.10a.



(a) (b)

Figure 2.10: (a) Measured drain efficiency (blue) and PAE (red) of the DPA versus output power at 10 GHz. The dashed line shows idealized Doherty PAE for a comparison. (b) Measured output power (red) and gain (blue) of the DPA versus input power at 10 GHz.

More than 41% PAE is obtained over 6 dB output power back-off. More than 30% PAE is obtained at 10 dB back-off at 10 GHz. Fig. 2.10b shows the measured output power and gain. The DPA provides a peak power of >36 dBm, peak PAE of 47% and peak gain of 9.2 dB. Part of the motivation for the original design of this PA was to determine if the output power back-off of a Doherty could be extended even further than conventional and state of the art designs. To further

investigate the use of supply modulation, the linearity of the fixed-supply Doherty was tested. In Fig. 2.11, the power spectral density of the DPA is shown for a 10 Mbps OQPSK signal at different output power levels.

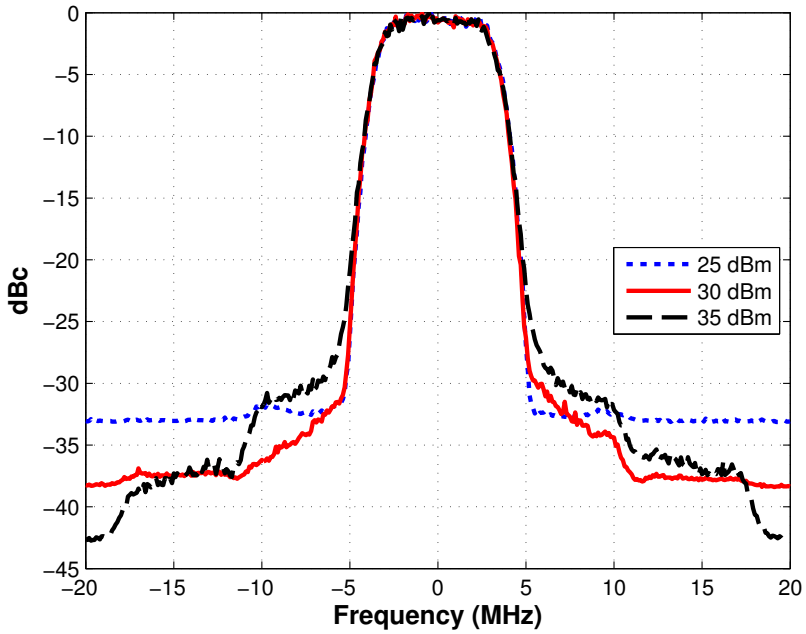


Figure 2.11: Adjacent channel power for the fixed-supply Doherty PA with various output powers. No DPD or predistortion was used.

The Adjacent Channel Power Ratio (ACPR) of the DPA with this 3.3-dB PAR signal is measured to be better than 30 dBc at an output power of 35 dBm and more than 33 dBc for 25 dBm of output power 10 MHz away from the carrier. The measured PAE vs. P_{out} characteristic in Fig. 2.10a does not exhibit the textbook Doherty behavior illustrated by the dashed line, where the carrier PA is fully saturated before the peaking amplifier turns on. In the design presented here, the saturation onset is soft which improves the linearity because of reduced clipping. Additional possible linearity improvement can be attributed to the harmonic cancellation from the two amplifiers using appropriate gate biases [54]. Because of the encouraging ACPR measurements, a stepped drain supply modulation experiment was performed [49]. The results of this experiment are shown in

Fig. 2.12.

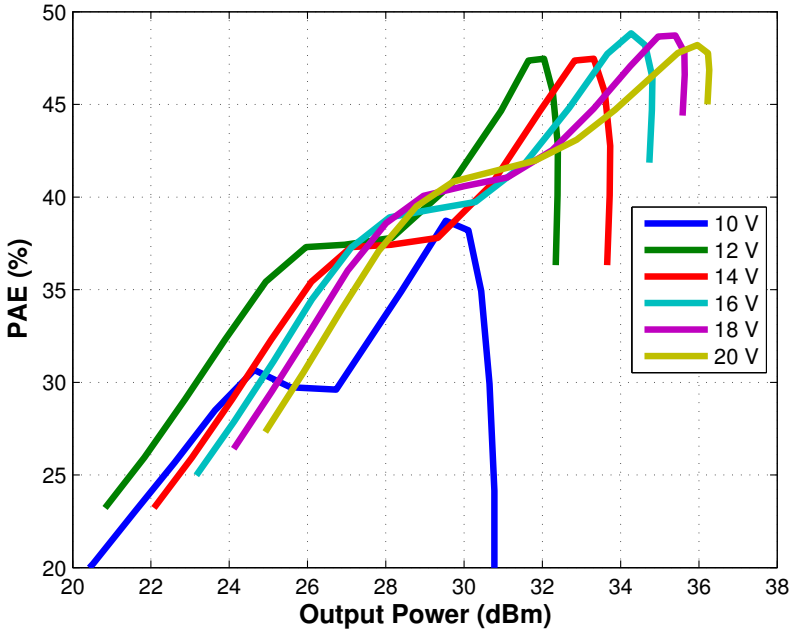


Figure 2.12: PAE and output power in a supply modulation experiment where both carrier and peaking PA were simultaneously modulated.

Moderate gains in PAE can be achieved by following the 20 – 12 V range trajectory. However, as the drain voltage drops below 10 V, the 20-V, fixed-supply Doherty PA maintains more efficient operation. The moderate gains of the 20 – 12 V range are also likely to be offset by the additional complexity and efficiency degradation due to a multi-level switched dynamic supply. In conclusion, this design presents a way to moderately enhance the efficiency of a Doherty PA with a limited range discrete step or continuous supply modulation scheme.

2.4 Class-E MMIC PA

This section demonstrates the analysis, design and measurement of a 10 GHz Class-E PA in a 300 GHz-f_T GaN-on-SiC process. More details on HRL's high-f_T process are given in chapter 4, where it is used for a PA design at 235 GHz. Relevant device details are given in this section as they pertain to Class-E operation. The Class-E amplifier was invented by Nathan and Alan Sokal in 1975 [55] but not immediately widely utilized. Part of the originally slow adoption of Class-E PAs in the microwave frequency range was device limitations and the fact that the Class-E was patented by its inventors in 1975 [56]. The device limitations are due to the need for many harmonics in a fast-rise time waveform. For transistors fabricated immediately after the introduction of the Class-E paper and patent, a typical photolioghrapically developed gate had a length of 1-2 μm and a resulting f_{max} of 45 GHz, and therefore a maximum number of two odd harmonics was typically possible for X-band amplifiers. [14,57]. To understand this and other limitations of device technology in Class-E design, it is necessary to introduce some background and theory.

An idea Class-E amplifier circuit is shown below in 2.13a. As shown, in the most basic form, the Class-E amplifier consists of a switch with associated switch capacitance, C_S (purple), a waveshaping output network, consisting of L and C in 2.13a (blue) and the load, R_L, that the amplifier delivers power to. The ideal Class-E amplifier is a resonant switched-mode circuit in which there are three important zeros: zero voltage and zero derivative of voltage at the switch terminals when turned on, and zero dissipated power from the product of switch voltage and switch current. These zero volt switching (ZVS) conditions all assume that the Class-E PA is operated at a 50% duty cycle, or D = 0.5. These conditions are summarized below:

$$v_s(0) = 0 \tag{2.5}$$

$$\left.\frac{dv_s}{dt}\right|_{DT} = 0 \tag{2.6}$$

$$D = 0.5 \tag{2.7}$$

Where T = 100 ps for a 10 GHz sinusoid. Enforcing these ZVS requirements results in the ideal

current and voltage waveforms described in [58] as:

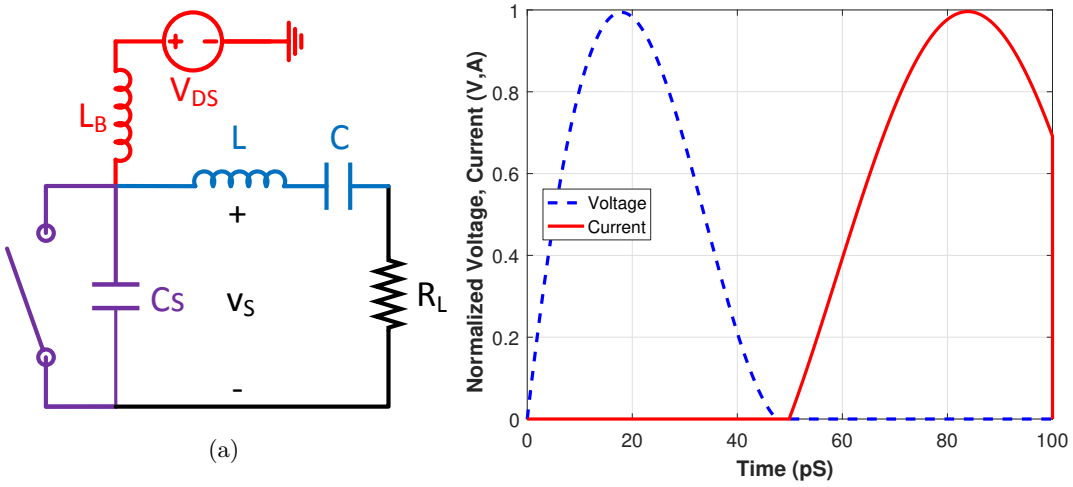
$$v_s(t) = \frac{I_{ds}}{\omega_s C_s}((\omega_s t) + a[cos((\omega_s t + \phi) - cos\phi)] \text{ for } 0 \leq (\omega_s t) \leq \pi \tag{2.8}$$

$$v_s(t) = 0 \text{ for } \pi \leq (\omega_s t) \leq 2\pi \tag{2.9}$$

$$i_s(t) = 0 \text{ for } 0 \leq (\omega_s t) \leq \pi \tag{2.10}$$

$$i_s(t) = I_{ds}(1 - a\, sin(\omega_s t + \phi)) \text{ for } \pi \leq (\omega_s t) \leq 2\pi \tag{2.11}$$

where I_{ds}, C_s and ϕ have been normalized for unity magnitude voltage and current, and a is the voltage or current amplitude. The ideal switch voltage and current waveforms are shown in Fig. 2.13b for $f_s = 10\,\text{GHz}$.



(a)

(b)

Figure 2.13: (a) The ideal Class-E amplifier circuit. (b) The switching waveforms for an ideal, $f_S = 10\,\text{GHz}$, Class-E amplifier.

It is shown in [58] that the analysis of Class-E operation relies on five assumptions which are inherently tied to the ZVS rules previously introduced. First, to repeat, is that the duty cycle of the

switch is 0.5 or 50%. Second, that the switch has zero ON-resistance and infinite OFF-resistance. Third, that C_S in Fig. 2.13a is only due to the device C_{DS} and is also linear. Next, that as a result of the previous assumptions, the circuit is lossless. Last, is that the output network of Fig. 2.13a has a high Q-factor and resonates slightly below the switching frequency, f_S, and therefore the voltage waveform at the load of the amplifier is purely sinusoidal. The use of these assumptions allows for a simplified analysis of the Class-E amplifier and the derivation of useful first-order approximation design equations. In [56, 58, 59] and others, the first-order design equations are derived from the switch capacitor voltage waveform and approximated commonly as:

$$V_{ds} \approx \frac{I_{max}}{56.5 C_s f} \tag{2.12}$$

$$f_{max} \approx \frac{I_{max}}{56.5 V_{ds} C_s} \tag{2.13}$$

$$Z_{net} \approx \frac{0.0446}{C_s f} e^{j49.05} \tag{2.14}$$

These equations are the starting point for a Class-E design. Examination of Eqns. 2.12 - 2.14 shows that the device I_{max} and C_s are needed. I_{max} is a manufacturer or foundry-provided parameter for MMIC processes and is usually specified in mA/mm and for this process is $85\,mA/mm$. The periphery of the device depends on the size of the selected unit cell and for this work is chosen to be 4x100 μm or 0.4 mm, allowing for an $I_{max} = 35$ mA. Determining the C_s for Class-E operation is not as straightforward. First, modern GaN devices are known to have a nonlinear C_{gs}, [60, 61]. Second, C_{gs} is an important part of the total device C_s for Class-E designs, [62,63]. The importance of the behavior of C_{gs} and its effect on C_s, are addressed in [64,65], where a method of determining the total capacitive reactance of the transistor is developed. This method uses the circuit shown below in Fig. 2.14. The procedure for determining the nonlinear C_s is as follows. First $V_{pinchoff}$ or V_p is determined from the IV curves. Next, V_{ds} is set to approximately $V_{max}/3.56$. The load, R_1 in Fig. 2.14, is set to R_{opt} for a Class-A amplifier as in [56]. Next, the input power of the harmonic-balance port is adjusted to ensure the device is presented with a sinusoidal input with magnitude ranging from V_p to V_{sat} and that I_{max} is not exceeded. This ensures maximum output power. Last, an inductor is added in parallel with the calculated R_{opt} load and adjusted to eliminate any

hysteric behavior in the dynamic load line. An example of the dynamic load line before and after the inductor tuning is shown in Figs. 2.15a and 2.15b.

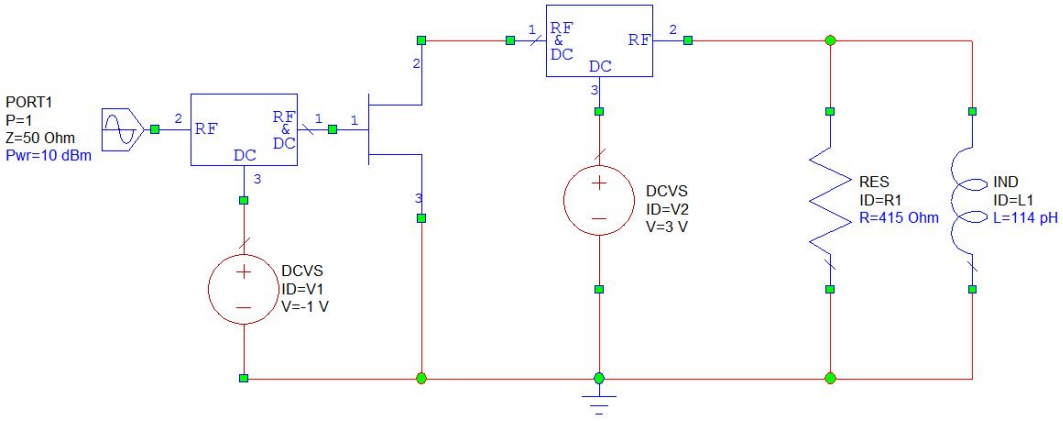
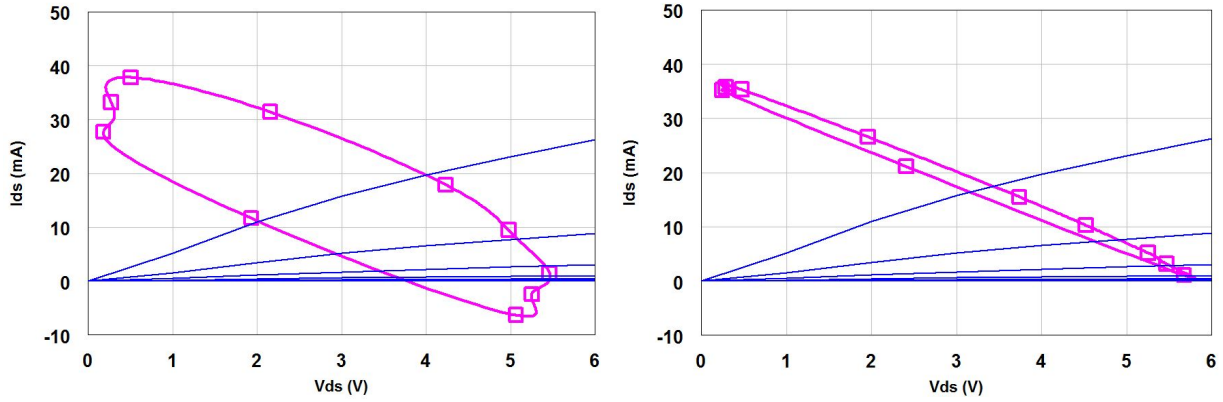


Figure 2.14: Simulation circuit for determining the nonlinear device capacitance C_s.



(a) (b)

Figure 2.15: Tuning the simulated dynamic load line of the Class-E amplifier. In (a) the dynamic load line without C_s cancelled, in (b) a inductance of 114 pH minimizes the hysteresis in the load line.

This inductor value, L, is used to calculate the device C_s as follows:

$$C_s = \frac{1}{w_0^2 L} \tag{2.15}$$

for the 4x100 μm device, the L was found to be $\approx$ 5 nH and the resulting C_s to be 50.66 fF. With

I_{max} and C_s determined, Eqns. 2.12 - 2.14 can now be used. From Eqn. 2.12, $V_{ds} = 1.22\,\text{V}$ however V_{knee} is approximately 1 V so this means that only a sub-optimal Class-E mode of operation will be possible. Similarly, $f_{max} \approx 10\,\text{GHz}$. This illustrates the trade-offs in a high-f_T process; the C_s in equation 2.13 should result in a very high f_{max} for Class-E operation but the inherently low I_{max}, $V_{breakdown}$ and a 1 V V_{knee} limits Class-E operation to approximately 10 GHz. Last, it is useful to calculate the Z_{net} as a starting point for the design of the output network. For the 4x100 μm device, $Z_{net} = 30.62 - j82.53\Omega$. Design of a network to present this impedance to the transistor for the Class-E design is presented in the next section.

2.4.1 Design and Layout of Class-E and Class-E Cascode MMIC PAs

The layout for the Class-E amplifier is shown in Fig. 2.16. Since Z_{net} was determined in the last section, it is used as a starting point for the matching network design. The design consists of a single 4x100 μm transistor and input and output matching networks. Shown in Fig. 2.17 and 2.18 are close-up views of the input and output networks. Their features are described below.

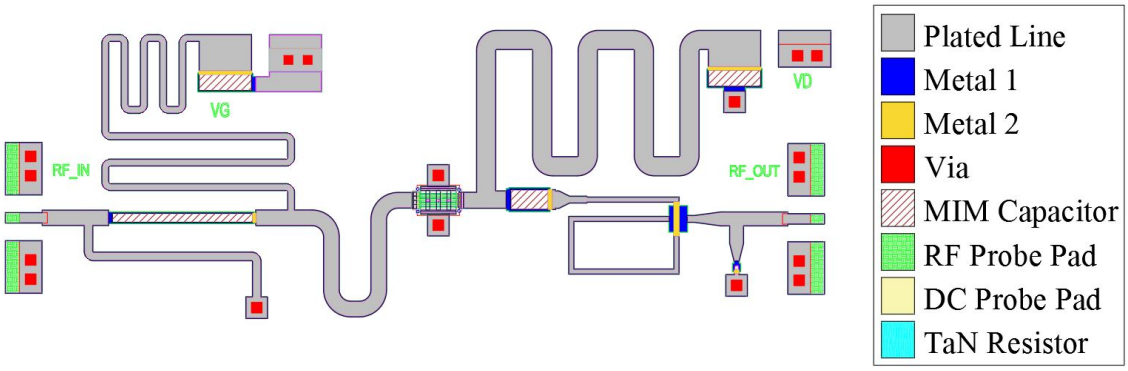


Figure 2.16: Layout View of the X-Band Class-E amplifier. The legend shows the relevant layers and passive components. The total die size is 2.335 mm x 0.807 mm.

The input matching network in Fig. 2.17 consists of a DC-blocking capacitor and a meandered line to the gate bias voltage, which separately are used as tuning elements and together form the bias tee. The total length of the meandered line is 2950 μm. The DC-blocking capacitor is 400 μm

in length and represents a capacitance of 3 pF. A shorted stub is also used as a tuning element and has length 625 μm. In red are the 30x30 μm square vias to the backside ground plane and in hatched green is the GSG RF probe pads. The primary purpose of the Class-E input network is to maximize amplifier gain but it is also important to pay attention to the return loss of the network as the transistor Z_{in} changes rapidly with input drive power.

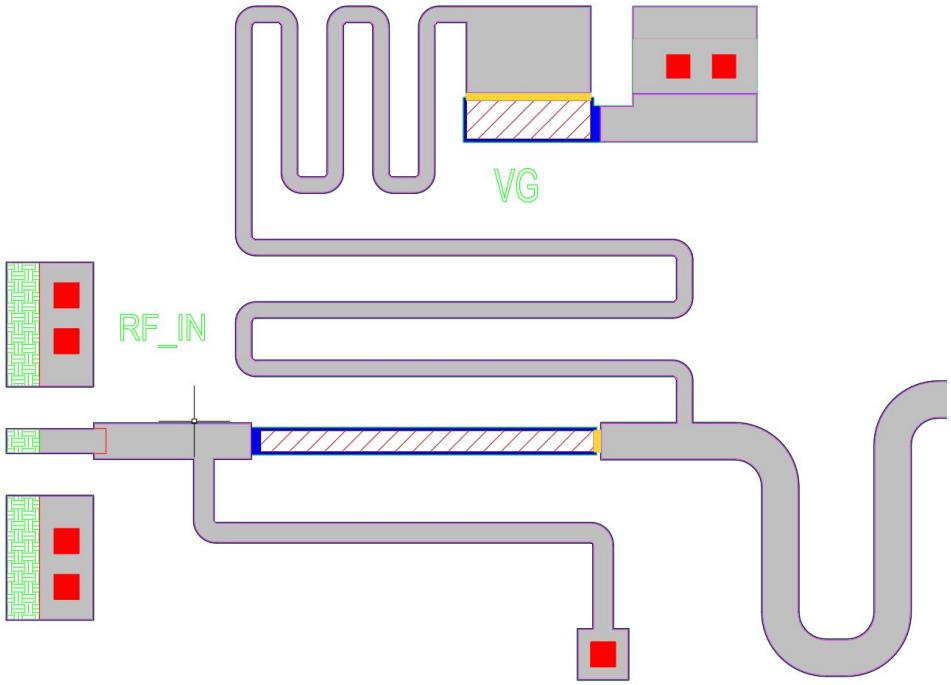


Figure 2.17: Input matching network layout view of the X-Band Class-E amplifier. The total size of the network is 1.15 mm x 0.807 mm.

On the output side, shown in Fig. 2.18, a DC-blocking capacitor and inductive path to the drain supply are again used as tuning elements and together form the bias tee. A simple series inductor and shunt capacitor form the waveshaping elements of the output network. Originally a microstrip stub matching approach was used for harmonic terminations, as in [59]. However, X-band MMICs present a unique trade-off between distributed and lumped elements, both work almost equally well at low-GHz frequencies. The use of a series L and shunt C turned out to be the lower loss implementation for this design. The series resonant circuit consisting of a large DC-blocking series

capacitor and the series inductor also present the necessary high impedance (ideally open circuits) to the higher-order harmonics required for Class-E operation.

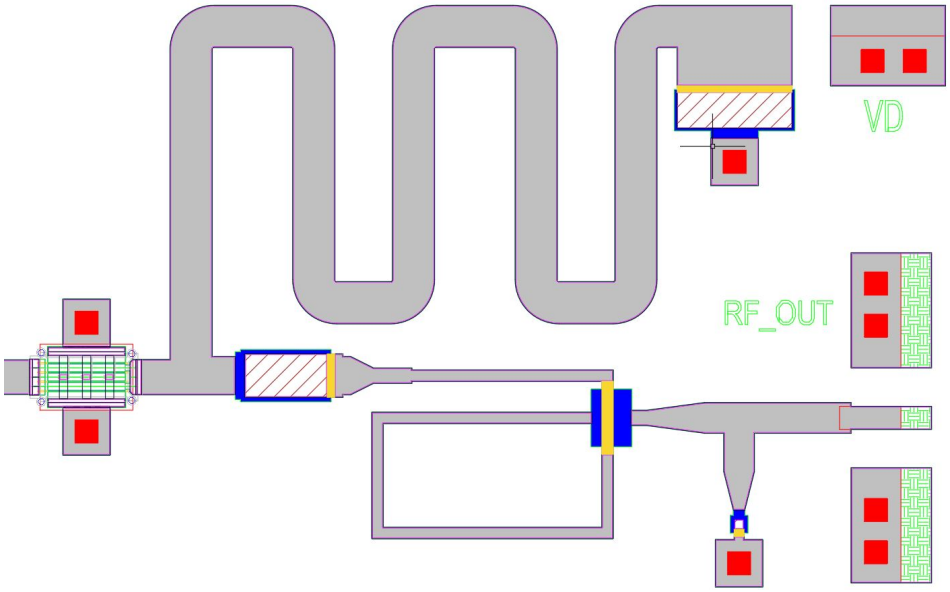


Figure 2.18: Layout view of the X-Band Class-E amplifier output matching network. The total size of the network is 1.02 mm x 0.807 mm.

The simulated output power, gain and PAE of the Class-E amplifier is shown in Fig. 2.19. Due to the low breakdown voltage of the high-f_T devices, an output power of 21 dBm is achieved. While the PAE peaks at over 60% for this design, it is very different from the 80-90% drain efficiencies sometimes typical of Class-E operation. An important parameter not discussed so far in the analysis of Class-E designs is the device static and dynamic R_{ON}. Taking R_{ON} into account for PAE is done by modeling the transistor in the ON state as a parallel RC network where the resistance R_s dominates the parallel response ($R_s \ll \frac{1}{\omega_s C_s}$) such that a the model reduces to a single resistor R_s. After re-solving the switch voltage boundary conditions in [58], an expression for the RF-DC efficiency is given as:

$$\eta_D = \frac{1 + (\frac{\pi}{2} + \omega_s C_s R_s)^2}{(1 + \frac{\pi^2}{4})(1 + \pi\omega_s C_s R_s)^2} \tag{2.16}$$

Since the ω_s, C_s, and η_D are known at this point in the design, it is useful to use 2.16 to obtain an

estimate of R_s. Rearranging 2.16 results in:

$$R_s = \frac{\sqrt{\eta_D(\pi^2+4)(\pi^4+4)-16}-\pi(\eta_D(\pi^2+4)-2)}{C_s\omega_s(\eta_D\pi^2(\pi^2+4)-4)} \tag{2.17}$$

which results in a $R_s = 35.83\,\Omega$. This R_s is very large and could be the result of a significant amount of current collapse in the experimental devices. Since dynamic R_{ON} is a difficult measurement and can vary greatly from static R_{ON} (IV curve calculation). An additional problem is that the optimal V_{ds} from Eqn. 2.12 is very close to the V_{knee} and this can also result in a low η_D and PAE.

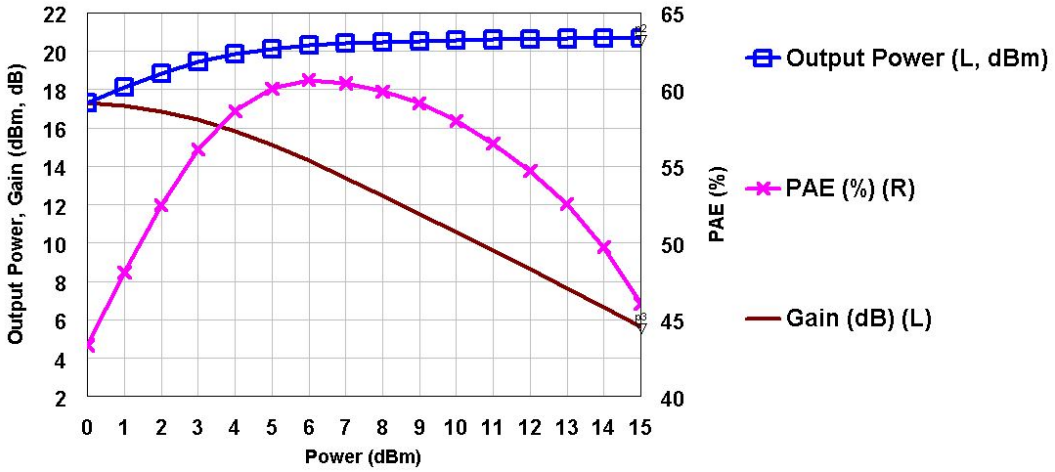


Figure 2.19: The simulated PAE (right), gain and output power (left) of the Class-E amplifier

2.4.2 Measurements and Comments

The fabricated Class-E amplifier is shown in a microphotograph in 2.20. The measured gain and efficiency is shown in Fig. 2.21a and Fig. 2.21b. Measurements made at different die locations on the wafer resulted in similar performance, indicating a high yield for these circuits and devices. Peak output power was 20.4 dBm at 9 GHz as can be seen in Fig. 2.21a. All measurements were performed with a 3 V V_d, however a 4 V V_d is also possible.

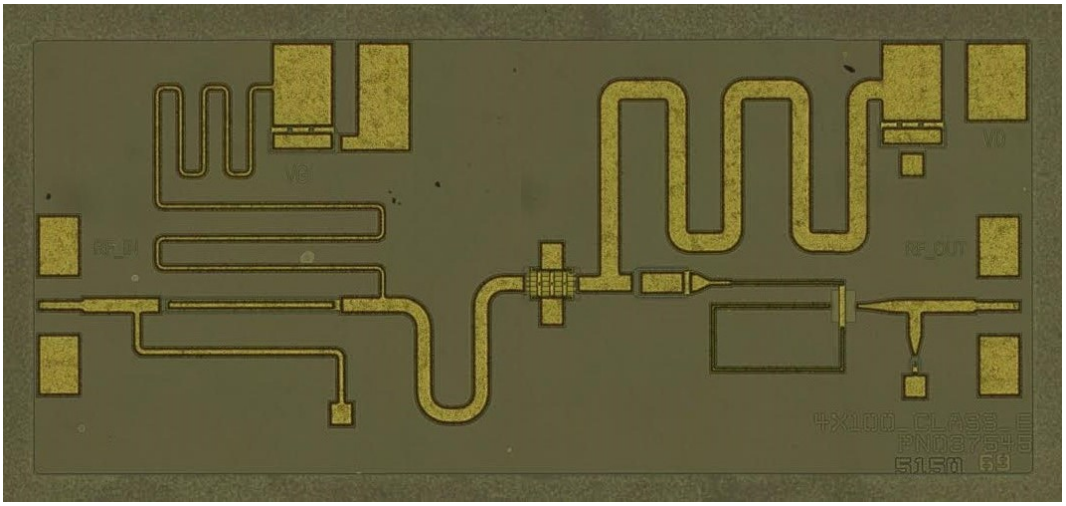
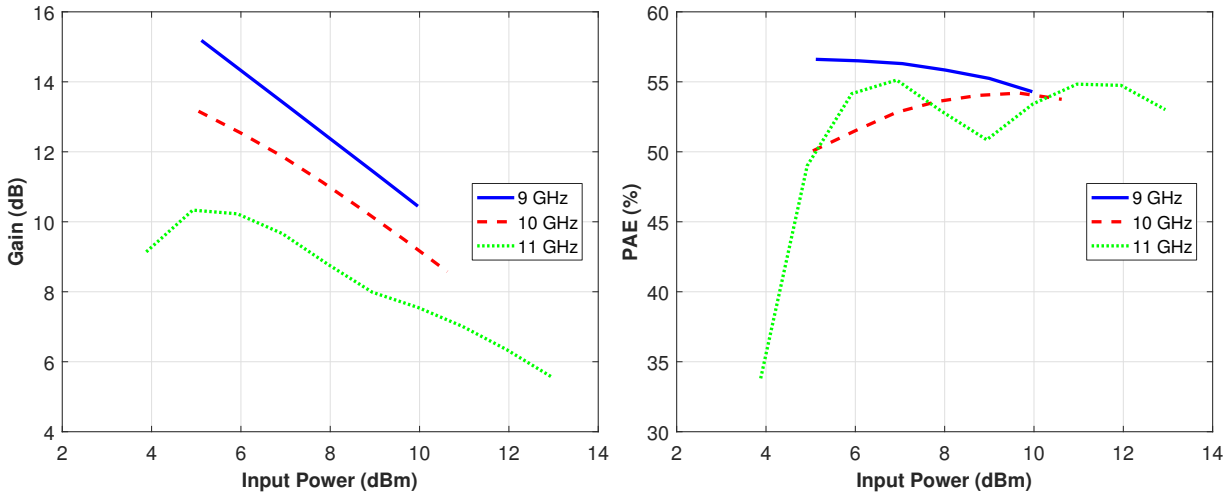


Figure 2.20: Microphotograph of X-Band Class-E amplifier. The total die size is 2.335 mm x 0.807 mm



(a) (b)

Figure 2.21: Class-E gain, output power and PAE measured from 9-11 GHz at $V_D = 3$V.

The peak output power of the Class-E amplifier with a 4 V supply was 22.8 dBm but efficiency and gain were degraded compared to the results from $V_d = 3$ V, shown below. While gain was higher than simulated for $V_d = 3$ V, the measurement setup was limited in input power so further testing was not possible. Overall, the results show sub-optimal Class-E operation, as predicted in the analysis and design sections.

2.5 Contributions from This Chapter

The specific contributions to the field from this chapter are as follows:

- Demonstrated a 4 W X-band output harmonic injection amplifier with measured efficiency improvement from 36 to 50%.
- Demonstrated X-band output harmonic injection amplifier with calculated efficiency improvement from 48 to 70% for separately measured fundamental and $2f_0$ amplifiers.
- Demonstrated a X-band GaN Doherty power amplifier with supply modulation that achieved a PAE of 41% and 31% for 6- and 10-dB backoff, respectively. This represents the highest efficiency for an X-band GaN Doherty PA in backoff.

Acknowledgment: This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

Disclaimer: The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

Chapter 3

Analysis and Design of a Reverse-Channel U-and V-band VCO

Contents

3.1 Millimeter-wave Voltage Controlled Oscillators

Interest in V-band (50-75 GHz) communication systems increased when the FCC approved the use of unlicensed wireless systems operating in the 57-64 GHz range in 1995 [66]. Part of the motivation for the unlicensed classification was that systems operating at 60 GHz have less range than lower frequency wireless systems for the same equivalent isotropically radiated power (EIRP) due to atmospheric attenuation. In 2013, the FCC modified the rules pertaining to 60 GHz operation to allow for higher output power to facilitate the use of the 57-64 GHz spectrum for high-capacity outdoor point-to-point communication systems. The IEEE 802.11ad standard outlines

the use of 60 GHz operation with a 2 GHz bandwidth and target data rate of 6.75 Gbps for indoor wideband local area networks, WLANs [3]. A summary of the current available spectrum allocation is shown in Fig. 3.1.

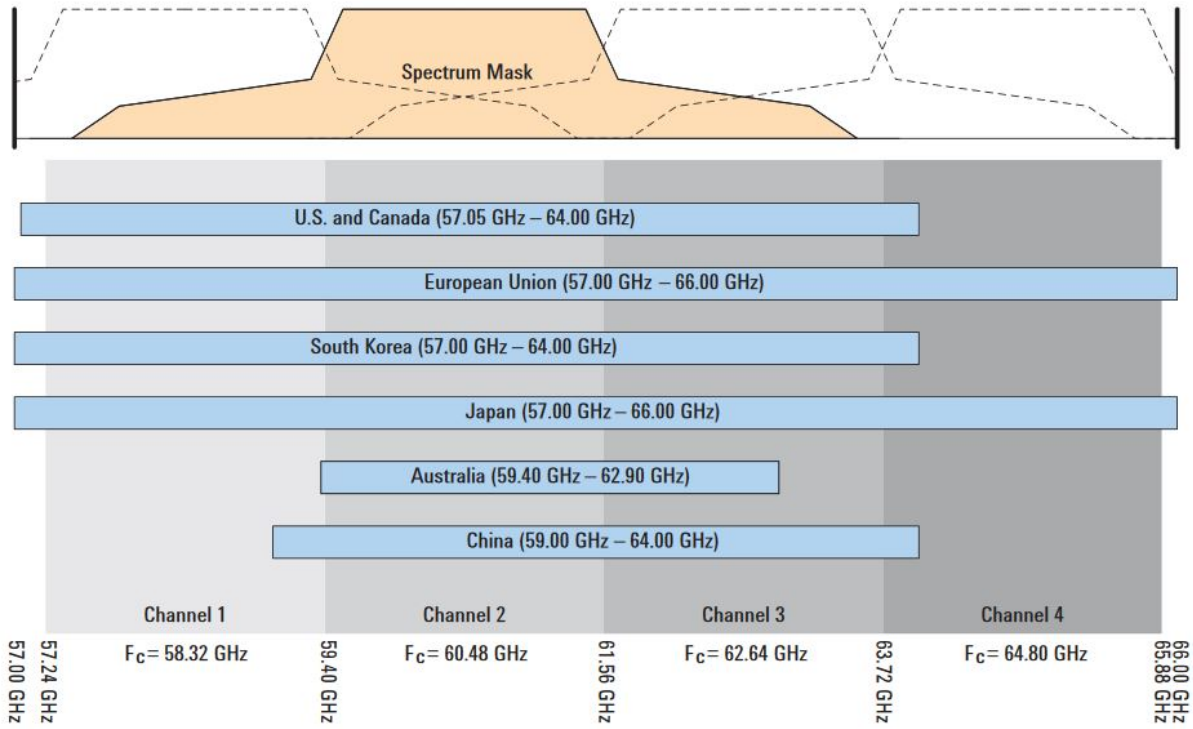


Figure 3.1: An overview of the unlicensed spectrum available in the 57-66 GHz range in each region where the standard is finalized. Source: [3]

One goal of the new 802.11 standards is to maintain backwards compatibility with 2.4 and 5 GHz radios while also allowing for all frequencies to be used in a single device (2.4, 5, and 60 GHz) [3]. An example might be general wireless use at 2.4 GHz, high performance local area use at 5 GHz and same-room wide bandwidth operation at 60 GHz. The combination of recent spectrum allocation and improved semiconductor operation at 60 GHz has created a wide range of interest in the technology. Potential applications for the technology are summarized below.

- Inter-satellite communications - On December 15th, 1995, Boeing's Milstar satellite constellation became the first satellite system to employ inter-satellite crosslink communication.

Milstar I and II were tactical and strategic multiservice satellite systems for survivable communications for US forces around the world [67]. The system used low (75-2400 bps) and medium (4.8-1544 kbps) data rates for voice, video and data communications and a 60 GHz system for crosslink communications [67]. The systems survivability depended on active and passive transmission security, including the ability to avoid signal jamming with antenna steering and variable system gain, the use of secure waveforms, and the ability to crosslink. The crosslink communication hardware consisted of autotracking modulators, narrow-beam antennas, and transmit and receive upconverters and downconverters operating at 60 GHz [68]. This equipment was state-of-the-art at the time and weighed approximately 800 lbs and used 260 watts.

- Wireless homes and offices - Several uses for high-bandwidth, short range wireless networks are found in the home or office where wired connections currently are used. These include: wireless displays, distribution of HDTV, file transfer and synchronization, and remote medical assistance. Some commercial uses of short range high-data rate communications are video tele-presence, automation control, police and security surveillance data transfer and public safety presence [3].

- Spaced-based internet communications - In March 2016, The Boeing Company filed a request to the FCC to allow for further increase in V-band radio output power and for a license to launch and operate 1,396 - 2,956 V-band satellites. The satellites would be positioned at 1,200 km in altitude in a non-geostationary orbit and provide internet service to residential, commercial and government clients [69]. Each satellites footprint would be divided into 8-11 km cells covering the US. In November 2016, five other companies, SpaceX, OneWeb, Telesat, O3b Networks, and Theia Holdings filed similar requests to the FCC [70]. All five companies have similar plans to field satellites that use transceivers in the unlicensed V-band frequency range to provide broadband internet in the US. The number of potential satellites and scope of the proposals is impressive, SpaceX's proposal

suggested 7,518 V-band low-Earth orbit satellites (referred to as VLEOs) and in-house designed and manufactured ground station terminals [71]. The other companies proposed smaller constellations of various configurations.

The ability to utilize the newly allocated spectrum in the V-band range for these applications relies on several high performance millimeter-wave components but starts with V-band LO generation or high-order frequency multipliers. Because multistage frequency multipliers in general have low efficiencies, a direct LO generation method is studied. To explore the potential of GaN-on-SiC technology for direct generation of U-band (40-60 GHz) and V-band LOs, Qorvo's 90 nm process is used and described in the next section.

3.2 Qorvo's 90-nm GaN-on-SiC process

This section details the passive and active technology that allows for V-band and higher operation in Qorvo's 90 nm GaN process.

3.2.1 Passive Technology

The passive technology used in this process is similar to the three metal layer interconnect (3MI) process used for the X-band harmonic injection and Doherty power amplifiers in chapter 2 but uses a thinner SiC substrate, 50 μm vs 100 μm, for higher frequency operation. For SiC MMIC substrates, 50 Ω microstrip has the useful characteristic that line width W $\approx$ substrate height H. To ensure a single mode in microstrip, W and H are made smaller than $\lambda/4$. For $f_0 = 75$ GHz and $\epsilon_r = 10$ for SiC, $\lambda/4 = 374\,\mu$m which is much larger than either 50 or 100 μm. The process has three metal interconnects to route RF signals and DC bias and supply. The thickness of the metal layers varies from 0.77 μm to 4 μm. The capacitors and resistors available are the same as in the 100 μm substrate process and include 240, 300 and 1200 pF/mm^2 density capacitors and 50 Ω/sq TaN and 0.34 Ω/sq ohmic metal resistors. A very useful feature carried over from the 100 μm substrate process is capacitor-over-via which allows for compact shunt capacitors to ground. In the

50 μm substrate, the through-hole-vias are square or slotted and 50 μm long per side. Similarly to the 100 μm substrate, the 50 μm process has a 0.25 μm SiN passivation layer. The main advantage of the similarities between the 50 and 100 μm substrate passives is that the high-performance and high-yield of the components is already proven and the PDK models are accurate.

3.2.2 Active Technology

The active device technology, coupled with the low-loss and high-power performance 3MI process, is what allows for $>$ 60 GHz operation with GaN devices in this technology. The high frequency operation of the HEMT devices is made possible by the use of a modified T-gate called a gamma-gate. A SEM photograph of the gamma-gate is shown in Figs. 3.2.

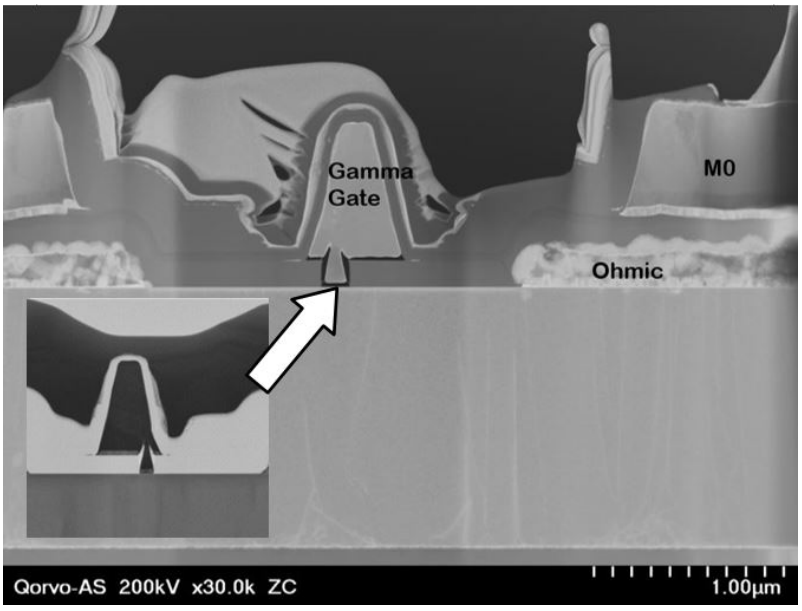


Figure 3.2: Gamma-gate SEM photograph. The source connection is on the right and the drain is on the left, the S-D separation is 2 μm. Photograph: Qorvo

Gamma-gate technology allows for higher-f_T, f_{max} and output power compared to GaN HEMTs with field plates [72]. Because the gain and efficiency of the field plated and gamma-gate devices are similar, the main benefit of the gamma-gate is higher frequency operation. Higher frequency

operation in gamma-gate devices is due to the absence of a dielectric passivation layer between the gate foot and head, resulting in lower parasitic gate capacitances [72]. In this design a gamma-gate transistor of gate width 90 nm was used with a 4x40 μm device periphery. The devices were characterized at V_d = 16, 18 and 20 V and with 40 - 180 mA/mm current densities. The PDK EEHEMT model was compared to measurements taken from 0.5 - 110 GHz and showed good agreement, meaning the models were accurate for design. Peak PAE of the 4x40 μm device at 35 GHz is near 40 %. The optimal power and efficiency match result in a drain impedance of 34-50 Ω/mm + j0.29-0.3 pF/mm, which is useful for matching with microstrip transmission lines that typically have 10 - 90 Ω impedances. The f_T of the devices was estimated to be 72 GHz at V_d = 18 V, and the power density to be 3.4 W/mm. The breakdown voltage of the devices is near 60 V. The high frequency operation of the active devices allows for V-band oscillation as well as amplification as described in the remainder of this chapter.

3.3 Reverse-Channel Operation

There are many possible configurations and layouts for FET-based oscillators. A good summary of commonly used configurations, mainly common amplifier schemes with external series or parallel feedback is given in [73]. To reduce the footprint and therefore production cost, as well as improve the phase noise of the FET-based oscillator, a reverse channel configuration is investigated. The block diagram of a reverse channel oscillator is shown in Fig. 3.3. The reverse channel oscillator in Fig. 3.3 has a simple circuit structure and layout, and the potential for lower phase noise near the carrier and better frequency tuning in a VCO application [74].

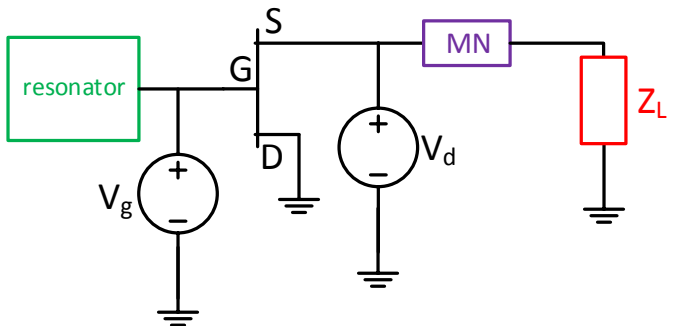


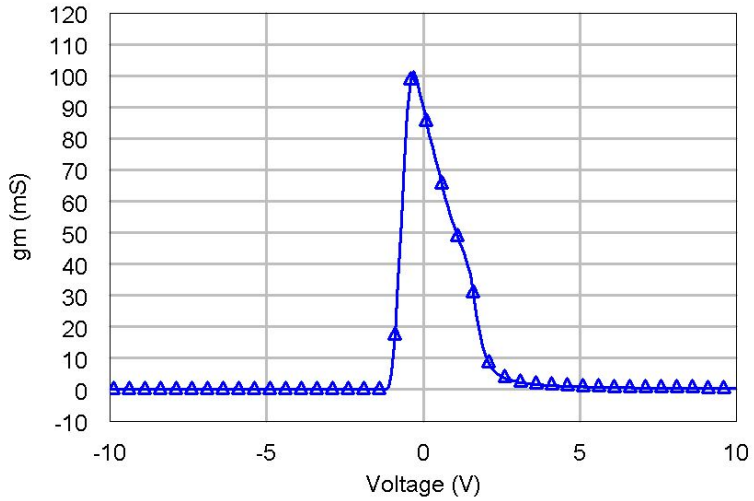
Figure 3.3: The reverse channel oscillator circuit schematic. DC gate bias and drain supply paths are not shown.

The idea behind a reverse channel oscillator is that the FET or HEMT drain is supplied with a negative voltage, making it the electrical source. The FET in this configuration is now a non-inverting amplifier, making the source inductance regenerative (positive feedback) rather than degenerative (negative feedback) [75]. The necessary feedback for the oscillator is now internal to the transistor as C_{gd} is increased in this configuration and acts as the feedback path [76]. Because the non-linear model is not verified in the III quadrant of the IV plane, the actual bias and supply voltages as well as the tuning voltage for the reverse channel oscillator resonator (a microstrip stub and additional transistor) will be optimized after fabrication. The symmetry of the HEMT model should also allow for accurate simulation of behavior in the III quadrant.

3.4 Design and Layout

The VCO design process is a combination of linear and nonlinear simulations with the foundry transistor and microstrip transmission line models. A similar process is detailed in [76] and [16]. Because the 90 nm process is not yet developed at the time of writing of this thesis, only two transistor geometries were verified with IV characteristics and the 4x40 μm device was chosen instead of the 6x40 μm device for higher-f_T operation. The first step is to determine what bias conditions for the device obtain peak g_m in the reverse channel configuration. This step is first and necessary because the oscillator will produce more output power when operating in the peak g_m

region. This is inherently a nonlinear simulation due to the large changes in the operation of the transistor as the gate voltage changes. The plot of the derivative of $\frac{i_{ds}}{v_{gs}}$, for different gate voltages is shown in Fig. 3.4 and shows a peak g_m at V_g = -0.3 V. A similar procedure is used to determine the V_d and it was found to be V_d = -2 V. The non-linear model then has the drain voltage V_d = -2 V and V_g = -0.3 V set and resulting S-parameters are used to avoid harmonic balance (large signal) simulations in subsequent steps.



(a)

V_d (V)	g_m (mS)
-10	85.74
-8	88.9
-6	92.18
-4	95.76
-2	100.7
0	0
2	100.7

(b)

Figure 3.4: a) Reverse channel $\frac{\mathrm{d}i_{ds}}{\mathrm{d}v_{gs}}$ for varying V_g. The peak is at -0.3 V. b) The range of g_m for different drain voltages showing peak transconductance at -2 V.

The next step is to determine where the transistor is unstable in the reverse channel configuration. By calculating the K-factor for the resulting S-parameters from the non-linear model biased at V_g = -0.3 V and V_d = -2 V, the range of potentially unstable operation is determined by use of K-factor and B_1 defined as:

$$K = \frac{1 - (|S_{11}|)^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.1}$$

$$B_1 = 1 + (|S_{11}|)^2 - |S_{22}|^2 - |\Delta|^2 \tag{3.2}$$

where the circuit is unconditionally stable if $K > 1$ and $B_1 > 0$. The calculated K-factor and B_1

are shown in Fig. 3.5 and show the device is unstable from 1 to 174 GHz, indicating that V-band operation is suitable.

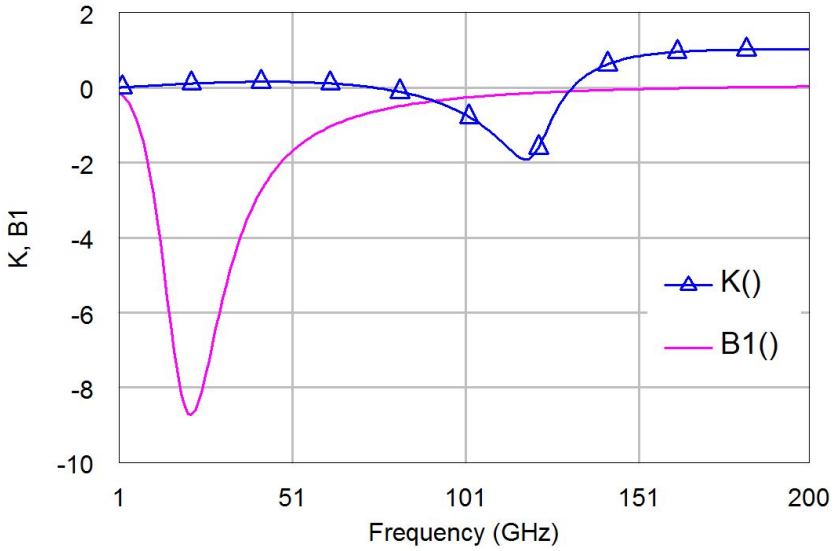
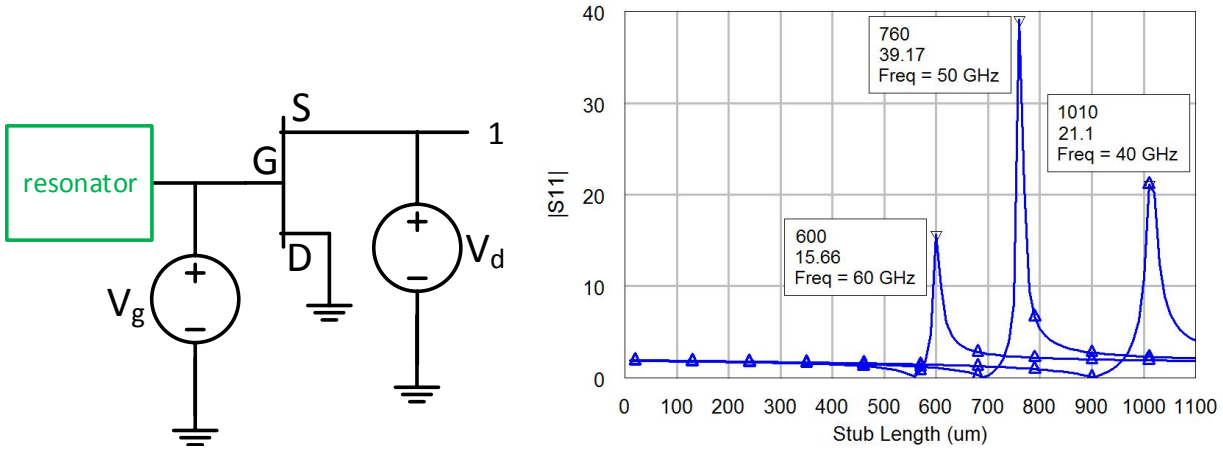


Figure 3.5: Range of potentially unstable operation for the reverse channel device. The K-factor is shown in blue and the B_1 factor in pink. The device is potentially unstable until 174 GHz but was modeled from 0.5 to 110 GHz.

An open-circuit microstrip stub resonator, is connected at the gate of the reverse channel device and tuned for maximum reflection coefficient at the drain terminal. Because this is a VCO design instead of a high-Q fixed frequency resonator, this step allows the designer to see what range of frequencies the VCO will produce. Shown in Fig. 3.6b is the resulting $|S_{11}|$ for various stub lengths, where $|S_{11}|$ refers to port 1 at the drain of the transistor. The stub lengths decrease with frequency according to the electrical length. The challenge in the design of this VCO is to provide a tuning range that can cover all of the values shown in Fig. 3.6b.



(a) (b)

Figure 3.6: (a) The oscillator with port 1 referenced. (b) Small-signal simulated $|S_{11}|$ for various gate resonator stub lengths. The 1.01 mm stub corresponds to an oscillation frequency at 40 GHz and the 600 μm stub corresponds to an output frequency at 60 GHz. The second number in the markers shows the magnitude of S_{11}, which is > 1 for all frequencies.

The final step in the oscillator design is to take the results from the previous linear simulations and perform a non-linear load pull simulation on the EEHEMT model to determine the impedance to present to the drain for maximum output power. This is done for 40, 50 and 60 GHz operation and the optimal reflection coefficient is found to be $0.7 \angle 150\,^{\circ}$ at all frequencies. So far, the simulations have all used a fixed length microstrip line model as the resonator at the gate of the oscillator transistor. To be able to tune the oscillator output frequency, a second transistor is connected to a short length of microstrip line to act as a variable length stub, as shown schematically in Fig. 3.16b. The resonator transistor source is connected to ground so the stub becomes a short circuit instead of an open. To check that the tuning range of the variable short circuit stub is wide enough to produce 40-60 GHz output frequencies, a comparison is made with each fixed length stub. The results of this comparison are shown in Figs. 3.7 - 3.9 for 40, 50 and 60 GHz. The variable stub has a similar reactance as the fixed length microstrip line model but more resistance, bringing the load contour closer to the center of the Smith chart.

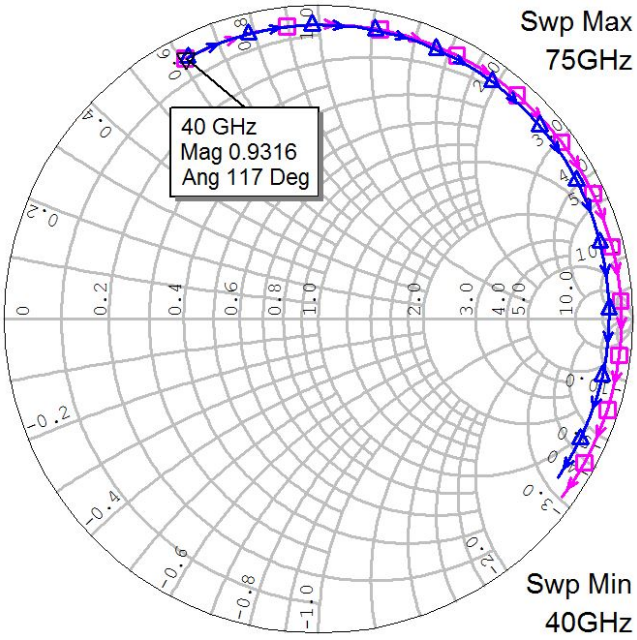


Figure 3.7: The simulated reflection coefficients for the 1.01 mm fixed length stub in pink and the tunable short circuit stub in blue with Vg = -1.5 V.

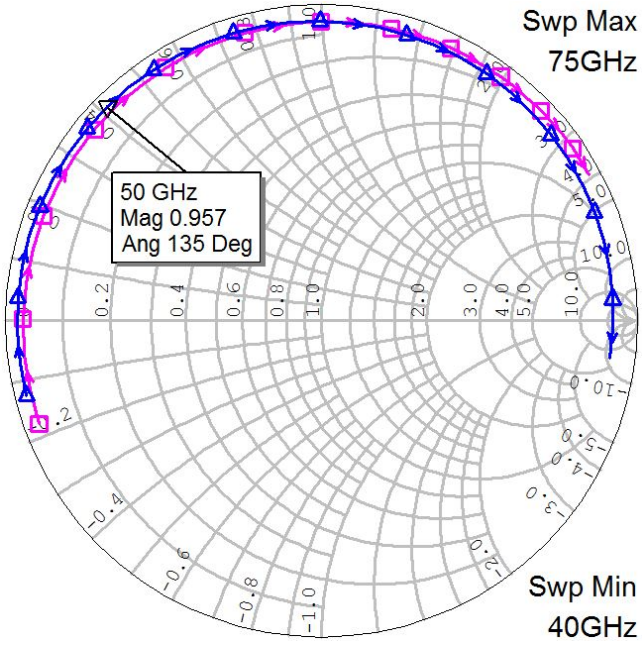


Figure 3.8: The simulated reflection coefficient for the 760 μm fixed length stub in pink and the tunable short circuit stub in blue with Vg = -5.3 V.

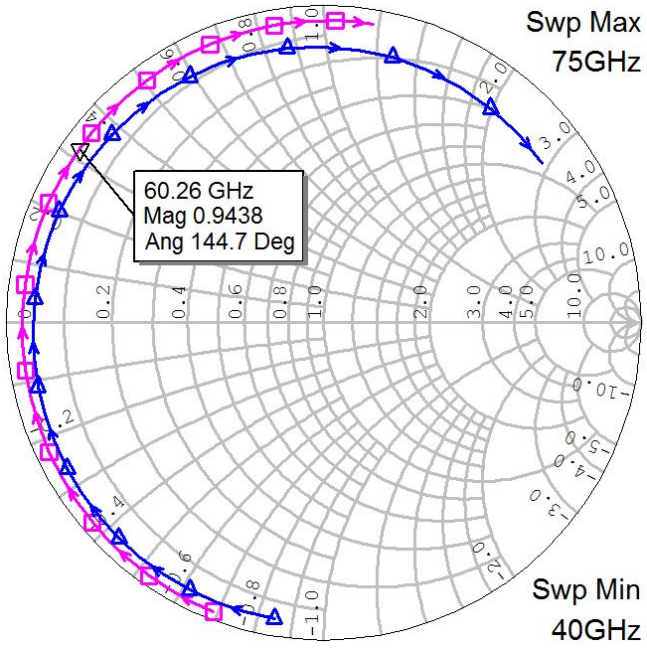
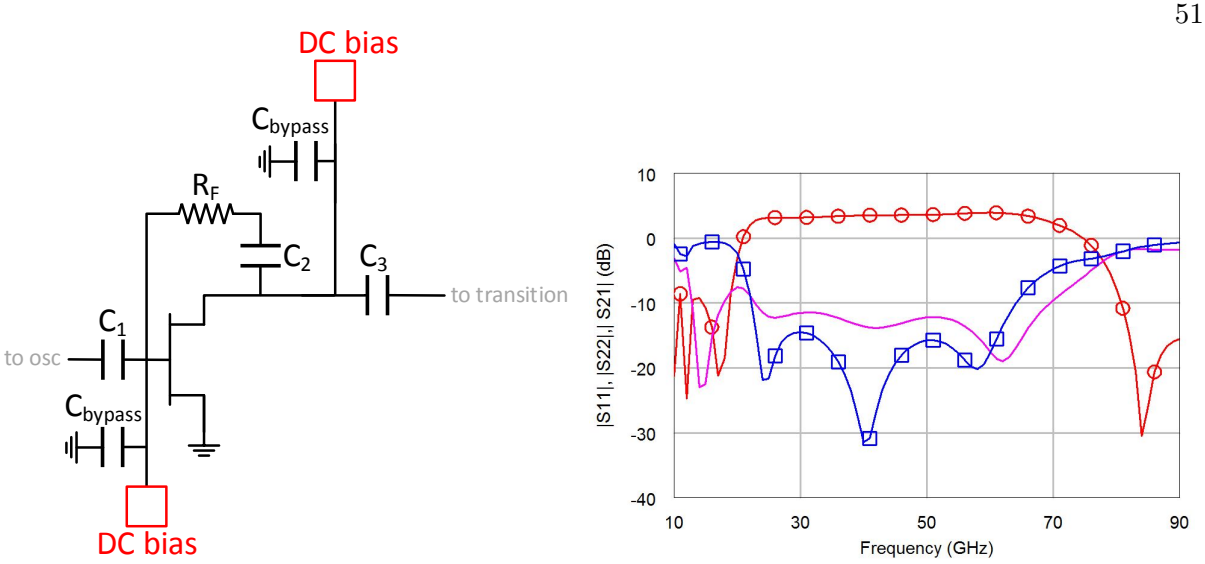


Figure 3.9: The 600 μm fixed length stub reflection coefficient in pink and the tunable short circuit stub in blue with Vg = -20.6 V.

The optimal impedance to present to the oscillator output has already been determined by the load pull simulation. To ensure that the oscillator always sees this impedance regardless of loading on the MMIC output, a buffer amplifier is included. The buffer amplifier is also designed to have a small amount of gain to increase overall output power. The buffer amplifier is designed as a common source amplifier with parallel feedback to improve broadband gain flatness and shown schematically in Fig. 3.10a. The simulated $|S_{11}|$, $|S_{21}|$ and $|S_{22}|$ are shown in Fig. 3.10b. The design of the buffer amplifier was done using the small signal model and a final check of the $|S_{11}|$, $|S_{21}|$ and $|S_{22}|$ was performed and validated with the large signal model.



(a) (b)

Figure 3.10: (a) The circuit schematic of the feedback buffer amplifier. C_1 and C_3 are DC blocking capacitors C_2 routes DC bias (capacitor top plate) and blocks DC (capacitor bottom plate.) (b) The simulated S-parameters of the buffer amplifier, $|S_{21}|$ is shown in red, $|S_{11}|$ in blue and $|S_{22}|$ in pink. The gain of the buffer amplifier is 4 dB at the center of the band.

Last, the waveguide-to-microstrip transition is designed. To avoid the use of wirebonds and increased assembly complexity, an on-chip transition is designed. The radial stub transition is shown in Fig. 3.11 and is based on the design detailed in [77]. The simulated S-parameters for the radial stub transition are shown in Figs. 3.12a and 3.12b and show low insertion loss, less than 0.3 dB from 40-70 GHz, and a return loss greater than 15 dB. The effect of non-optimal probe depths is also shown. The transition is simulated with a 50 μm SiC substrate. The bandwidth of the transition is much greater than the oscillator predicted output frequency range.

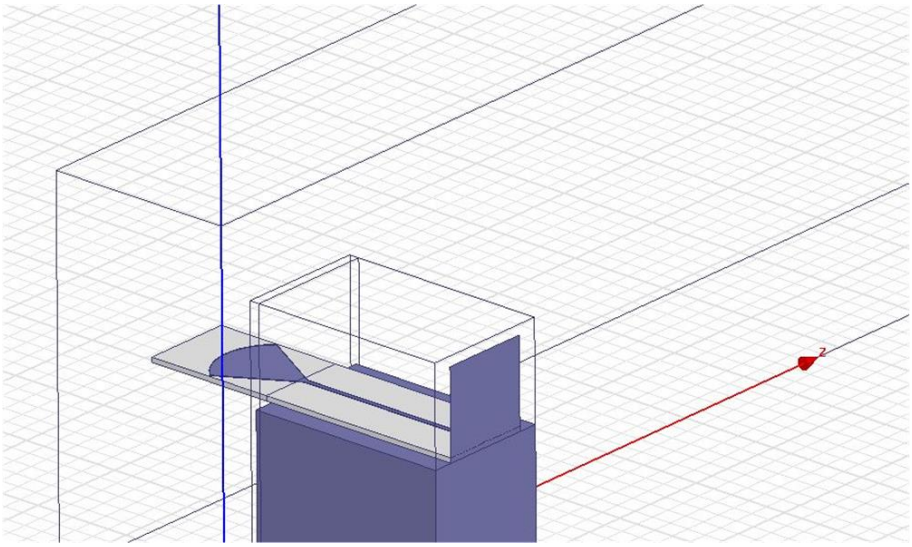
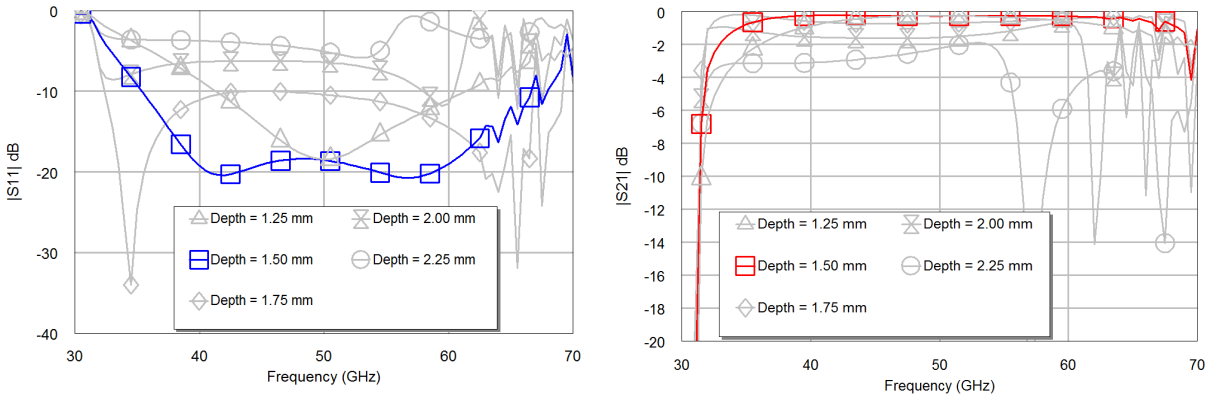


Figure 3.11: The simulation setup for the radial stub microstrip-to-waveguide transition on a 50 μm SiC substrate. The transition is inside a WR-15 waveguide and excited with a microstrip mode in a cavity with a reduced height to suppress higher order modes.



(a) (b)

Figure 3.12: (a) Simulated $|S_{11}|$ and variations of the probe depth into the waveguide. (b) $|S_{21}|$ and variations of the probe depth into the waveguide. The insertion loss for the transition is 0.23 dB at 50 GHz.

The tunable stub, reverse-channel oscillator, buffer amplifier and microstip-to-waveguide transition were then all simulated together to show the predicted output power over tuning voltage, V_c. The

result of that nonlinear simulation is shown in Fig. 3.13, and predicts an output power of 15.5 dBm for a wide range of tuning voltages. The nonlinear simulation to predict oscillation frequencies does not converge at V_c = -7 V but the transistor model should be correct for small negative V_c voltages.

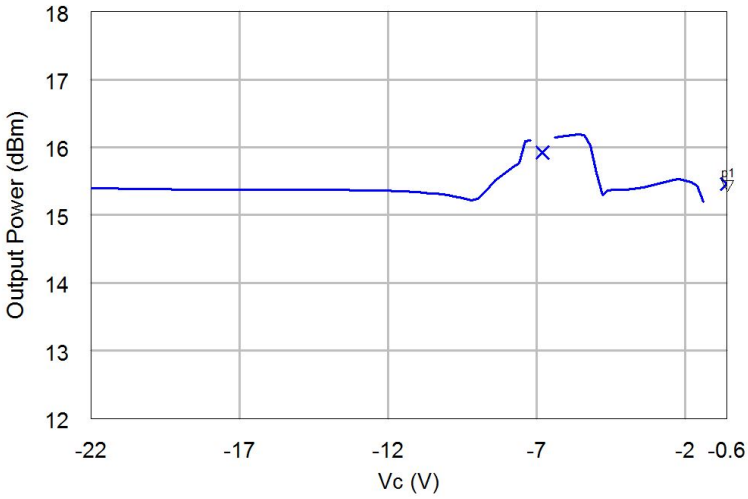


Figure 3.13: The simulated output power versus control voltage, V_c, for the complete reverse-channel oscillator. The simulation includes the tunable stub, reverse-channel oscillator, buffer amplifier and S-parameters from the microstrip-to-waveguide simulation.

The complete layout of the VCO is shown in Fig. 3.14. Each section of the layout is described below.

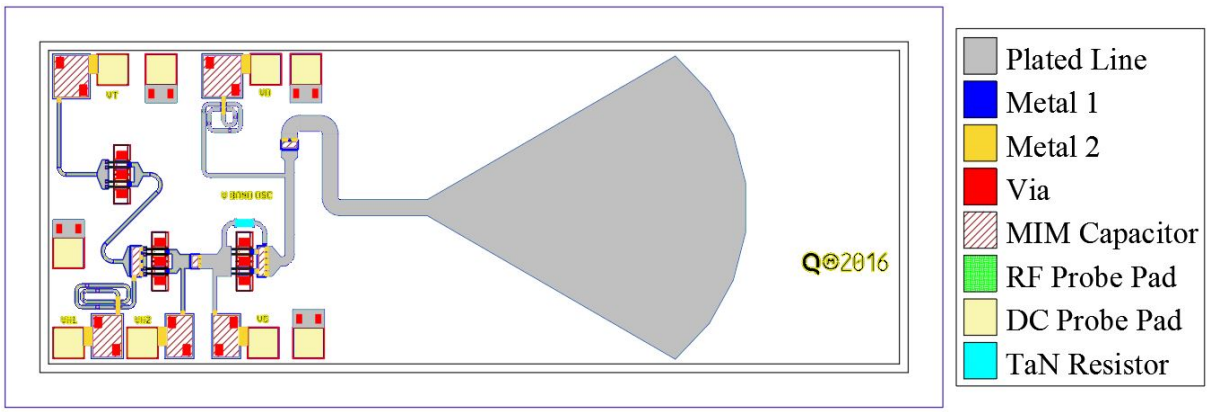
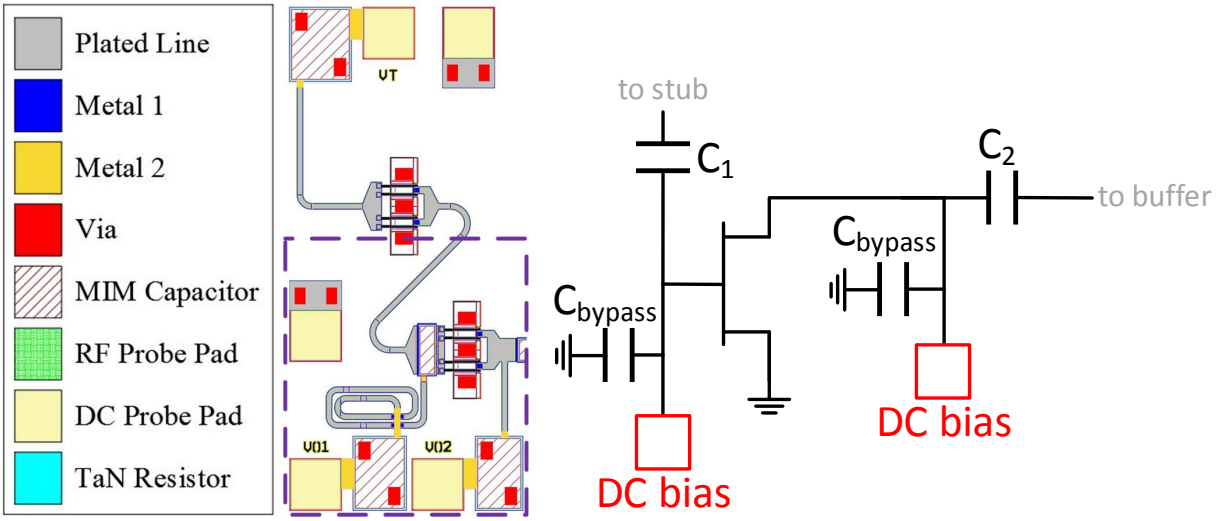


Figure 3.14: The detailed layout of the V-band oscillator. The total die size is 2.7x1.15 mm^2.

The oscillator layout is highlighted in Fig. 3.15a. Because of the simple circuit topology of the reverse channel design, the layout is compact. The highlighted area measures 400 μm x 300 μm and has bias and supply voltage routing and bypass capacitors. The bypass capacitors are designed in a capacitor-over-via way to minimized space. The large capacitor at the transistor gate is part of the bias tee, it acts as a DC path from the gate DC bias pad, V_{O1}, and blocks DC from being applied to the adjustable stub network. The matching network between the oscillator and the buffer amplifier is also very compact, measuring 176 μm. The challenge in higher frequency interstage matching network design is to match the drain impedance of one stage to the gate impedance of the other without adding unnecessary lengths of transmission line. Because solutions to the impedance transformations of matching networks repeat every half-wavelength, the goal is to route bias and supply voltages and perform matching without adding multiple half-wave lengths of transmission line. The circuit schematic is shown in Fig. 3.15b.

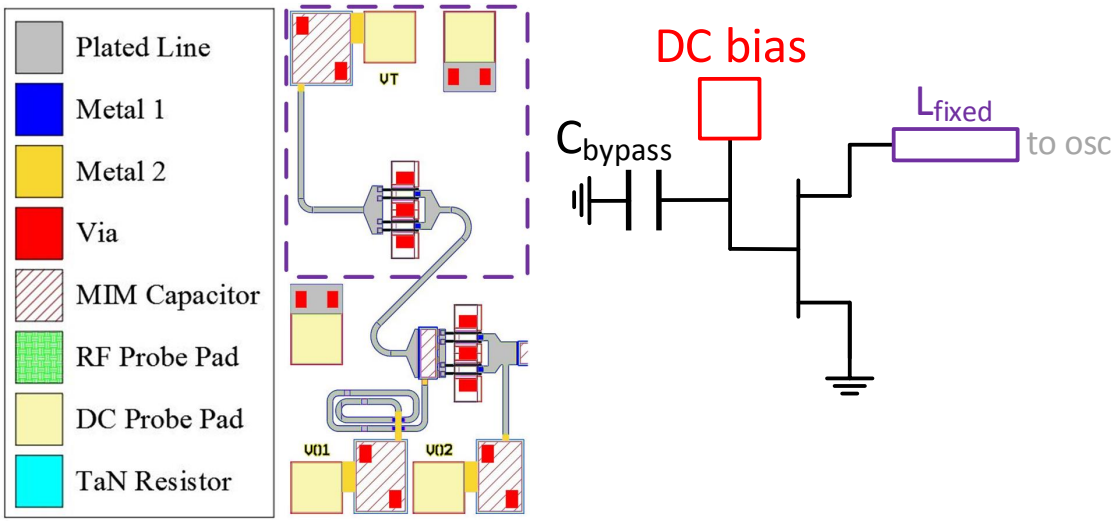


(a) (b)

Figure 3.15: (a) The reverse channel oscillator layout detail, highlighted in purple. (b) The corresponding circuit schematic.

The tunable stub circuit is shown in Fig. 3.16a. This circuit is simple to implement and the layout relies primarily on adjusting the "S" bend stub to be close to the minimum overall stub size required

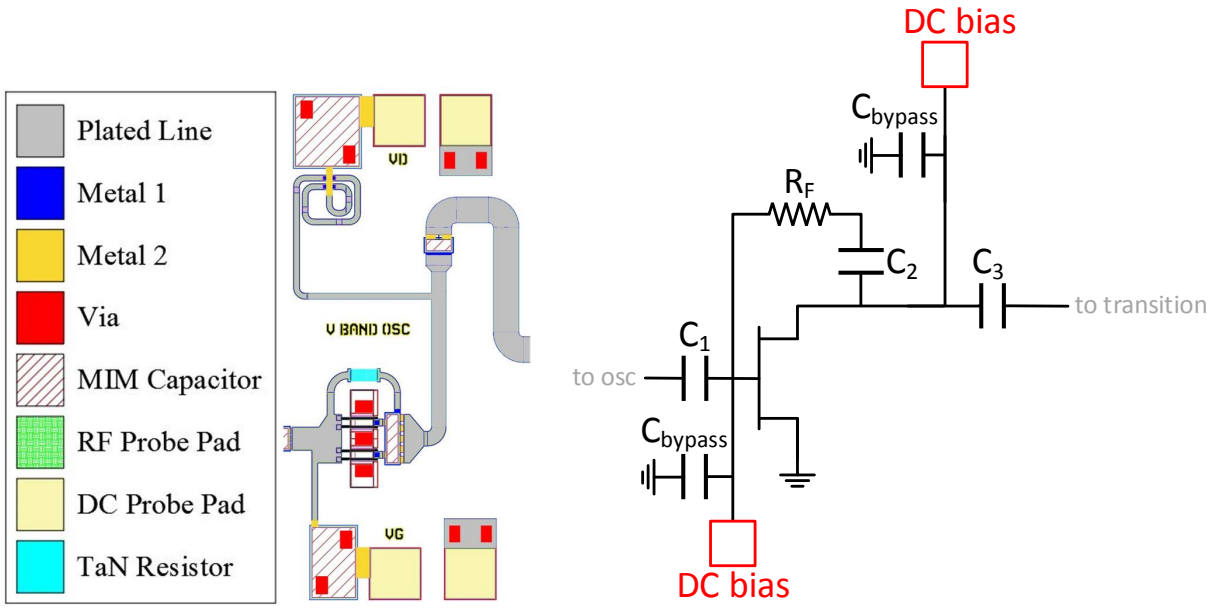
for 60 GHz operation. The transistor is then biased from the DC pad to be the adjustable part of the stub network. Because the gates of the transistors in this process are developed with an electron beam machine, the transistors must be vertically aligned so the stub has to route in a bend as shown. The equivalent circuit schematic is shown in Fig. 3.16b.



(a) (b)

Figure 3.16: (a) The tunable short circuit stub, highlighted in purple. (b)The circuit schematic of the tunable short circuit stub.

The last part of the circuit layout is the buffer amplifier and is shown in Fig. 3.17a. The broadband gain of the buffer amplifier is a result of the parallel feedback resistor shown. This resistor is 50 μm x 20 μm and has a value of 128 Ω . The resistor must also be DC blocked from the drain supply and gate bias to not interfere with the buffer amplifier's operating point. To do this, the same type of DC block as used previously was employed. The capacitor C_2 in the schematic shown in Fig. 3.17b routes DC supply for the drain on the top plate and RF signal through the feedback path on the bottom plate. Without this capacitor, a large DC current would flow through the feedback capacitor. The output matching network of the buffer amplifier transforms the impedance of the amplifier to 50 Ω before the microstrip-to-waveguide transition.



(a) (b)

Figure 3.17: (a) The layout detail of the buffer amplifier. (b) The circuit schematic of the feedback buffer amplifier. C_1 and C_3 are DC blocking capacitors, C_2 acts as part of a bias tee.

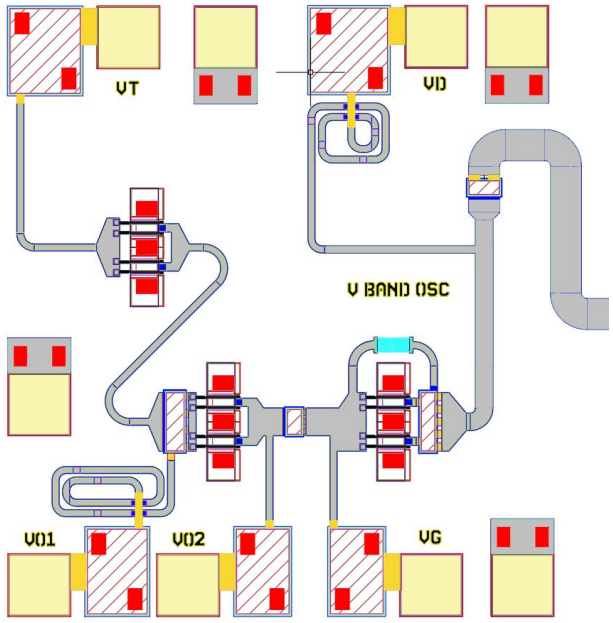


Figure 3.18: Close-up view of the detailed layout of the tunable short-circuit stub, oscillator circuit, and buffer amplifier.

The previous sections of the oscillator circuit are all combined in the detailed layout drawing in Fig. 3.18. The remainder of this chapter describes the waveguide assembly design and the measured results of the oscillator.

3.5 AM Waveguide Intergration

The fabricated V-band waveguide assemblies for the VCO are shown in Figs. 3.20, 3.21. Similar assemblies were made with WR-19 for U-band operation. Traditional machining was used to create the set shown in Fig. 3.20 and direct metal laser sintering (DMLS) additive manufacturing was used to create the other in Fig. 3.21. The assembly is designed in a split block fashion, the two halves are fastened together after the DC bias board, bypass capacitors and MMIC are mounted on one half. The pedestal on the left half in both figures is constructed to suppress cavity modes in the assembly. On the right half, the MMIC integrated transition sits on a pedestal and will be inserted into the waveguide as in Fig. 3.11. Once assembled, the waveguide output is interfaced with a standard UG-387 (MIL-DTL-3922/67E) flange. The mechanical drawing of the DC bias board that provides drain supply and gate bias voltages to the VCO is shown in Fig. 3.19.

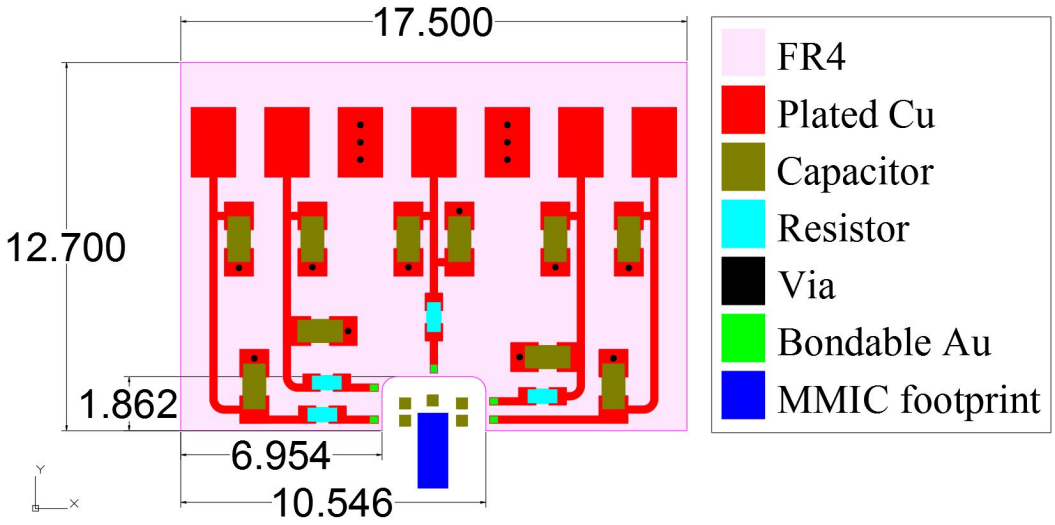


Figure 3.19: Assembly drawing of the bias and control board. The total size is 17.5x12.5 mm^2. All dimensions are specified in mm.

To compare the two manufacturing techniques, waveguide-to-microstrip-to-waveguide test structures were also fabricated with traditional manufacturing and AM, shown in Fig. 3.22. The profile of the alumina thin film test structure is shown in Fig. 3.23.

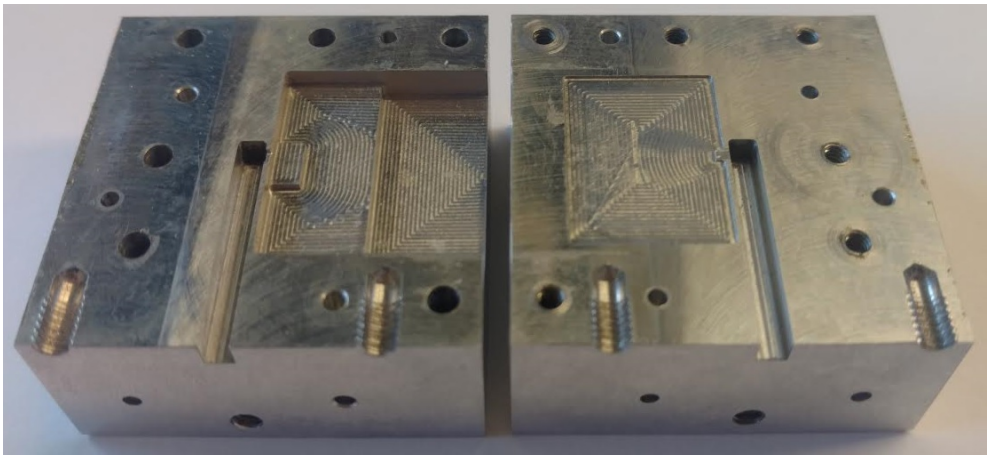


Figure 3.20: Photograph of machined V-band waveguide housing. The waveguide is WR-15 and made of Al. Each split block is approximately 3.5 cm per side. WR-19 waveguide housings were also fabricated.

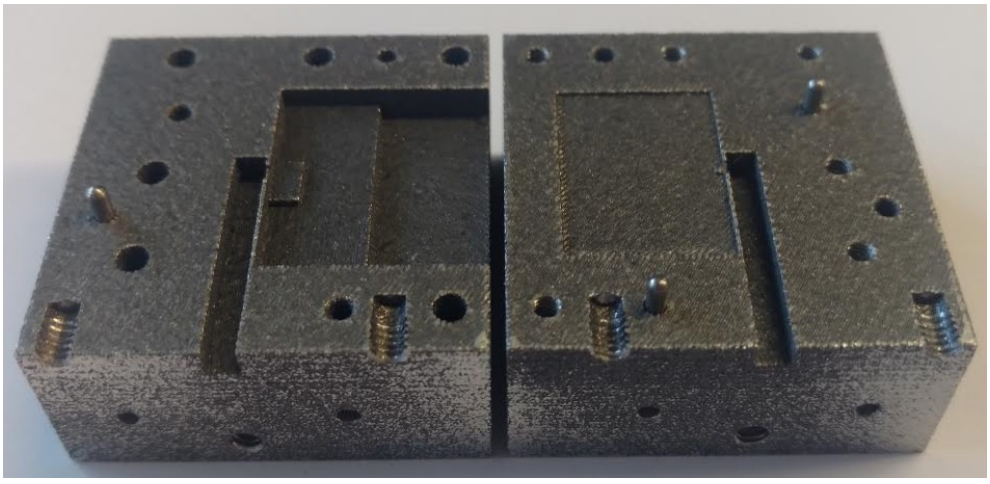


Figure 3.21: Photograph of AM V-band waveguide housing. The waveguide is WR-15 and made of AlSi10Mg. Each split block is approximately 3.5 cm per side. WR-19 waveguide housings were also fabricated.

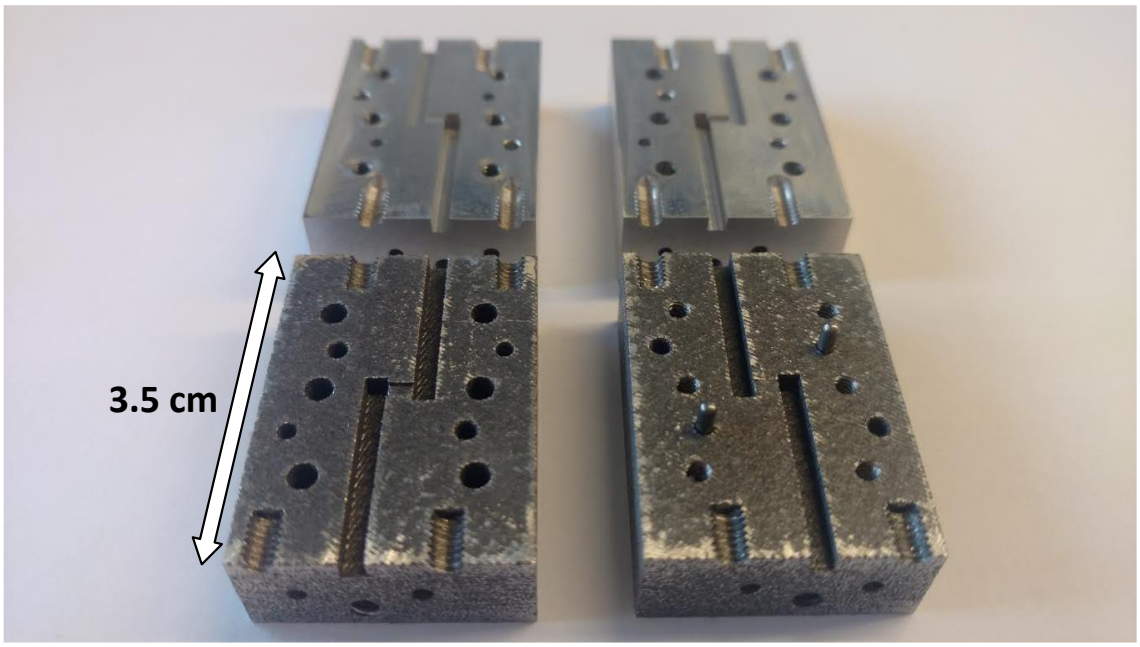


Figure 3.22: Photograph of the AM V-band test assemblies with AM and traditional machining. The AM structures are shown in the foreground and traditionally machined in the background.

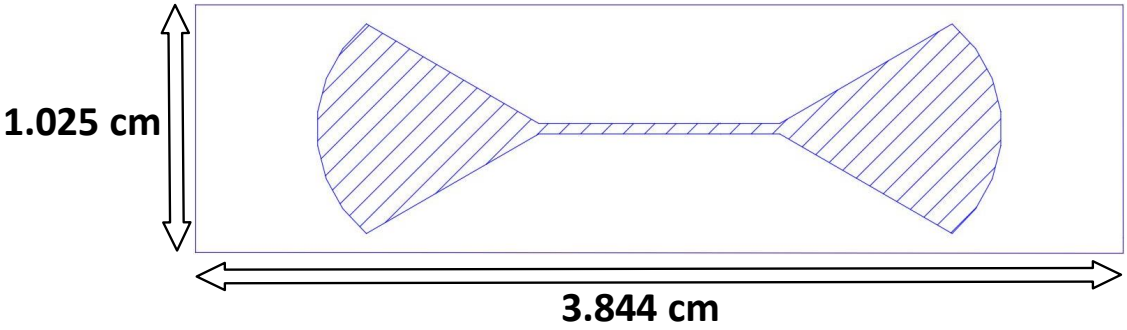


Figure 3.23: Assembly drawing of the V-band alumina test structure. The metal layer is hatched and the bare alumina is white. The thin film size is 3.844x1.025 mm^2 and 100 μm thick.

The photographs of the assembled traditionally machined and AM waveguide-to-microstrip-to-waveguide test structures are shown in Figs. 3.24 and 3.25.

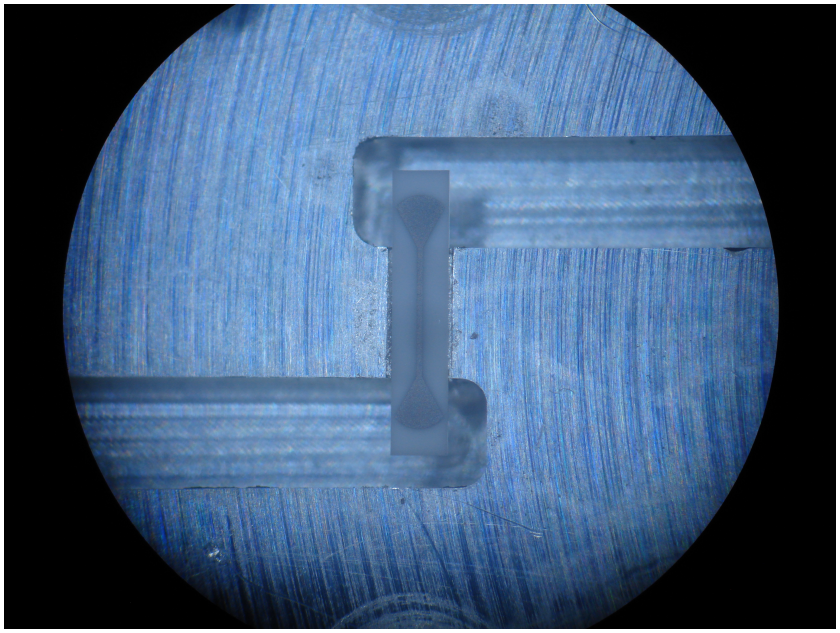


Figure 3.24: Assembled machined V-band waveguide-to-microstrip-to-waveguide test structure. The waveguide is WR-15 and made of Al.

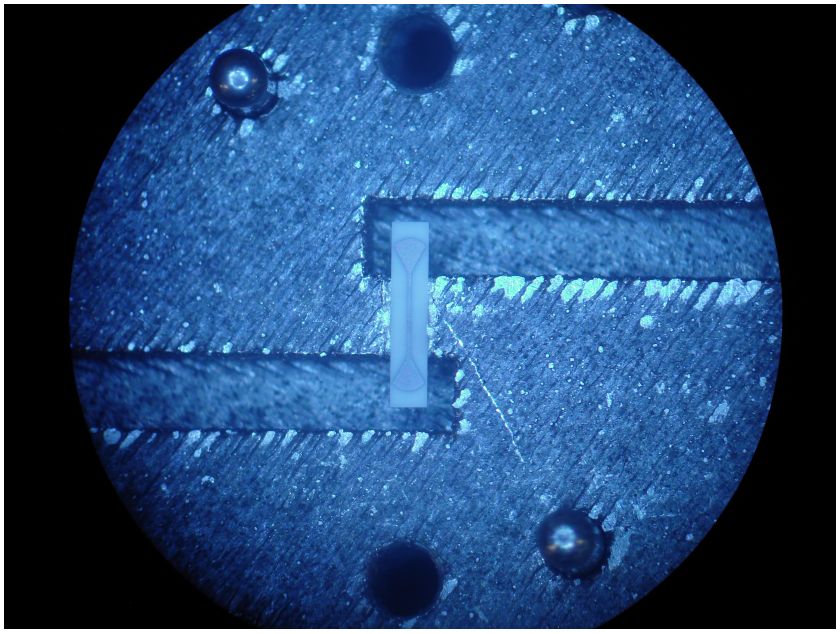


Figure 3.25: Assembled AM V-band waveguide-to-microstrip-to-waveguide test structure. The waveguide is WR-15 and made of AlSi10Mg.

The measured S-parameters are shown in Figs. 3.26 and 3.27.

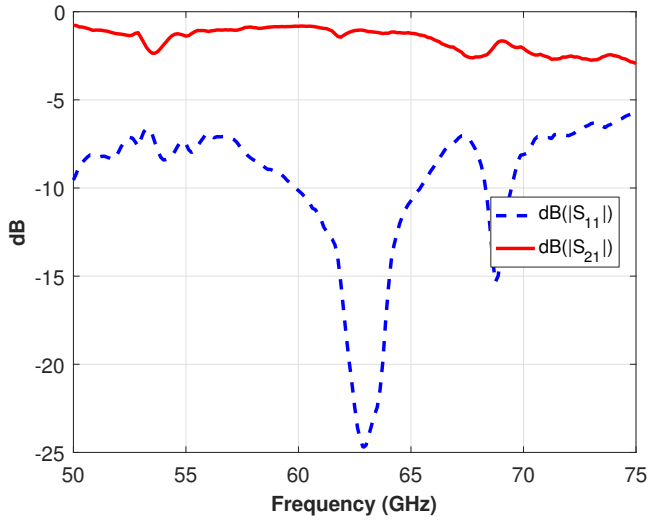


Figure 3.26: $|S_{11}|$ and $|S_{21}|$ for the machined V-band waveguide-to-microstrip-to-waveguide test structure. The $|S_{21}|$ data shown is the measured loss divided by two to approximate the loss of a single transition.

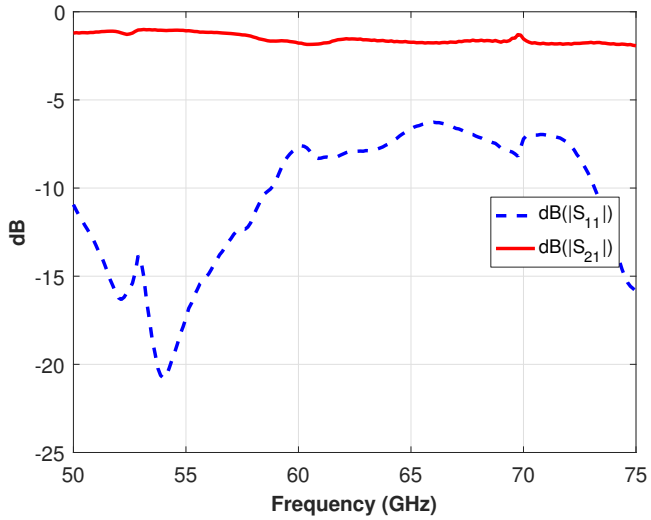


Figure 3.27: $|S_{11}|$ and $|S_{21}|$ for the AM V-band waveguide-to-microstrip-to-waveguide test structure. The $|S_{21}|$ data shown is the measured loss divided by two to approximate the loss of a single transition.

The measured S-parameters show through loss of the transition to be low and similar to simulated performance. The insertion loss is 0.82 dB and 1.7 dB at 60 GHz for the machined and AM waveguide assemblies, respectively. This loss includes not only the transition but the small microstrip section in the middle that measures 1000 μm and has a simulated loss of 0.068 dB. More details on additively manufactured waveguides is given in chapter 6.

3.6 Measurements and Conclusion

Shown in Fig. 3.28 is a microphotograph of the VCO during fabrication. The completed V-band machined and AM waveguide assemblies are shown in Figs. 3.29 and 3.30.

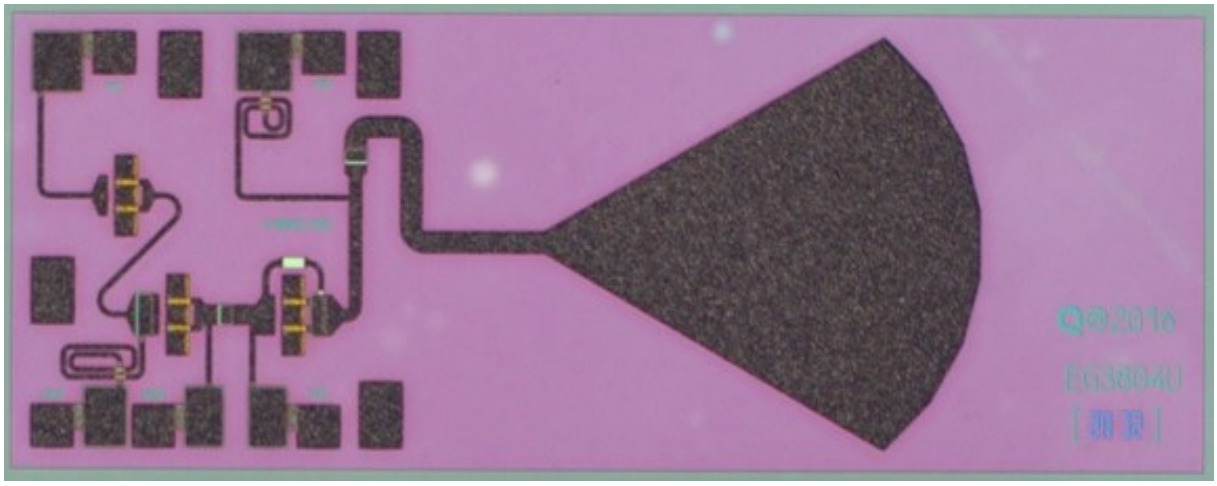


Figure 3.28: Microphotograph of the VCO during fabrication. The total die size is 2.7x1.15 mm^2.

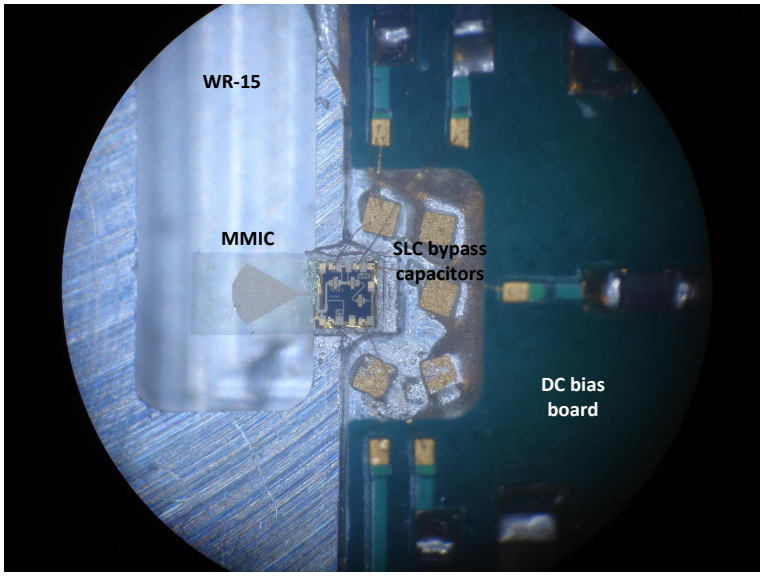


Figure 3.29: Complete V-Band oscillator assembly with MMIC, bypass capacitors, bias board and DC wirebond connections. The waveguide housing is fabricated in Al with traditional machining. The waveguide is WR-15 and made of Al.

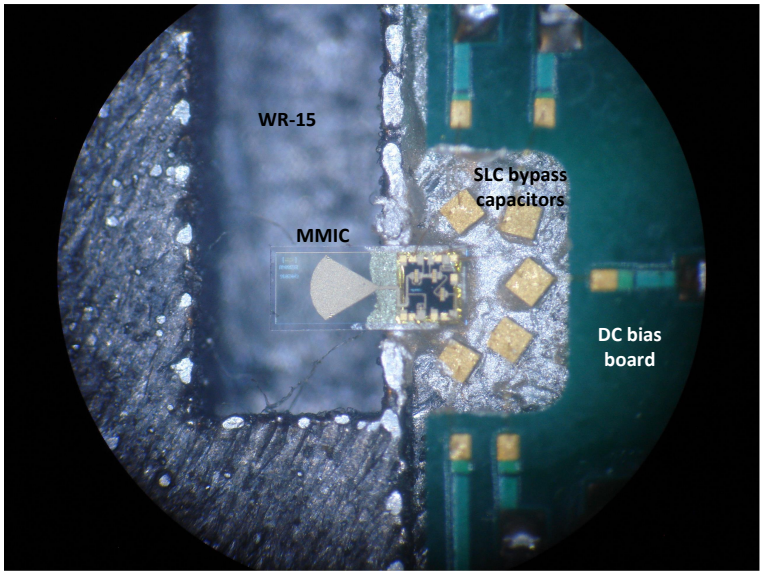
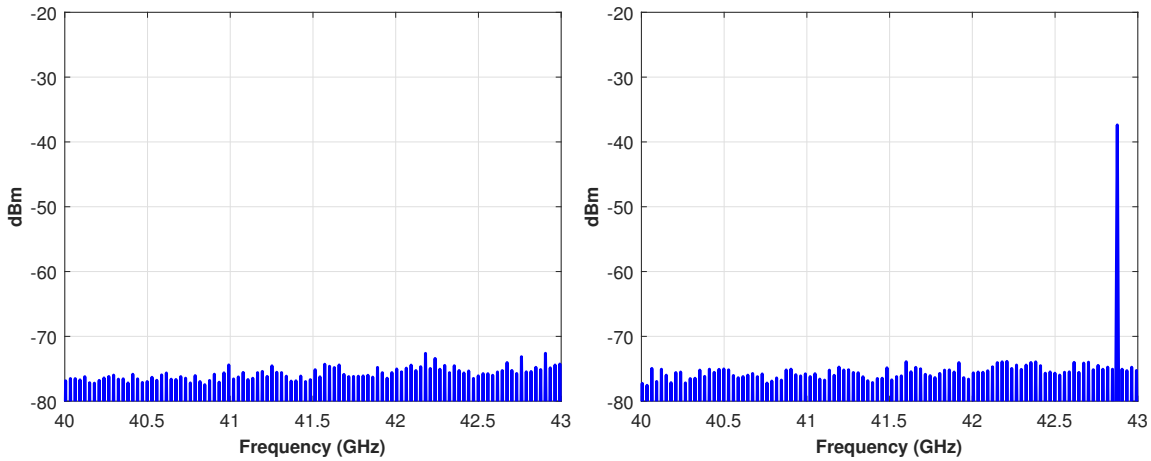


Figure 3.30: Complete V-Band oscillator assembly with MMIC, bypass capacitors, bias board and DC wirebond connections. The waveguide housing is fabricated in AlSi10Mg with AM.

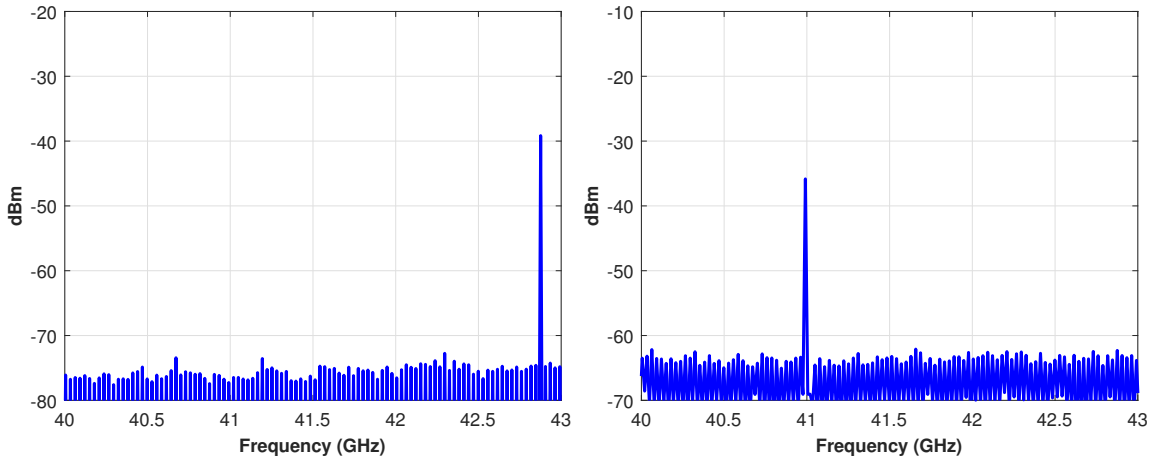
The U-band and V-band VCO modules, in WR-19 and WR-15, were measured with a N9030A for

40-44 GHz operation and with a M1970V waveguide harmonic mixer for 50-75 GHz operation. The noise floor of the N9030A used to test the VCO is shown in Fig. 3.31a. The output power and frequency of the V-band oscillator is shown for tunable stub control voltages, V_c, = -2, -3 and -6 V in Figs. 3.31b, 3.32a, 3.32b. The bias conditions for the above measurements are as follows. For the oscillator, V_d = 15 V and V_g = -0.58 V, I_d = 12 mA. For the buffer amplifier, V_d = 15 V and V_g = -1 V, I_d = 10 mA. The control voltage, V_c, was swept from 0 to -10 V but oscillations were only observed from -2 to -6 V. A wide range of biases and supply voltages was tried to attempt to optimize output power. As shown in Figs. 3.31b, 3.32a, 3.32b, the output power of the oscillator is below the simulated values and the range of tunable output frequency is limited to 40.99 - 42.88 GHz. This is thought to be due to several fabrication problems. First, the backside metal on the wafer was etched to remove the ground plane below the radial stub microstrip-to-waveguide transition. The etchant also undercut the ground plane metal by seeping into the wafer saw streets. This caused the backside metal under the oscillator circuit to lift off and makes the ground connection from the transistor vias and DC bypass capacitors questionable.



(a) (b)

Figure 3.31: (a) The noise floor of the N9030A. b) The output tone frequency and power for V_c = -2 V. The tone power is -37.38 dBm and the frequency is 42.76 GHz.



(a) (b)

Figure 3.32: (a) The output tone frequency and output power for V_c = -3 V. The tone power is -38.82 dBm and the frequency is 42.88 GHz. (b) The output tone frequency and output power for V_c = -6 V. The tone power is -35.84 dBm and the frequency is 40.99 GHz.

Second, the g_m of the devices was measured to be 30-40% lower than the model used in design. Because the g_m is lower than simulated, the lower output power is not a surprise. These fabrication issues are not uncommon in a process under development and new MMICs are currently being fabricated.

3.7 Contributions from This Chapter

The specific contributions to the field from this chapter are as follows:

- Demonstrated analysis and design of reverse-channel oscillator in GaN process.
- Demonstrated feasibility of AM AlSi10Mg waveguide assemblies in U-band and V-band with measured results for insertion loss and return loss.
- Demonstrated measured performance of V-band microstrip-to-waveguide radial stub transition. This transition allows for the removal of wirebonds and other labor intensive processes to couple energy from a millimeter-wave MMIC to waveguide.

Chapter 4

Analysis and Design of 235 GHz GaN-on-SiC Amplifiers

Contents

4.1 Motivation for MMICs Operating at 235 GHz

This chapter focuses on the applications, technology and design of integrated circuits that operate above 200 GHz. Integrated circuits and resulting systems operating at low sub-terahertz frequencies (100s of GHz) are currently limited by device technology, packaging loss, and very high unit cost. However, systems operating at these frequencies have unique and interesting uses and research and development in this area continues to progress. The technology is nevertheless not yet fully developed and design and fabrication times can be very long with low device yields.

Before showing why and in what areas there is interest in MMICs operating at such frequencies, it is necessary to understand what the Earth's atmosphere is like for very small wavelength EM waves. Shown below, in Fig. 4.1, is an atmospheric attenuation chart from [78]. Between the H_2O attenuation peaks at approximately 200 GHz and 350 GHz is a range of low-attenuation that is known as an atmospheric window. In this frequency range, a propagating plane wave in free space will have a wavelength $\lambda = 1.5$ to 1 mm ($f = 200$ to 300 GHz.) While there is some interest in operating wireless communications systems near the high attenuation regions in Fig. 4.1 for privacy, most systems are built to operate in the low attenuation atmospheric windows and that is the focus of this work.

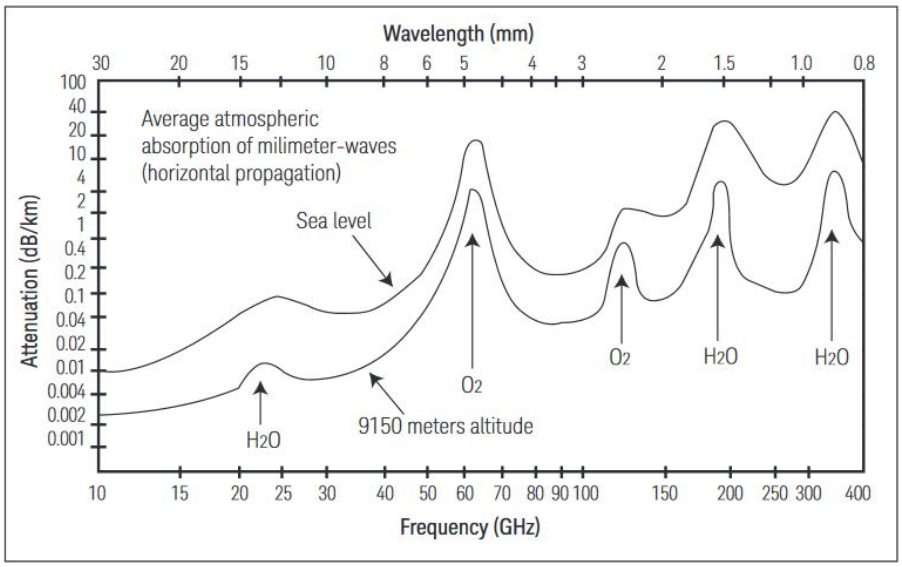


Figure 4.1: Atmospheric attenuation from 10 to 400 GHz at sea level and approximately 9 km. A region of relatively low attenuation occurs between 200-300 GHz.

Aside from the obvious benefits of high frequency operation (antenna size $\propto \frac{1}{f}$) and increased target resolution for radar systems, the combination of very small wavelength and minimized attenuation in this frequency range allows for several interesting applications, examples of which are summarized below:

- Millimeter-wave Radiometers - Microwave frequencies of 300 to 3000 GHz with corresponding wavelengths of 1 mm to 100 μm have an approximate photon energy of 1.2 to 12.4 meV. By use of the Maxwell-Boltzmann distribution, which relates electron energy to peak temperature as 1 eV = 11,604 K, energies of 1.2 to 12.4 meV correspond to a peak in black body radiation at 14 - 140 K. The 14 - 140 K temperature range corresponds to the vibrational motion of many lightweight molecules and atoms typically observed using molecular line spectroscopy [79]. Blackbody radiation from thermally illuminated gas and dust peaks at the low-terahertz range [79]. Lower in frequency, 183 GHz radiometers allow for precise measurement of precipitable water vapor and accurate prediction of changes in humidity [80].

- Wide-bandwidth Communications - The Japanese government estimated a 71% compound annual growth rate for mobile traffic in Japan from 2007 to 2017 [81]. Market research in the US forecasted similar advancements, resulting in total mobile data exceeding 327 PB/month (1 PB = 10^{15} Byte) by 2015 [82]. The authors of [82] suggest a 10 Gb/s or faster instantaneous bandwidth will be necessary in the future to keep up with data consumption demands. A 10 Gb/s signal corresponds to a 10 GHz BW when a modulation scheme such as QPSK or OQPSK is used. Systems in the future are not going to inherently be much more broadband so this naturally leads to higher frequency carriers and similar fractional bandwidth but greatly expanded absolute bandwidth. In [20] a communication system with a carrier frequency of 220 GHz is used to achieve a 25 Gb/s data rate. The system in [20] experiences similar losses due to rain fade and fog as systems operating in the E-band and low millimeter-wave regions, yet has superior bandwidth.

- Millimeter-wave Synthetic Aperture Radar - Synthetic aperture radar (SAR) can produce high-resolution images of a scene on the earth's surface in both range and cross-range. SARs can produce images of scenes at long range, and in adverse weather that are not possible with infrared or optical sensors [83]. Moving targets are a problem for SAR because of

serious distortion and displacement. However, resolution increases with frequency and video-speed imaging (frame rate of 10s of Hz vs 0.1 Hz) is possible with G-band based SAR systems. The output power levels needed to reach minimum signal-to-noise-ratios (SNR) for a G-band SAR in airborne applications is $\approx 50\,\mathrm{W}$, and this was part of the original motivation for the work done in this chapter [84].

The key to these applications is in the development of high performance active and passive MMIC technology.

4.2 HRL T4 GaN-on-SiC Process and Device Characteristics

This section describes the relevant features of the HRL T4 GaN-on-SiC process as they apply to millimeter-wave PA design. [1] The remainder of this chapter covers the passive and active technology used in the HRL T4 process, and details the design methodology and measured results of a 3-stage, 8-way power combined PA operating at 235 GHz.

4.2.1 Passive Technology

The passive technology used in this design includes transmission lines, through-substrate-vias, TaN thin film resistors and SiN MIM capacitors used to provide matching, signal routing, and DC supply and bias connections. An overview of these components and the basics of their fabrication is given in the introduction chapter. The key to the passive technology used in HRL's T4 process is based on Cu damascene metalization which allows for low-loss, high-power and high-current handling interconnects [4]. Cu damascene metalization is widely used in the Si semiconductor industry [85], [86], yet not common in III-V processes. The widespread use of Ti/Au metallization in III-V processes instead of Cu damascene metallization is due to concerns about Cu diffusion (contamination) into the epitaxial layers [4]. A simplified example cross-section showing various interconnects is given in Fig. 4.2. MMIC processes are often defined by the number of metal layers and in the example of Fig. 4.2 it is seen that the process has four metal layers, M0-M3. Also

[1] All details given are obtained from material that is publicly available. [4], [8], [7]

shown is the BCB layer that supports the M2 airbridge and protects the GaN devices, and the SiC dielectric substrate which the active and passive devices and transmissions lines are deposited on. Dry-etching of the BCB layer and the use of CMP (chemical-mechanical-polishing) instead of etching results in the ability to construct high-aspect ratio, well-defined rectangular metal traces, as desired in microstrip and CPW designs. The performance of the Cu damascene process is superior to the sometimes under-etched metal traces formed from the photoresist liftoff process [6].

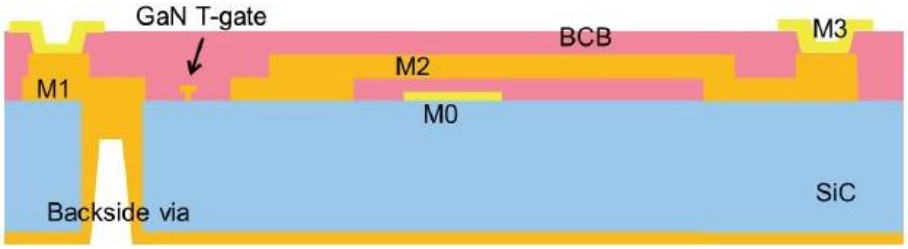
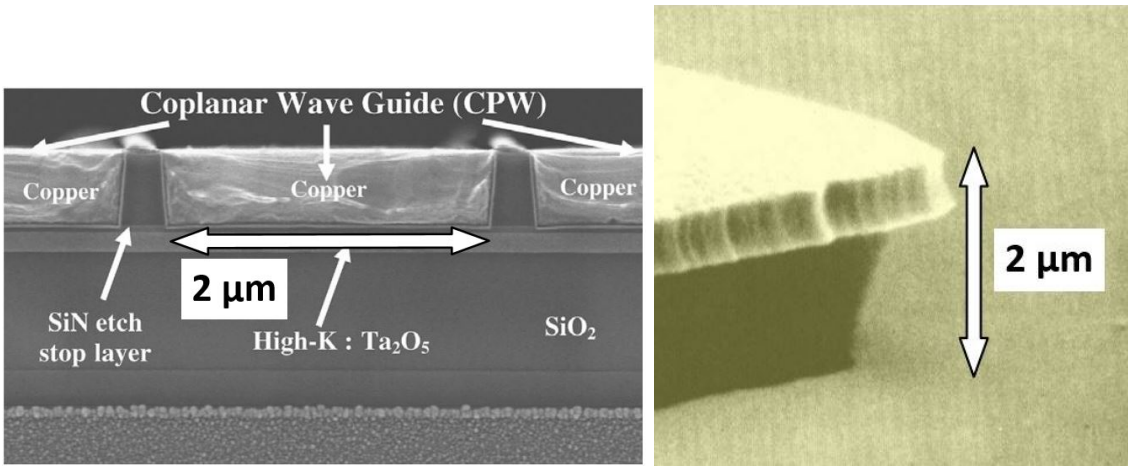


Figure 4.2: Cross-section view of CMP Cu interconnects combined with GaN-on-SiC MMIC technology. Source: [4]



(a) (b)

Figure 4.3: a) An example of a CPW line fabricated in a Cu damascene process on Si. The profile of the traces is vertically uniform. (b) The non-uniform vertical profile of a microstrip metal trace that has been developed with a photoresist liftoff process [5], [6]

.

4.2.2 Active Technology and Device Characteristics

The active technology, combined with the previously described passive technology is what allows the HRL T4 process to achieve $f_T > 300\,\text{GHz}$ performance with GaN technology. Shown in Fig. 4.4 are the recent developments in transistor architecture scaling that allows for devices with $f_T > 300\,\text{GHz}$. The previous GaN process technology at HRL, the T3 process, with devices represented by Gen-I in Fig. 4.4, used a traditional electron-beam (e-beam) T-gate metal lift-off fabrication process with a large 1.1 μm source-drain separation [8]. Higher frequency performance (W-band and higher) was achieved by simultaneously scaling the device gate length and epitaxial-layer stack up from larger geometries. In Gen-II and -III a higher f_T and f_{max} were achieved by reducing the source-drain separation from 1 μm to 100 nm and use of a self-aligned 40 nm gate fabrication process [7]. The gate length was also reduced to 40 nm to increase electron velocity. Last in Gen-IV, the self-aligned gate process in Gen-II and -III was modified to control the L_{gs} and L_{gd} independently. Gen-IV devices are what was used in the design of the 3-stage, 8-way combined PA, and the X-band Class-E amplifiers in chapter 2. This process has a $f_{max} = 517\,\text{GHz}$, a $NF_{min} = 0.8\,\text{dB}$ (noise-figure-minimum) at 50 GHz, and an increased $V_{breakdown}$ compared to Gen-II and Gen-III devices [8]. The gate length was also scaled further in Gen-IV to 20 nm and is shown in Fig. 4.5.

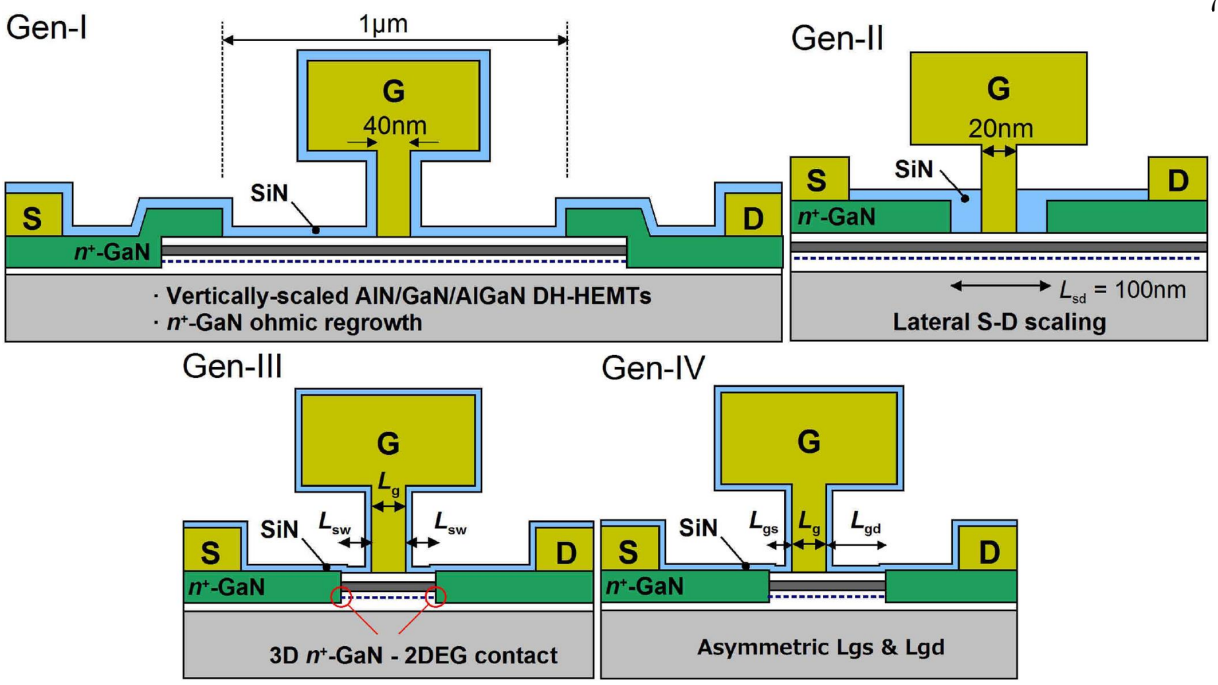


Figure 4.4: The various generations of transistor technology scaling at HRL. The current work was performed with Gen-IV technology. Source: [7]

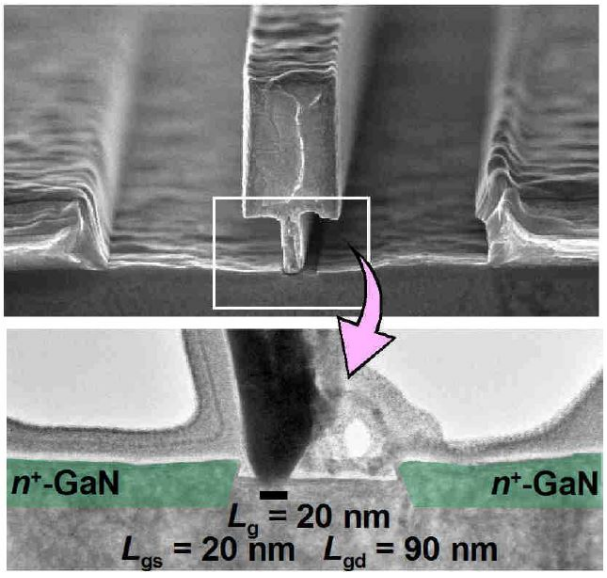


Figure 4.5: SEM photograph of HRL's Generation-IV T-gate. The gate length is 20 nm and the asymmetric-self-aligned gate fabrication process allows for a $L_{gs} = 20\,\text{nm}$ and $L_{gd} = 90\,\text{nm}$. Source: [8]

4.3 Design

The design of the 3-stage and 4-stage 8-way combined PAs is detailed in this section. The design of a MMIC PA starts with the process transistor models. Linear and non-linear simulations with a foundry transistor model provide all of the important parameters for the design, assuming low-loss interconnect and passive technology is available. In this work, a specific maximum output power was not defined but based on the work summarized earlier in this chapter, and the potential uses for 235 GHz amplifiers, meeting or exceeding the current state-of-the-art was the goal. The current state-of-the-art at the time this project began was approximately 100 mW at 235 GHz and this was the initial goal [17]. The first step in designing a MMIC PA is to select a transistor geometry that will serve as the unit cell, the fundamental device for subsequent power combining. A useful parameter for determining the correct device size to use in a PA is G_{max}, defined for two-port networks as:

$$G_{max} = \left|\frac{S_{21}}{S_{12}}\right| (K - \sqrt{K^2 - 1}) \tag{4.1}$$

where $K = \frac{1-(|S_{11}|)^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}$. A more in-depth discussion of the K factor and stability is given in chapter 5. A plot of G_{max} and K for the 4x20 μm and 4x100 μm device is shown in Figs. 4.6 and 4.7, as these represent a small and large device. The G_{max} plots show that the smaller 4x20 μm device still has gain at 235 GHz and the 4x100 μm transistor does not. The fact that devices with smaller channel lengths have greater high frequency gain is well known and therefore a 4x20 μm device was chosen as the unit cell for this design. One other important feature of the G_{max} plots is the discontinuity shown at 447 GHz in Fig. 4.6. This discontinuity is where K $>$ 1, meaning the region of lower frequency before the discontinuity will have more gain yet is not unconditionally stable. The 4x20 μm device will be unconditionally stable when operated past the discontinuity, yet gain is low or sometimes below zero dB. The G_{max} plot of the 4x100 μm device shows an interesting shape; there are two distinct discontinuities. These discontinuities again correspond to where K $>$ 1 (unconditional stability) meaning the device has a high-frequency region where it can oscillate. It is suggested that long device channels (100 μm) are not electrically short and at some bias conditions

could act as a feedback path or resonator.

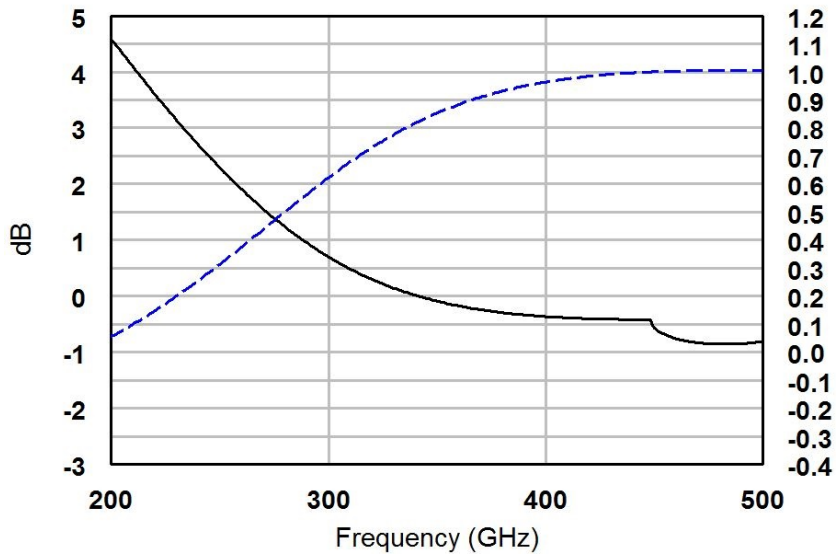


Figure 4.6: G_{max} (black) and K (blue dashed) for the 4x20 μm device. The discontinuity at approximately 447 GHz corresponds to where K $>$ 1.

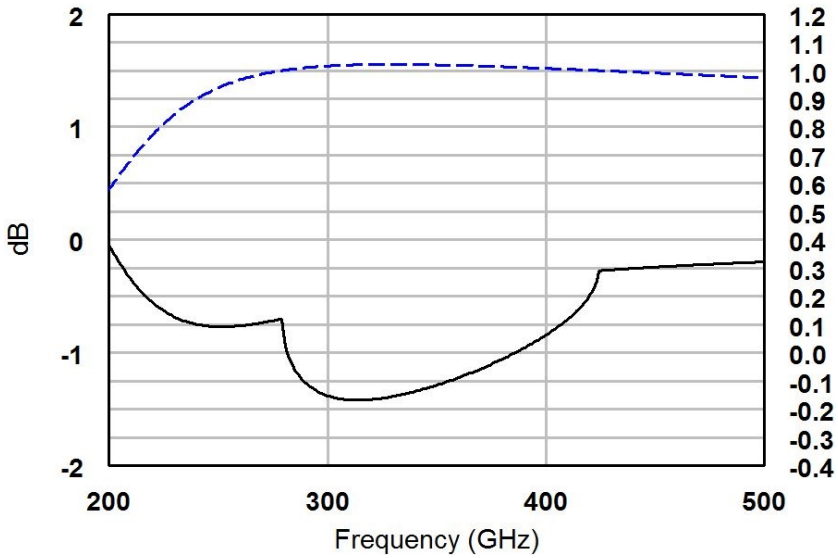
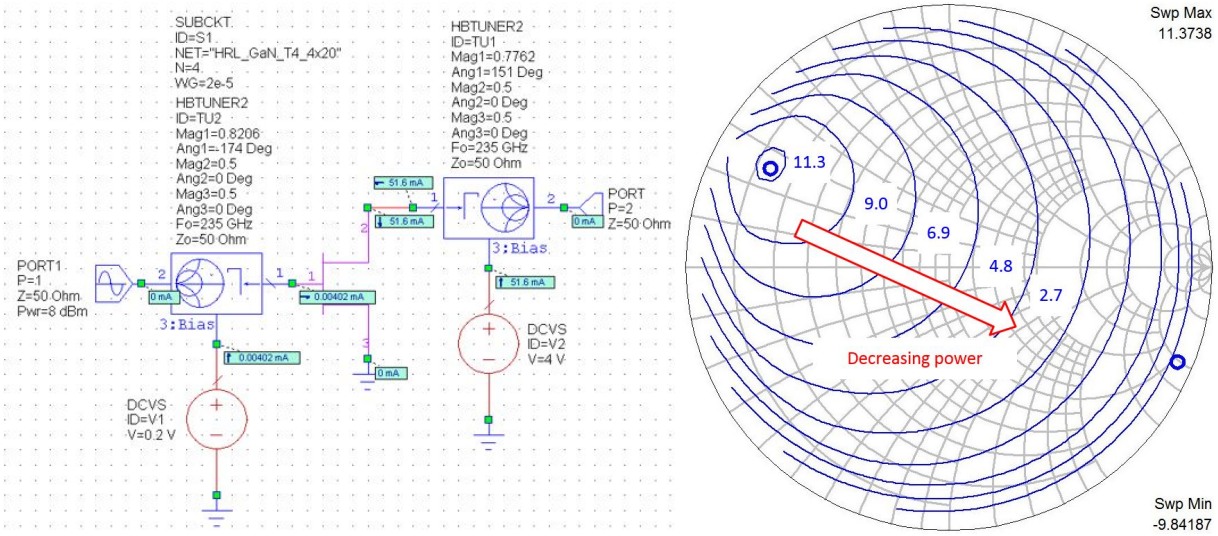


Figure 4.7: G_{max} (black) and K (blue dashed) for the 4x100 μm device. The discontinuities at approximately 278 and 447 GHz correspond to where K $>$ 1. This device has a limited unconditionally stable region between the two frequency points.

Shown in Fig. 4.8a is the load and source pull simulation setup using the 4x20 μm device. Gain, output power and PAE of a single 4x20 μm transistor was simulated and output power was maximized at this stage. The optimal combination of maximum output power and device gain was achieved with $\Gamma_S = 0.821 \angle$ -174 $^\circ$ and $\Gamma_L = 0.776 \angle$ 151 $^\circ$, resulting in an output power of 11.3 dBm and a large-signal gain of approximately 3.4 dB, with a drain supply voltage of 4 V and a gate bias voltage of -0.2 V.



(a) (b)

Figure 4.8: (a) Single 4x20 μm device load and source pull simulation setup. (b) The output power contours on the Smith chart show the optimal load impedance for maximum power.

In [1], a procedure is used to convert the load and source pull reflection coefficients into equivalent gate and drain impedances. Analysis of load pull data in [1] shows that transistor drain behavior more closely follows a parallel RC network than a series network. To convert the equivalent gate and drain impedances into a parallel RC network, Eqn. 4.2 is used.

$$Y_L^* = \frac{1}{Z_L^*} = \frac{1}{R_p} + j\omega C \tag{4.2}$$

where R_p is the equivalent real part of the impedance in parallel. By use of Eqn. 4.2, the Γ_S and Γ_L found from the simulated load pull result in an equivalent gate and drain impedance of $Z_{gate} =$

R + jX = 9.79 Ω + 4.05 pH and Z_{drain} = R + jX = 27.5 Ω + 53 pF. The networks that model the transistor gate and drain in the rest of the design are shown in Fig. 4.9.

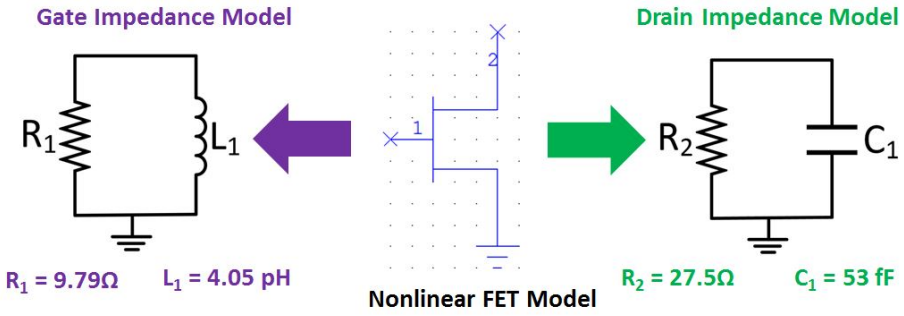


Figure 4.9: The optimal gain and output power equivalent gate and drain models for the 4x20 μm device. The gate behaves slightly inductive and the aggressive scaling of the transistor geometry results in a very low (53 fF) equivalent drain output capacitance.

4.3.1 On-chip Power Combining with Even Odd Mode Analysis

As is common in many MMIC PAs and can be seen here, the output power of an individual transistor is not great enough for the desired application, and power combining must be used. To get to 100 mW with the above device and a binary combiner ($n_{transistors}$ = 2, 4, 8, 16 etc) requires 8 transistors (11.37 dBm = 13.7 mW, 8x13.7 mW = 109.7 mW). Binary power combiners in MMIC PAs are widely used. The reason to combine smaller unit cell transistors instead of utilizing large periphery multi-finger transistors has already been explained. Power combiners can introduce new modes of operation not possible with single device power amplifiers. To avoid these new unwanted modes, binary structures are typically used as they imply basic inherent symmetry. The output section of the 8-way combined PA is shown in Fig. 4.10 with resulting half and quarter plane symmetry sections.

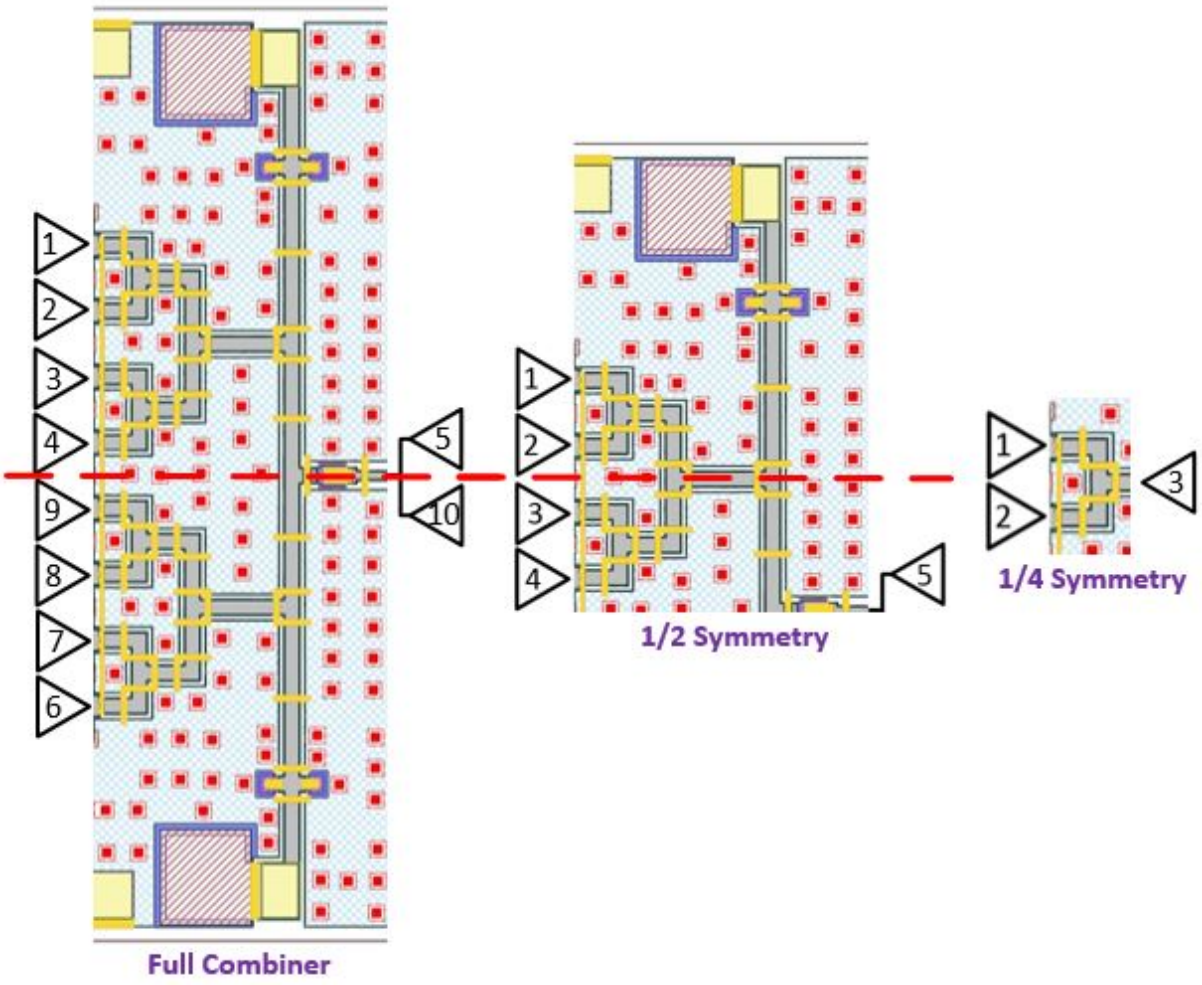


Figure 4.10: The 8-way combiner and half and quarter symmetrical sections. The half and quarter symmetrical networks are analyzed for odd mode instabilities.

The method used to analyze and design the input power splitter and output power combiner is based on decomposition of a symmetric network into even and odd mode components, illustrated in Fig. 4.10. The even mode represents the power combiner in a way that S-parameters of the network do not, with all transistors driven equally in magnitude. The odd mode represents undesired modes of operation, the scenario where one or more transistors load the others. The odd mode circuit is generated solely to detect instabilities that often arise in power combiners. To facilitate this decomposition, the network must first be symmetrical and any ports that lie on the various planes

of symmetry must be duplicated in parallel with their port impedances doubled. The port numbers shown in Fig. 4.10 are arranged where either the transistors (ports 1-4 and 6-9) or the output port (ports 5 and 10) would be. They are numbered in a way that allows for subsequent symmetrical network sections to be analyzed as in [87]. Ports 5 and 10 are duplicate ports with impedance $2Z_0$. arranged in parallel, connected by a short circuit. The half and quarter plane symmetric circuits shown in Fig. 4.10 represent odd modes of operation in the PA that must be analyzed for potential instabilities.

With the complete S-parameters of the 8-way combiner network denoted as $S_{i,j}$, the even and odd mode S-parameters, $S^E_{i,j}$ or $S^O_{i,j}$, are described as:

$$S^E_{i,j} = S_{i,j} + S_{i,n+j} \tag{4.3}$$

$$S^O_{i,j} = S_{i,j} - S_{i,n+j} \tag{4.4}$$

where n is the order of the resulting even or odd mode network, for an 8-way combiner that has 10 ports, n = 5. For the 8-way combiner as shown in Fig. 4.10, the even and odd mode S-parameters are expressed as:

$$S^E = \begin{bmatrix} S_{11}+S_{16} & S_{12}+S_{17} & S_{13}+S_{18} & S_{14}+S_{19} & S_{15}+S_{110} \\ S_{21}+S_{26} & S_{22}+S_{27} & S_{23}+S_{28} & S_{24}+S_{29} & S_{25}+S_{210} \\ S_{31}+S_{36} & S_{32}+S_{37} & S_{33}+S_{38} & S_{34}+S_{39} & S_{35}+S_{310} \\ S_{41}+S_{46} & S_{42}+S_{47} & S_{43}+S_{48} & S_{44}+S_{49} & S_{45}+S_{410} \\ S_{51}+S_{56} & S_{52}+S_{57} & S_{53}+S_{58} & S_{54}+S_{59} & S_{55}+S_{510} \end{bmatrix} \tag{4.5}$$

$$S^O = \begin{bmatrix} S_{11}-S_{16} & S_{12}-S_{17} & S_{13}-S_{18} & S_{14}-S_{19} & S_{15}-S_{110} \\ S_{21}-S_{26} & S_{22}-S_{27} & S_{23}-S_{28} & S_{24}-S_{29} & S_{25}-S_{210} \\ S_{31}-S_{36} & S_{32}-S_{37} & S_{33}-S_{38} & S_{34}-S_{39} & S_{35}-S_{310} \\ S_{41}-S_{46} & S_{42}-S_{47} & S_{43}-S_{48} & S_{44}-S_{49} & S_{45}-S_{410} \\ S_{51}-S_{56} & S_{52}-S_{57} & S_{53}-S_{58} & S_{54}-S_{59} & S_{55}-S_{510} \end{bmatrix} \tag{4.6}$$

The even and odd mode S-parameters now describe a 5-port network with either a virtual open at the plane of symmetry (even mode) or a virtual ground at the plane of symmetry (odd mode). The response of the even mode circuit is the ideal response of the power combiner, it represents how well the network will function as a balanced combiner. The reflection coefficient, Γ, at each device port, i, in the even mode circuit is given by Eqn. 4.7

$$\Gamma_i = S^E_{i1} + S^E_{i2} + S^E_{i3} + S^E_{i4} \tag{4.7}$$

The total combiner loss, the loss of the combiner network when all device ports are energized, is given by Eqn. 4.8:

$$\text{combiner loss} = \frac{S^E_{51} + S^E_{52} + S^E_{53} + S^E_{54}}{\sqrt{4}} \tag{4.8}$$

A plot of the simulated even mode S-parameters for the half-plane 5-port network, shown in Fig. 4.10, is shown in Fig. 4.11. The various odd mode networks are analyzed with the stability analysis technique described in chapter 5 by applying the even odd mode decomposition to each symmetrical network section.

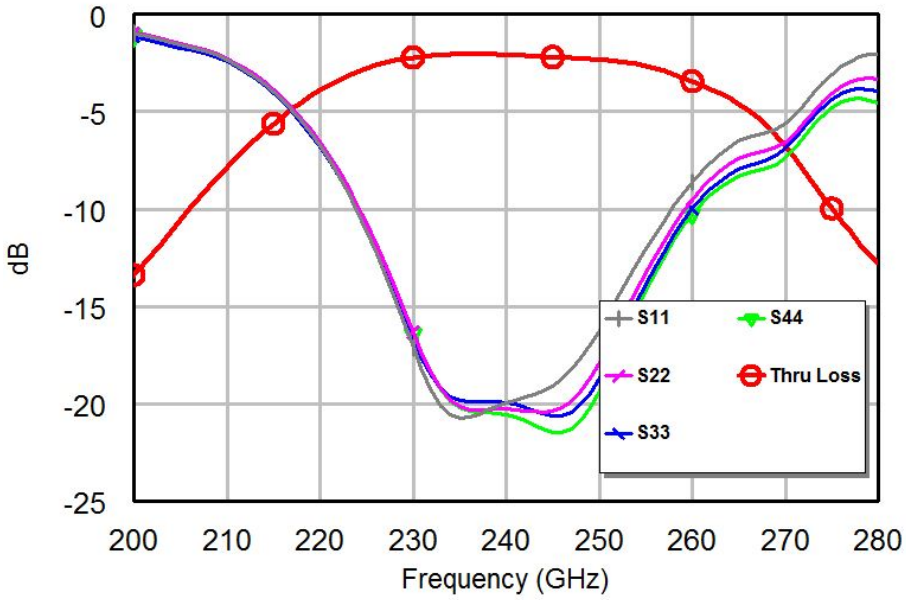
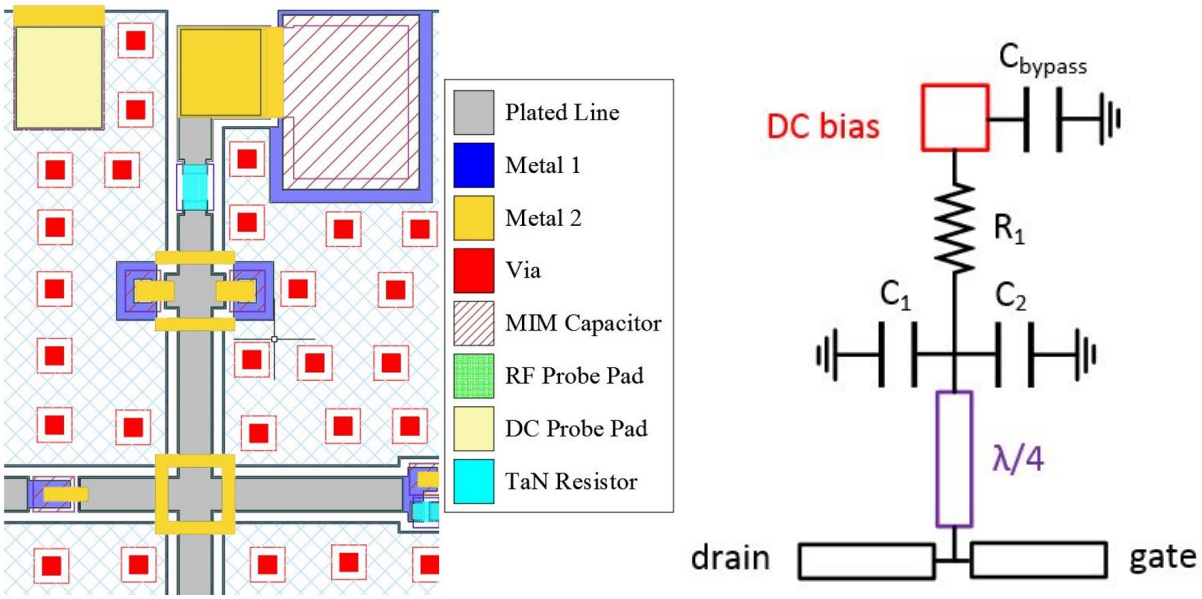


Figure 4.11: Simulated 8-way combiner S-parameters with even mode excitation. The results are from an EM simulation of the entire combiner. The loss mid-band is 2.1 dB.

4.3.2 Design Features

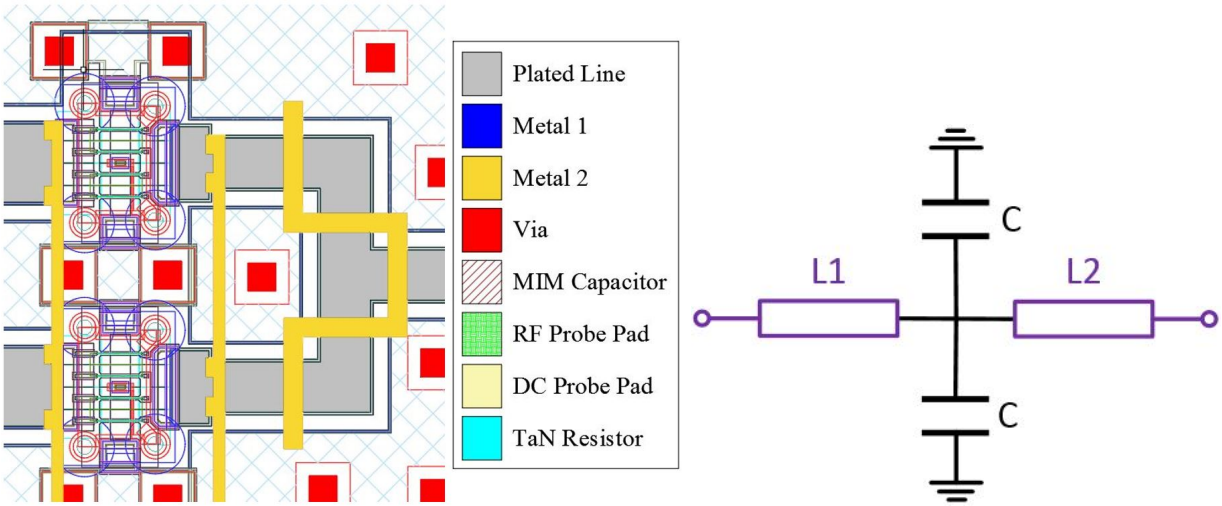
The main features of the PA design excluding the 8-way power splitter and combiner are detailed here. The bias tee which provides gate bias and drain supply to the transistors is shown in Fig. 4.12a. This structure utilizes a $\lambda/4$ transformer from the drain-gate line to two shunt capacitors. The two small shunt capacitors are a short at 235 GHz and this is transformed to an open at the drain-gate line. This serves two purposes: first to ensure that no RF signal is lost to the DC supplies, second, to allow the electrically and physically-large bypass capacitors at the DC pads to be arbitrary in size and position. Without the $\lambda/4$ transformer, the size and position of the components on the DC side of the bias tee would be critical and unwieldy because the blocking capacitor and DC pad are electrically large at these frequencies and their effects would have to be compensated for. A schematic of the bias tee structure is shown in Fig. 4.12b to illustrate the previous discussion.



(a) (b)

Figure 4.12: (a) The bias tee structure used in the MMIC PA design. The small shunt capacitors (red hatch pattern over M1) are a quarter-wave from the interstage connecting lines. The series resistor (cyan) is for stability. (b) The schematic view of the bias tee structure.

The air bridges formed by M2 to ensure equipotential ground around the lines can also be used as tuning elements. In Fig. 4.13a, the air bridges across the output of the transistors in the output combiner are tuned by moving them closer to or further from the transistor to help resonate out the reactance of the transistor and transmission lines. The air bridge can be modeled as a pair of 4.5 fF shunt capacitors that are a length L_1 from the transistor drain and L_2 from the output port. A plot of the input impedance of the network from the drain connection in Fig. 4.13a is shown for different lengths $L_1 = 50$ to $200\,\mu$m in Fig. 4.14.



(a) (b)

Figure 4.13: a) The layout view of multiple air bridges at CPW line bends and discontinuities. b) The circuit schematic for the air bridge. C $\approx$ 4.5 fF and this can be a minor tuning element in the design process.

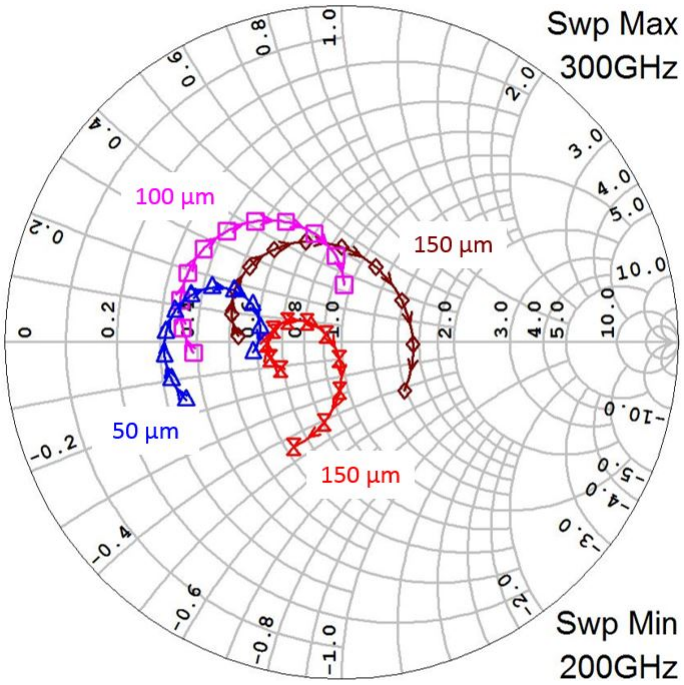
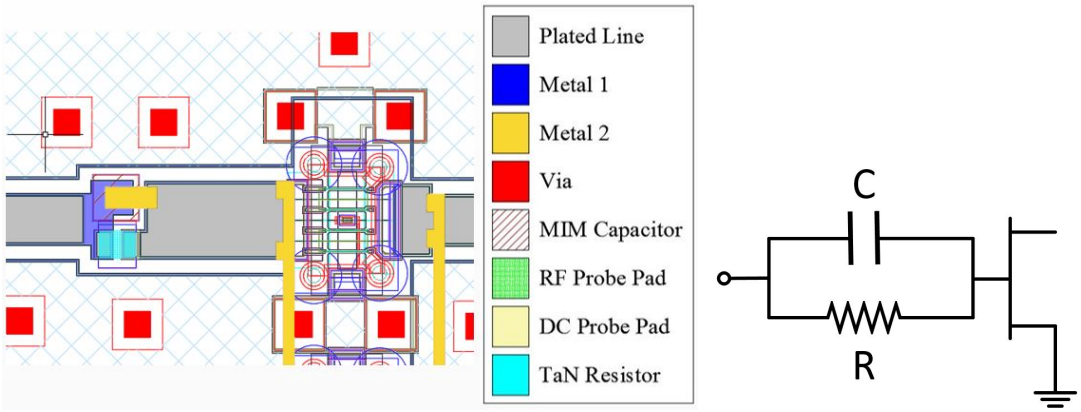


Figure 4.14: The input impedance of the air bridge network with increasing length L_1. The total length of $L_1 + L_2$ is kept constant and L_1 ranges from 50 to 200 μm in 50 μm steps.

Last, to help stabilize the PA, staggered parallel RC networks were added in series with each transistor gate as shown in Fig. 4.15a.



(a) (b)

Figure 4.15: a) The layout view of the parallel RC network in series with the transistor gate. b) The circuit schematic of the parallel RC network. R = 54.6 Ω and C = 42.2 fF.

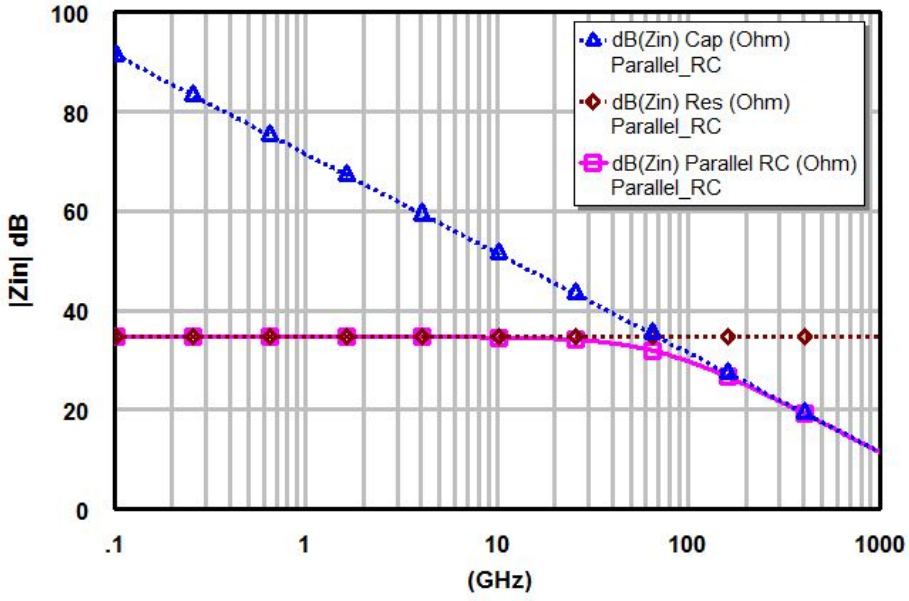


Figure 4.16: Impedance plot of the parallel RC stability network at each device gate. The impedance of the network (pink) is the parallel summation of the capacitor (blue) and the resistor (brown). The response of the network is the inversion of the impedance plot shown and acts as a high-pass filter.

This is a common preventative stability practice for power combined PAs. The break frequency of a simple RC filter is given by:

$$f_0 = \frac{1}{2\pi RC} \tag{4.9}$$

and the plot of Z_{in} for the parallel RC network is shown in Fig. 4.16 by adding the impedance of the resistor and capacitor in parallel. This network acts as a high-pass filter and helps to reduce low-frequency gain in the overall passband. The use of these filters at each gate and at each stage improves the rejection of low-frequency signal propagation. The distance of the RC network from each transistor in a given stage was kept constant but the network was moved closer or further from the transistor gate in different stages to tune the amplifier.

Shown in Fig. 4.17 is the simulated $|S_{11}|$ dB and $|S_{21}|$ dB for the 4-stage amplifier with the PDK nonlinear transistor model. The simulation was performed with 10 dBm input power and shows 10 dB large signal gain and an output power $>$ 20 dBm.

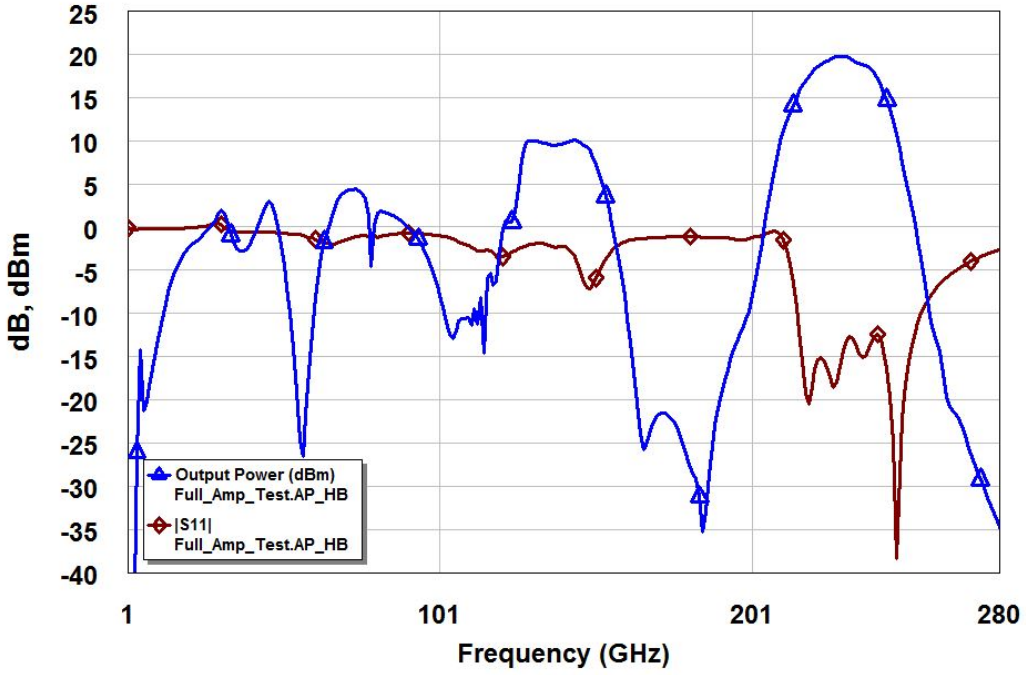
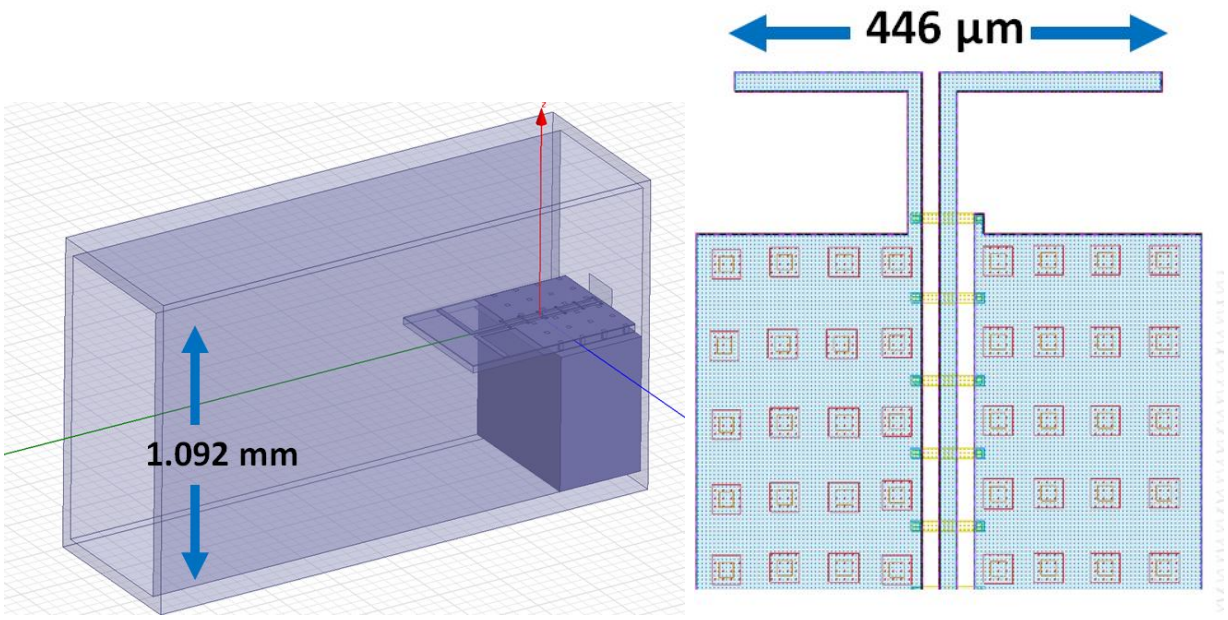


Figure 4.17: The $|S_{11}|$ dB (brown) and $|S_{21}|$ dB (blue) for the 4-stage amplifier with the 4x20 μm nonlinear model. There is significant gain at lower frequencies. For a 10 dBm input power, the simulation shows $>$ 20 dBm output power and 10 dB large signal gain.

4.3.3 Transition to WR 4.3 Rectangular Waveguide

Typical packaging solutions for MMICs usually include off-chip alumina, quartz thin film microstrip or CPW-to-waveguide transitions. These separate passive elements are expensive to fabricate and require wirebonding to connect to the MMIC. As an alternative to this approach, on-chip transitions can be incorporated into the MMIC design and couple directly to the waveguide. For the second version of the MMIC PA, a dipole CPW-to-waveguide transition was designed. The orientation of the dipole probe allows the MMIC to be inserted into the WR4.3 waveguide as shown in Fig. 4.18a. Because the chip is larger than the waveguide aperture, the final diced MMIC will have the notched profile as in Fig. 4.21. The simulated S-parameters of the transition are shown in Fig. 4.19. The simulated $|S_{21}|$ of the probe is 0.6 dB and the input match is $<$ -12 dB from 220 to 250 GHz, which greatly exceeds the bandwidth of the PA.



(a) (b)

Figure 4.18: a) Simulation view of the dipole probe for CPW-to-waveguide transition. b) Detail of the dipole transition. The dipole is approximately 1λ at 235 GHz.

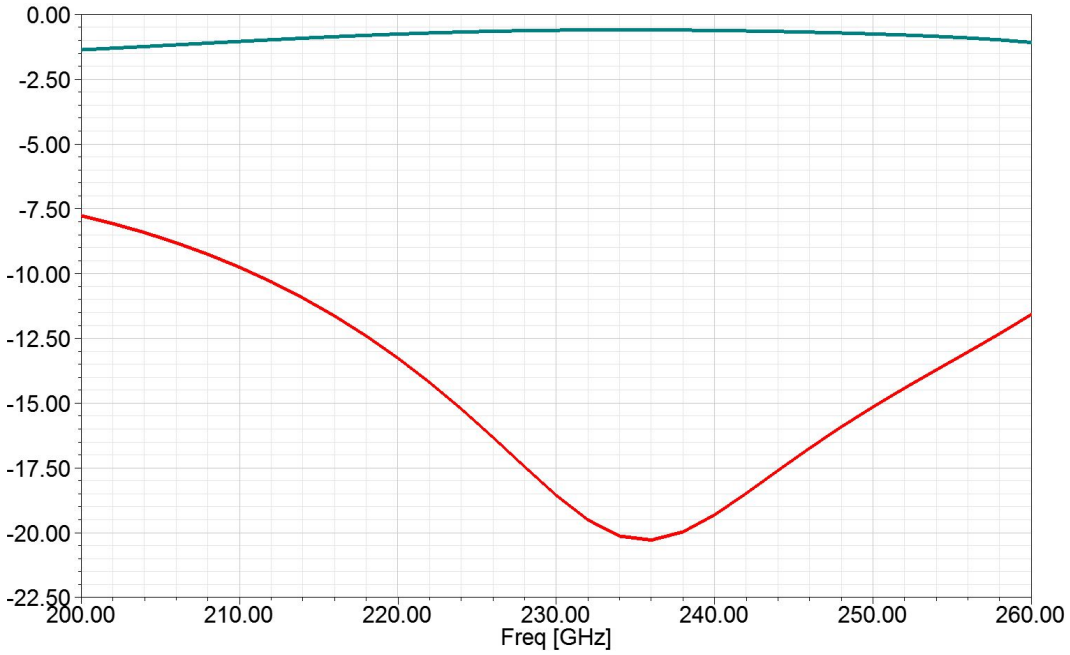


Figure 4.19: S-parameters of the CPW-to-waveguide transition. $|S_{21}|$ dB is in green and $|S_{11}|$ dB in red.

The final layout for the 8-way power combined 3-stage and 8-way power combined 4-stage PAs are shown in Figs. 4.20, 4.21.

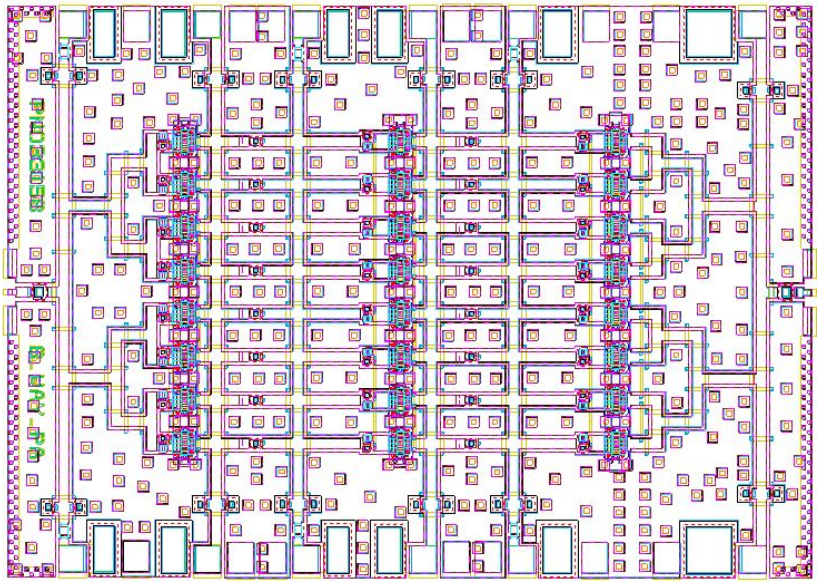


Figure 4.20: Layout view of the 3-stage 8-way combined PA. The MMIC dimensions are 2.2x1.65 mm^2.

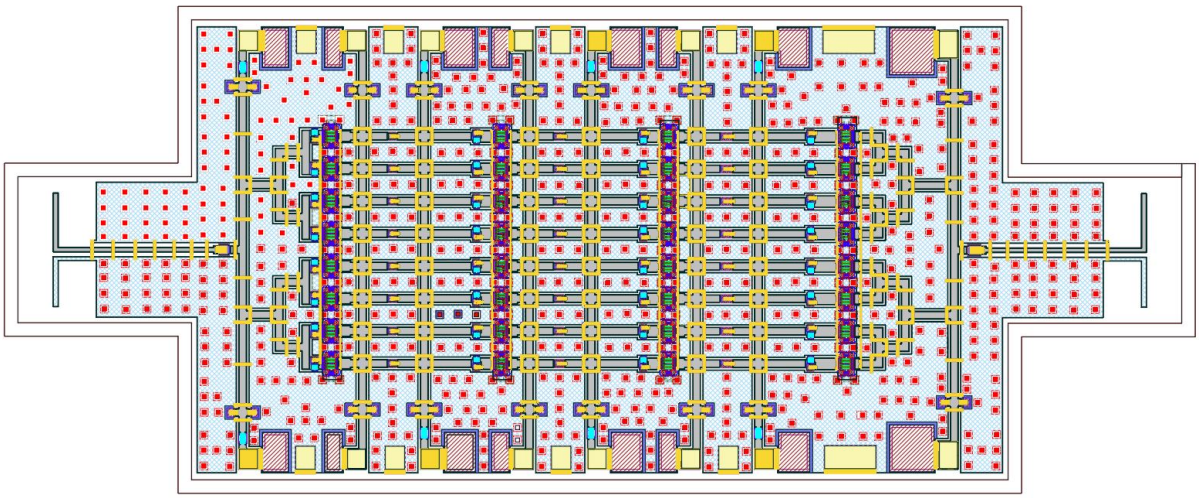


Figure 4.21: Detailed layout view of the 4-stage 8-way combined PA with CPW-to-waveguide transitions on input and output. The MMIC dimensions are 4.4x1.8 mm^2.

4.4 Measurements and Conclusion

The microphotograph of the fabricated 3-stage 8-way combined PA is shown in Fig. 4.22. Measurements of the PA S-parameters were performed at HRL with WR4.3 waveguide probes and VDI, Inc. WR4.3-VNAX frequency extenders. Due to the high frequency of operation, a maximum input power of -6 dBm was used and the measurements represent small signal operation.

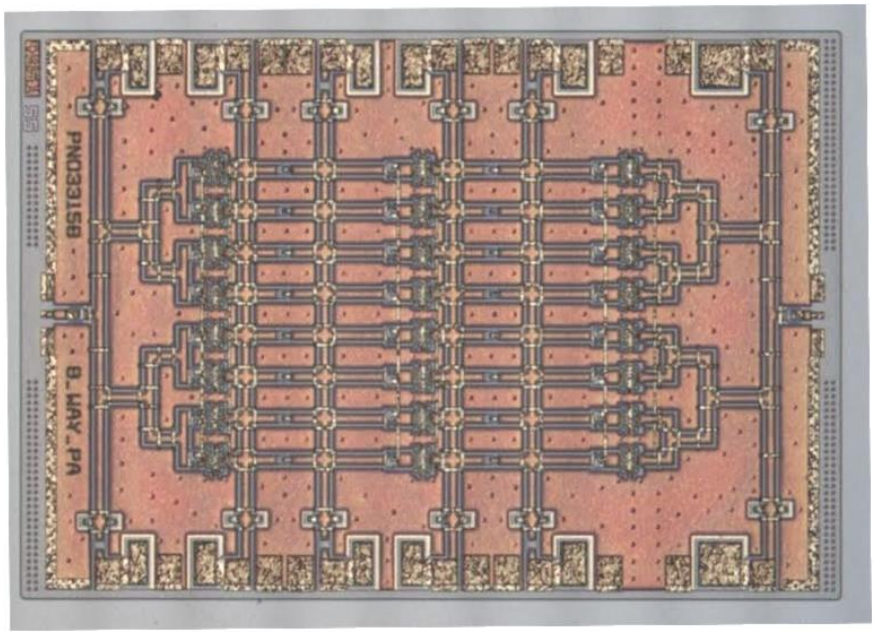
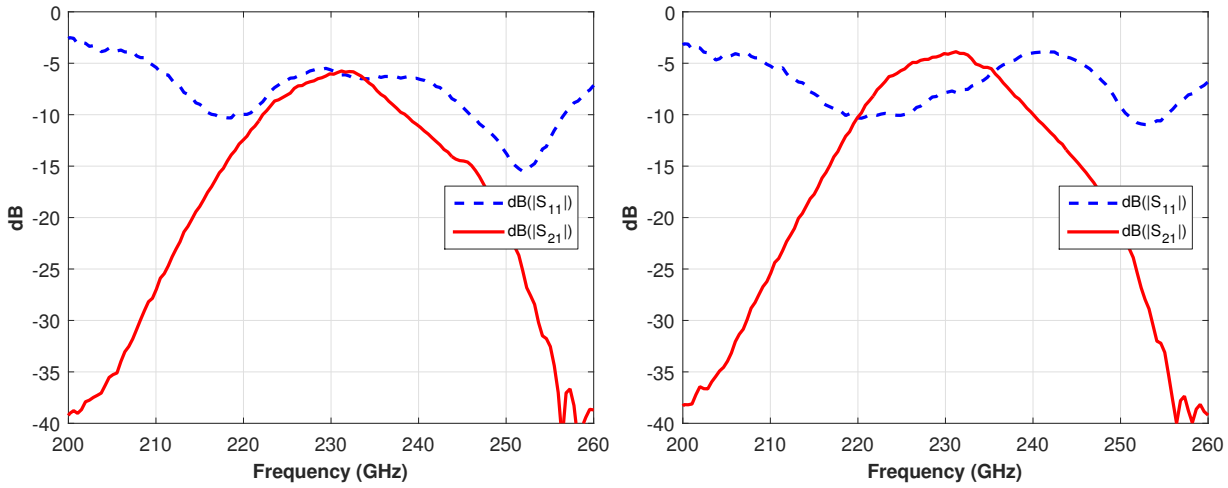


Figure 4.22: Microphotograph of the fabricated 3-stage, 8-way combined MMIC PA. The MMIC dimensions are 2.2x1.65 mm^2.

The S-parameters of two copies of the PA is are shown in Fig. 4.23a and 4.23b. Measurements across wafers and between other wafers showed good agreement but the f_T of the 4x20 μm device was lower than predicted by the model. The $|S_{11}|$ shape and magnitude in the measured results matches the simulated performance but the amplifier gain is much lower. Shown in Fig. 4.24 is the simulated EM networks cascaded with the measured S-parameters of the 4x20 μm device. The gain in this simulation is not low as in the measured results but a large spike in $|S_{11}|$ at 78 GHz is predictive of an oscillation. Because of the use of waveguide probes in the measurement, it is not possible to measure or prove this oscillation.



(a) (b)

Figure 4.23: Measured $|S_{11}|$ dB and $|S_{21}|$ dB for the 3-stage, 8-way combined PA. $|S_{11}|$ is shown in dashed lines.

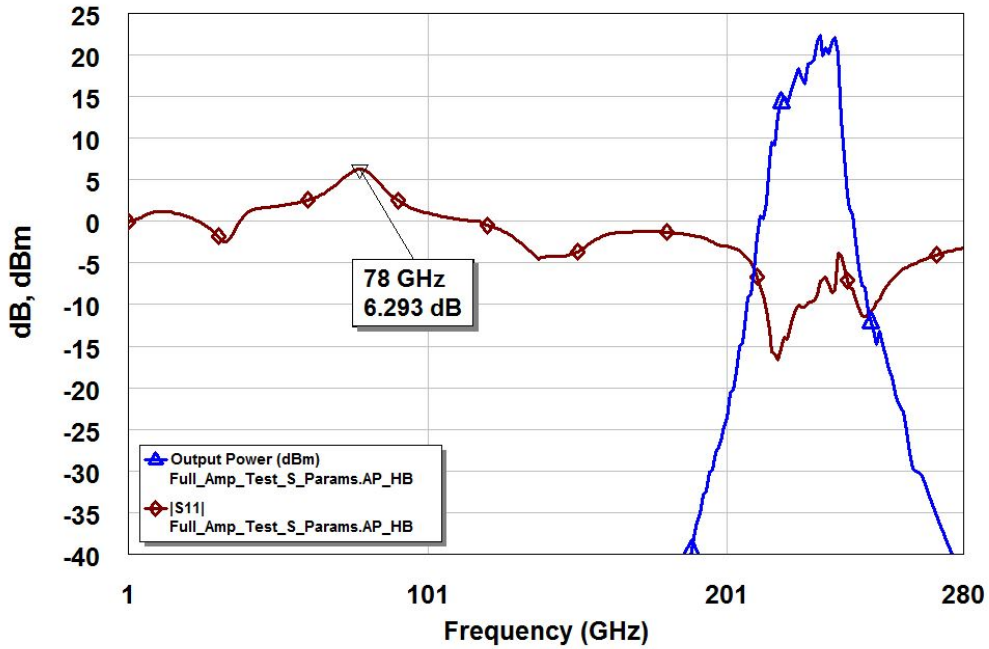


Figure 4.24: The $|S_{11}|$ dB (brown) and $|S_{21}|$ dB (blue) for the 4-stage amplifier with the 4x20 μm S-parameters. There is a significant positive $|S_{11}|$ at 78 GHz and this is indicative of an out of band oscillation.

4.5 Contributions from This Chapter

The specific contributions to the field from this chapter are as follows:

- Demonstrated analysis and design of a 235 GHz GaN power combined PA in CPW.
- Demonstrated power combiner analysis technique using even-odd mode decomposition in a 8-way power combiner. This technique is also compatible with the dual-injection stability analysis to detect odd-modes of oscillation in power combiners.

Acknowledgment: This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

Disclaimer: The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

Chapter 5

Stability Analysis in Microwave Circuits

Contents

5.1 Introduction to Stability Analysis in Microwave Circuits

Results from the previous chapters have shown the importance of ensuring microwave amplifier stability, yet a reliable analysis is not well known to most designers. Circuit stability is especially important for single-stage, multistage, and power combined MMIC PAs as fabrication is expensive and the circuits are difficult or often impossible to modify. The drive for higher power, efficiency, and operating frequency, while maintaining or improving linearity in solid state transmitters has resulted in increased design complexity at the MMIC level, adding to the difficulty of stability analysis. A simplified typical MMIC design flow is shown in Fig. 5.1. The arrow in the

reverse direction signifies the iterative process that is encountered in simulation and design, and shows where the proposed stability analysis technique developed in this chapter is performed.

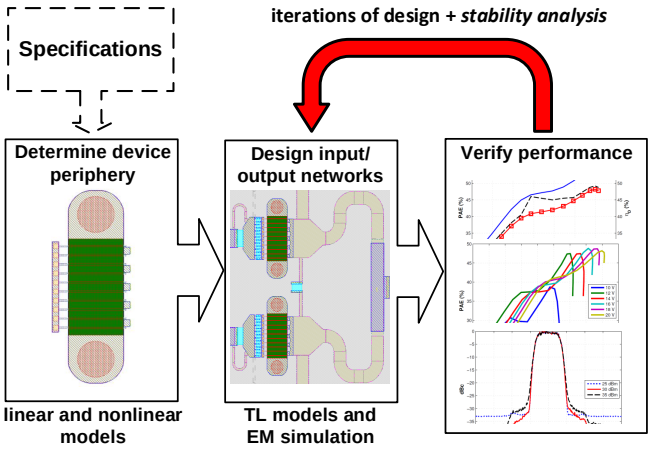


Figure 5.1: Typical MMIC PA design flow. The boxes represent a step in the process with the additional text representing what tools and methods are used to achieve the step.

In the traditional analysis of amplifier stability, most circuit designers resort to linear techniques implemented in standard circuit simulators, such as the well known K-factor [88]. Other techniques are essentially small-signal approaches that are modified or adjusted by designers to attempt to make them suitable for nonlinear and multistage designs [89–93]. These techniques are widely used despite the fact that multiple sources in the literature highlight their pitfalls, with experimental validation [94], [90]. A concise summary of the necessary conditions for validity regarding these modified small-signal approaches is given in [95].

The most commonly accepted and utilized approach by microwave amplifier designers seems to be to inject an ideal voltage or current source somewhere in the circuit and analyze the return ratio, similar to classical loop gain analysis introduced in [96]. An expression for the loop transfer function is then approximated and sometimes further analyzed using numerical methods and/or pole zero cancellation [97–101]. One of these methods is implemented in a commercial tool [102,103] and is gaining popularity despite being a proprietary and expensive software package. A widely used technique is detailed in [90] and [9], and a two-transistor ring oscillator is analyzed both with

K-factor and the introduced method, the normalized determinant function (NDF). The example from [9] is shown below as an introduction to multiple-transistor stability analysis and to highlight the problems in using the K-factor.

As described in [88] and used in popular circuit simulation software, the necessary and sufficient conditions for unconditional stability in a two-port network are that $K > 1$ and $B_1 > 0$ where K and B_1 are defined as:

$$K = \frac{1 - (|S_{11}|)^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{5.1}$$

$$B_1 = 1 + (|S_{11}|)^2 - |S_{22}|^2 - |\Delta|^2 \tag{5.2}$$

and $\Delta = S_{11}S_{22} - S_{12}S_{21}$. The K-factor analysis is not complete because it fails when the circuit contains poles with positive real parts. As proposed in [90], the proper stability criterion regarding the K-factor is that stable networks without poles in the right half plane (RHP) will remain stable if $K > 1$ and $B_1 > 0$, regardless of loading on the input and output ports. The proposed stability criterion for the K-factor technique limits its use for microwave amplifiers. To further explore this idea, the test circuit in Fig. 5.2 is analyzed with both K-factor and the normalized determinant function (NDF). The test circuit is a two-transistor ring oscillator and is either stable or unstable depending on source and load parameter values. The devices have different transconductances, g_{m1}, g_{m2}, because they are discrete devices. However, the determinant of the y-matrix of the network is solved directly and reveals two complex poles in the RHP. Since the location of these poles is known analytically for the simple test circuit, the NDF and the K-factor methods are validated by applying the Nyquist stability criterion on the known transfer function. The NDF is defined as:

$$NDF = \frac{\Delta(s)}{\Delta_0(s)} \tag{5.3}$$

where $\Delta(s)$ is the determinant of the circuit being analyzed and $\Delta_0(s)$ is the determinant of the same circuit with all dependent sources set to zero. The circuit is stable if the NDF encircles the origin of the polar plot more times clockwise than counterclockwise. For simple circuits like the one in Fig. 5.2, encirclement of the origin indicates instability. In Figs. 5.3a - 5.6a the NDF is

plotted from 0.1 to 100 GHz for various circuit parameters, given in Table 5.1. The NDF is plotted over a large frequency range to demonstrate the general behavior of the function. The test circuit oscillates at approximately 1.4 GHz and the K-factor plots are detailed in that range.

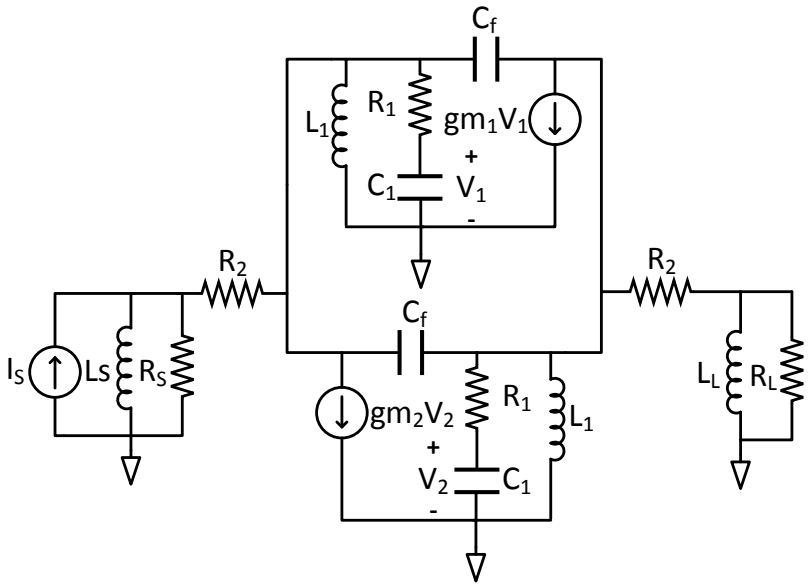
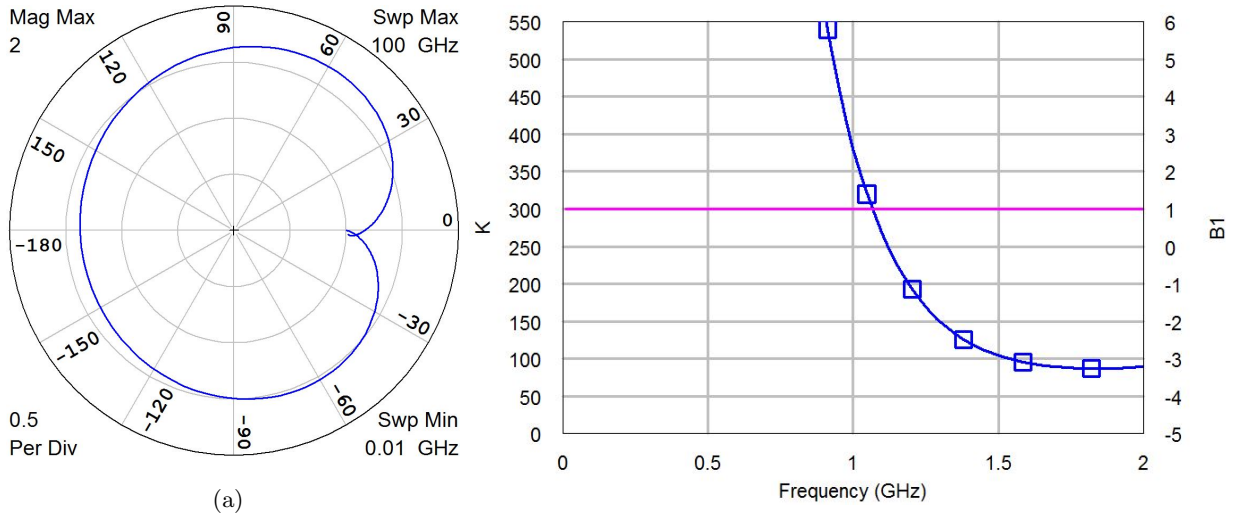


Figure 5.2: Two-transistor ring oscillator in [9]. Components with fixed values: $R_1 = 10\,\Omega$, $L_1 = 560\,\text{pH}$, $g_{m1} = 500\,\text{mS}$, $g_{m2} = 400\,\text{mS}$, $C_f = 0.1\,\text{pF}$, $C_1 = 16\,\text{pF}$.

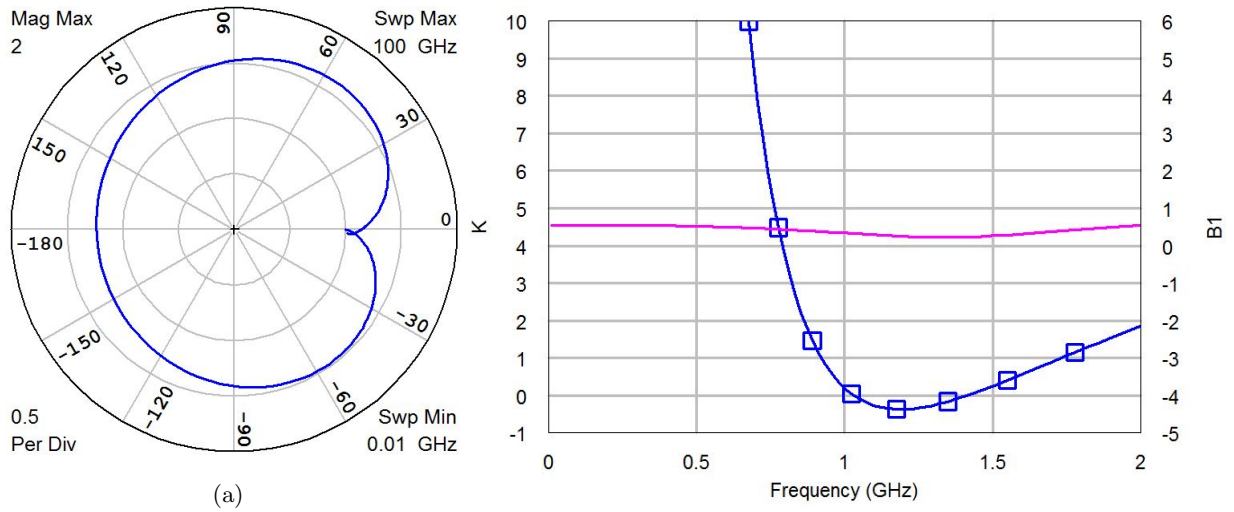
Table 5.1: Ring Oscillator Circuit Parameters

Case	$R_s\,(\Omega)$	$L_s\,(\text{pH})$	$R_L\,(\Omega)$	$L_L\,(\text{pH})$	$R_2\,(\Omega)$
I	50	0	50	5	50
II	50	0	50	5	5
III	6.666	500	10	1250	5
IV	20	500	10	1250	5



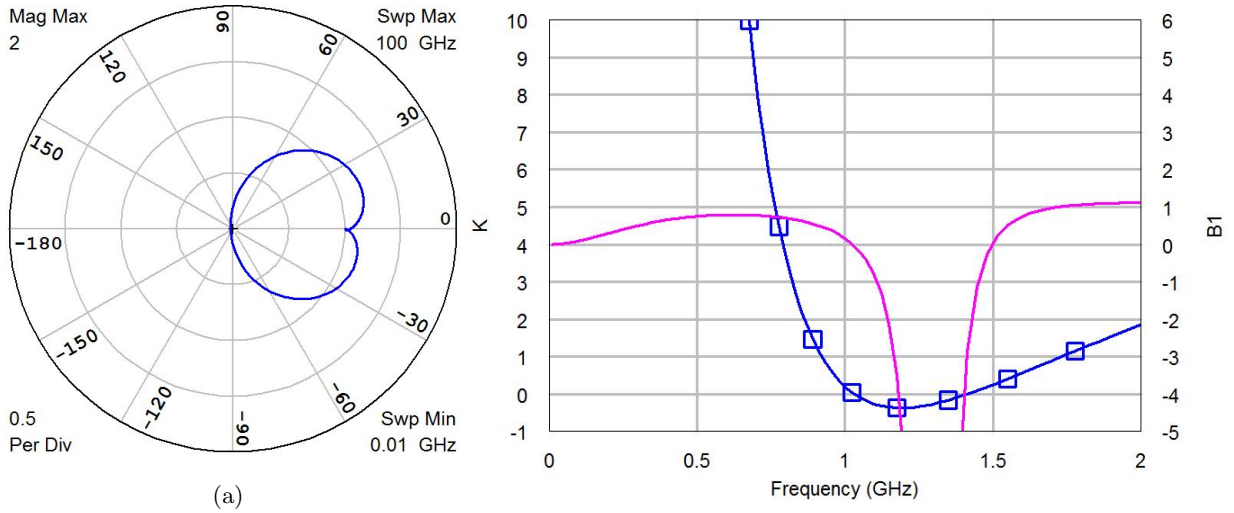
(a) (b)

Figure 5.3: (a) Polar plot of the NDF for case I from Table 5.1. (b) K (blue-square) and B_1 (pink) for case I. The NDF correctly predicts instability and the K-factor incorrectly predicts stable behavior.



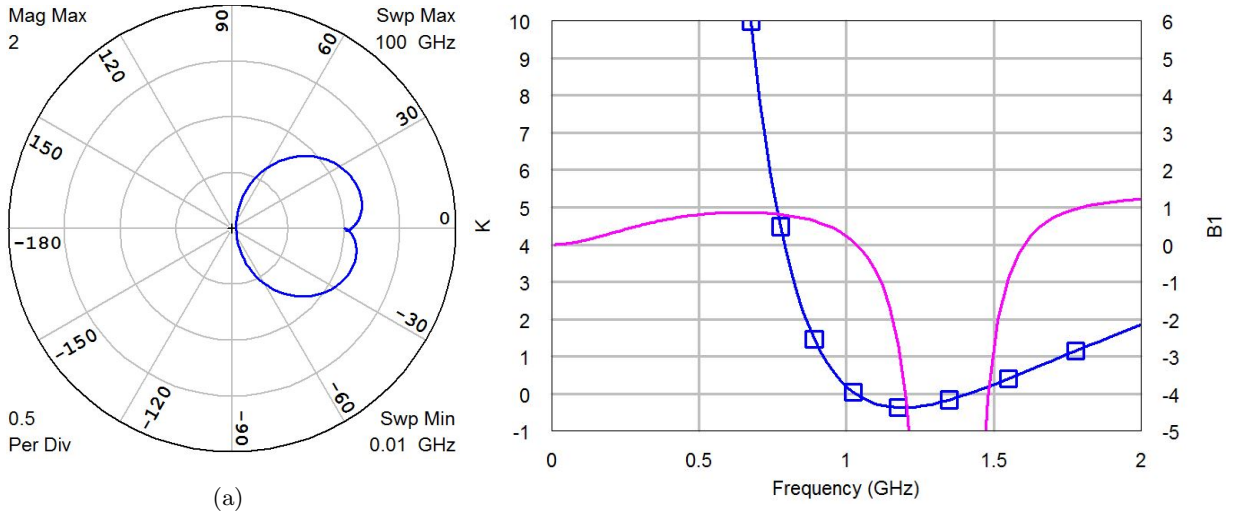
(a) (b)

Figure 5.4: (a) Polar plot of the NDF for case II in Table 5.1. (b) K (blue-square) and B_1 (pink) for case II. The NDF correctly predicts instability and the K-factor correctly predicts unstable behavior.



(a) (b)

Figure 5.5: (a) Polar plot of the NDF for case III (b) K (blue-square) and B_1 (pink) for case III. The NDF correctly predicts instability and the K-factor correctly predicts unstable behavior.



(a) (b)

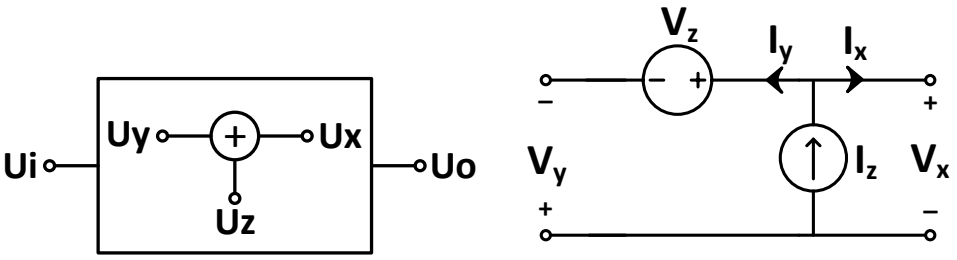
Figure 5.6: (a) Polar plot of the NDF for case IV (b) K (blue-square) and B_1 (pink) for case IV. The NDF correctly predicts stability and the K-factor incorrectly predicts unstable behavior.

In cases I, II and III from Table 5.1, the circuit is unstable and the NDF predicts this by encircling the origin. In case IV, the circuit is stable and the NDF predicts this with no encirclement of the origin. In contrast, the K-factor has varied results. In case I, the K-factor incorrectly predicts no

oscillation and in case IV incorrectly predicts oscillation. False positives are an acceptable problem in this type of analysis but false negatives are not. While it is shown above that the NDF can predict oscillatory behavior, there are several limitations. First, the definition of the NDF requires the network to be analyzed by setting the dependent sources to zero in the $\Delta_0(s)$ determinant, which is not possible with black box large signal transistor models. Small signal transistor models that are proprietary will also not allow access to the dependent sources in the equivalent circuit. Second, the NDF analysis requires calculations of the determinant of very large networks in power combined and multi-transistor circuits. The authors of [90] propose a reduced form of the NDF that allows for complex circuits with multiple dependent sources to be analyzed by reducing the networks. This method still requires knowledge of the equivalent circuit that is not normally known in microwave or MMIC design. A technique that does not contain these limitations and that can be easily implemented in modern circuit simulators as part of the design process is the topic of the remainder of this chapter.

5.2 A General Technique for Stability Analysis of Microwave PAs

The stability analysis technique presented in this chapter is based on the technique of double null injection from [104] and [105], which is an extension of the initial work by the same author in [96]. The General Feedback Theorem (GFT) in [105] is based around a linear network model as shown in Fig. 5.7. U_i and U_o are the input and output signals (either current or voltage), respectively, of the network. The injection point, somewhere inside the network, is represented by the summing junction with U_z being the injected signal. Upon injection of U_z, two dependent signals, U_y and U_x are generated.



(a) (b)

Figure 5.7: (a) Network diagram with injection source. (b) Injection source template used in this paper. U_z will be V_z or I_z for voltage or current injection, respectively.

From the diagram and injection source template in Fig. 5.7, and assuming x_1, x_2 and y_1, y_2 are arbitrary constants that describe the linear network, several governing equations can be written as follows:

$$U_z = U_x + U_y \tag{5.4}$$

$$U_y = y_1 U_i + y_2 U_z \tag{5.5}$$

$$U_x = -y_1 U_i + (1 - y_2) U_z \tag{5.6}$$

$$U_o = x_1 U_i + x_2 U_z \tag{5.7}$$

By using (1-4) and nulling each signal in Fig. 5.7 in turn one obtains five auxiliary equations:

$$A = \left.\frac{U_o}{U_i}\right|_{U_z=0} = x_1 \tag{5.8}$$

$$B = \left.\frac{U_y}{U_x}\right|_{U_i=0} = \frac{y_2}{1 - y_2} \tag{5.9}$$

$$C = \left.\frac{U_o}{U_i}\right|_{U_y=0} = x_1 - x_2 \frac{y_1}{y_2} \tag{5.10}$$

$$D = \left.\frac{U_o}{U_i}\right|_{U_x=0} = x_1 + x_2 \frac{y_1}{1 - y_2} \tag{5.11}$$

$$E = \left.\frac{U_y}{U_x}\right|_{U_o=0} = \frac{x_1 y_2 - x_2 y_1}{x_1 - (x_1 y_2 - x_2 y_1)} \tag{5.12}$$

Equation (5.8) can be rewritten in terms of (5.9) - (5.12) as:

$$A = C \frac{B}{1 + B} + D \frac{1}{1 + B} \tag{5.13}$$

The general result of (5.13) is the basis for the feedback analysis used in this work. When the error signal summing point is selected as the injection point, (5.13) represents the closed-loop system transfer function. Other system quantities, the loop gain (5.9), ideal forward gain (5.10), direct forward transmission function (5.11), and null loop gain (5.12), to be defined, also follow from this choice of injection point. It is important to clarify two concepts here. First, the analysis is linear under the assumptions that it is performed under large signal excitation and that the injected signal is small enough in magnitude as to not disturb the nonlinear operating point. This weak-nonlinear assumption is valid for a wide range of designs that operate in the Class A - Class B region. Second, the choice of injection point is important because secondary loops that do not represent the main feedback path or mechanism do not predict circuit stability.

In modern circuit simulators, the node voltages or loop currents may not be readily known and in harmonic balance (HB) analysis, there is no simple way to enforce the nulling conditions required to obtain (5.8) - (5.12). An insightful solution to this issue in time-domain circuit simulators is partially described in an unpublished tutorial found in [106] and is here expanded and adapted for use in HB type circuit simulators. The key to this analysis is to perform three simulations of the circuit under test with different small-signal source states while retaining large-signal excitation, and therefore circuit operation, from a different source, as stated earlier. The voltage and current harmonic components are then measured at the appropriate nodes in the circuit. These voltage and current harmonic components contain the magnitude and phase information of selected harmonics and are used in conjunction with the RF input source magnitude and phase information to form the first and second order transfer functions. For the first simulation, V_z is enabled, U_i is disabled and I_z is disabled. This first simulation and the necessary other two are described below:

$$\mathit{Simulation}\ 1 : V_z = 1, U_i = 0, I_z = 0$$

$$\mathit{Simulation}\ 2 : U_i = 1, V_z = 0, I_z = 0$$

$$\mathit{Simulation}\ 3 : I_z = 1, U_i = 0, V_z = 0$$

To obtain a result for (5.10), the U_y signal (V_y or I_y) must be set to zero. For the injection source

of Fig. 5.7, there are two y-signal components, V_y and I_y, and from superposition can be written as:

$$V_y = \alpha V_{y1} + \beta V_{y3} + V_{y2} \tag{5.14}$$

$$I_y = \alpha I_{y1} + \beta I_{y3} + I_{y2} \tag{5.15}$$

where the $y1$, $y2$ or $y3$ subscripts correspond to simulation states 1, 2 or 3, respectively, and α and β are again arbitrary constants that describe the network. The α and β values will be manipulated to enforce the necessary conditions of (5.10), $U_y = 0$ and by extension, V_y and $I_y = 0$. Solving the system of equations shown in (5.14) and (5.15) gives:

$$\alpha = \frac{V_{y3}I_{y2} - V_{y2}I_{y3}}{V_{y1}I_{y3} - V_{y3}I_{y1}} \tag{5.16}$$

$$\beta = \frac{V_{y1}I_{y1} - V_{y1}I_{y2}}{V_{y1}I_{y3} - V_{y3}I_{y1}} \tag{5.17}$$

Equation (5.10) can now be evaluated by summing the responses of the network with no injection, current injection only and the voltage injection only as shown below,

$$C = \left.\frac{U_o}{U_i}\right|_{U_y=0} = V_{out_2} + \alpha V_{out_3} + \beta V_{out_1} \tag{5.18}$$

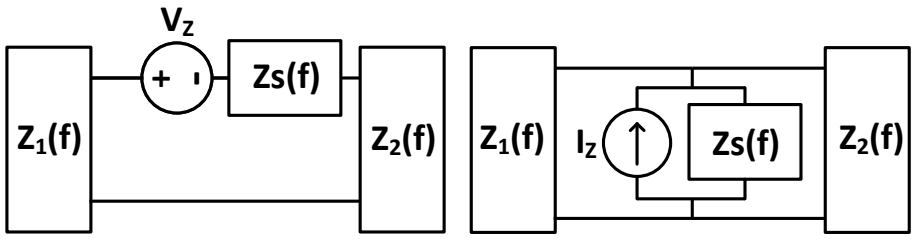
By further use of (5.8) - (5.11), similar systems of equations are created and solved. The primary equation of interest for this work is (5.9), the loop gain, with (5.10) and (5.12) used to validate the simulation.

After the loop gain transfer function is synthesized, the magnitude and phase results are plotted and Nyquist criterion is applied [107]. ($1 \angle 180\ ^\circ$) crossings are points of potential instabilities but the designer must decide how close to these crossings is acceptable. Transfer function analysis using Nyquist stability criterion is traditionally plotted in a polar fashion but it is more intuitive here to plot the loop gain responses in a rectangular format over frequency and output power. In this paper, the criterion for a potential instability is the loop gain magnitude exceeding 0 dB with the phase crossing $180\,^\circ$. Pole zero identification is not used in this work because an analytic expression for the transfer function would be a further approximation. Because Nyquist

stability criterion is essentially a mathematical test that finds if poles of the transfer function lie in the right half plane, the final analysis results of this technique and methods that synthesize a polynomial transfer function are similar.

5.2.1 Comparison to Single-Injection Analysis

Widely used stability analysis techniques described in the literature rely on single-injection voltage or current test sources, and here the dual-injection method is compared to a current injection test. A typical setup for each type of single injection is shown in Fig. 5.8 with V_z or I_z being the injection source, Z_s the source impedance and Z_1 and Z_2 the impedances of the equivalent networks to the left and right of the injection location, respectively. There are two important conditions for the single injection technique, first that the injection point resides inside the feedback loop, and second that the injection does not significantly change the impedances seen on either side of the injection location. A good summary of the impedance relationship between $Z_1(f)$ and $\mathrm{Z}_2(f)$ necessary at the injection point and other practical issues is given in [108] and states that for current injection $Z_1(f) \gg Z_2(f)$ and for voltage injection $Z_1(f) \ll Z_2(f)$. The problem of ensuring that the injection source is located inside the feedback loop is solved by selecting multiple injection sites and performing the analysis multiple times while monitoring the response, this approach is recommended by the authors of [102]. The second condition, the impedance relationship, is more difficult to enforce because the impedances change over frequency and input drive level in an unknown way. Furthermore, there is no clear indication when the injection point, and by extension the stability analysis, is incorrect.



(a) (b)

Figure 5.8: Single source injection schemes, (a) voltage injection and (b) current injection. The impedances to the left and right of the injection location are frequency and possibly input drive dependent.

An example of this problem is given in Fig. 5.9. This FET model is similar to a GaN HEMT model described in [1], and the same element values are used for simulation. The model is first analyzed without R_i and the C_{GD} and C_{GS} capacitors.

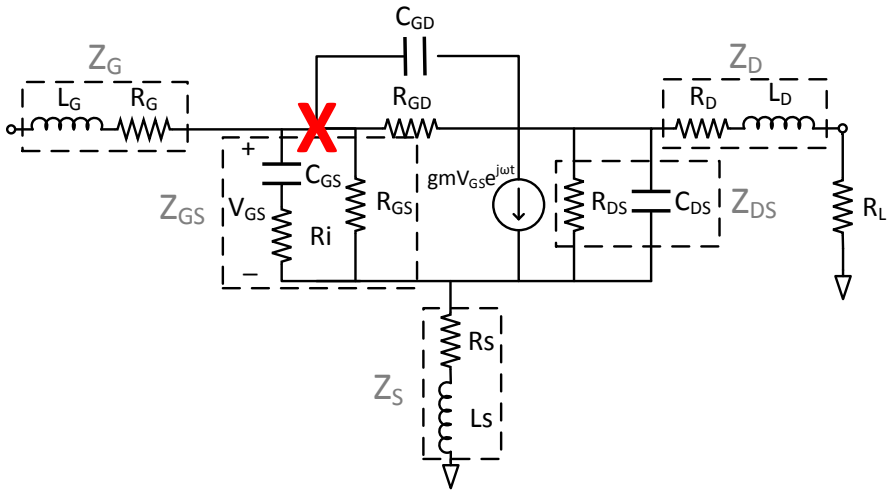
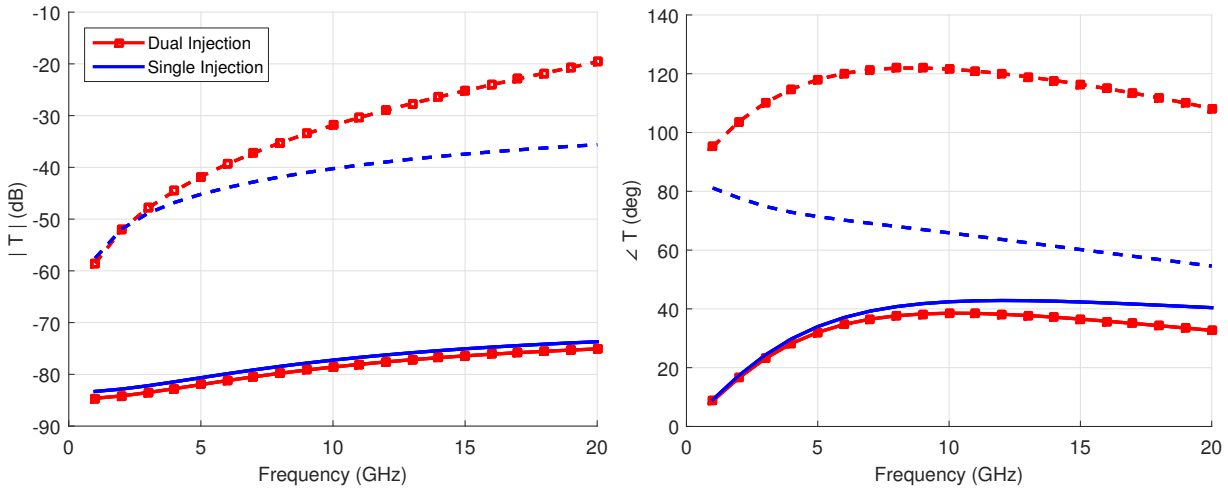


Figure 5.9: Small signal HEMT model with lead parasitics, C_{GD} and C_{GS} and parasitic paths R_{GS}, R_{GD} and R_{DS}. The current source injection location is at the node connecting R_{GD} to R_{GS}, marked with a red X. The simulation is performed first without and later including C_{GD}, C_{GS}, and R_i.

The loop gain magnitude (Fig. 5.10a) and phase (Fig. 5.10b) are shown in solid lines for the single

and dual-injection case and show close agreement. The impedance relationship between $Z_1(f)$ and $Z_2(f)$ is shown in the top half of Fig. 5.11 and shows that for current injection at the selected injection location, $Z_1(f) \gg Z_2(f)$, predicting accurate results. The network response with the addition of parasitics C_{GD}, C_{GS} and R_i is analyzed next. These capacitors and the parasitic resistance alter the impedance relationship at the injection location as shown in the bottom half of Fig. 5.11.



(a) (b)

Figure 5.10: Loop gain magnitude (a) and phase (b) for single and dual-injection with C_{GD}, C_{GS}, and R_i (dashed line) and without (solid line).

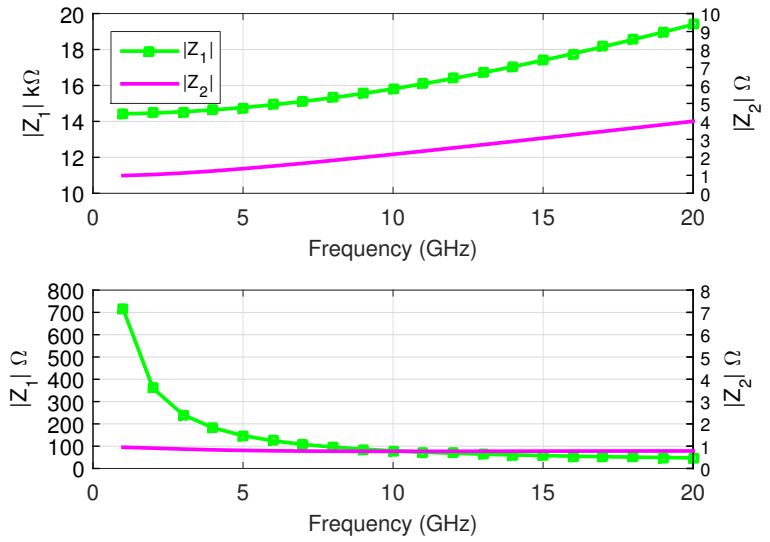


Figure 5.11: Impedance relationship for the FET model without (top) and with C_{GD}, C_{GS}, and R_i, (bottom) of the left (Z_1) and right (Z_2) networks at the injection plane for single current source injection.

The FET model with C_{GD}, C_{GS} and R_i is analyzed at the same injection location and the resulting loop gain and phase for single injection and dual-injection is shown in Fig. 5.10a and 5.10b. The loop gain magnitude and phase deviation between single and dual-injection for this circuit is now >12 dB with more than 50 degrees. These results show that the single injection and dual-injection techniques diverge but do not prove that dual-injection is correct. To show that the dual-injection loop gain results are correct, it is useful to look at some of the other transfer functions resulting from (5.8) - (5.12) and interpret their meaning.

Consider the network of Fig. 5.12 as an alternative to the classical feedback structure consisting of only a forward gain path and a feedback path. This network allows for a signal to travel from input to output through the feedback network and is the general model used in [104] and [105].

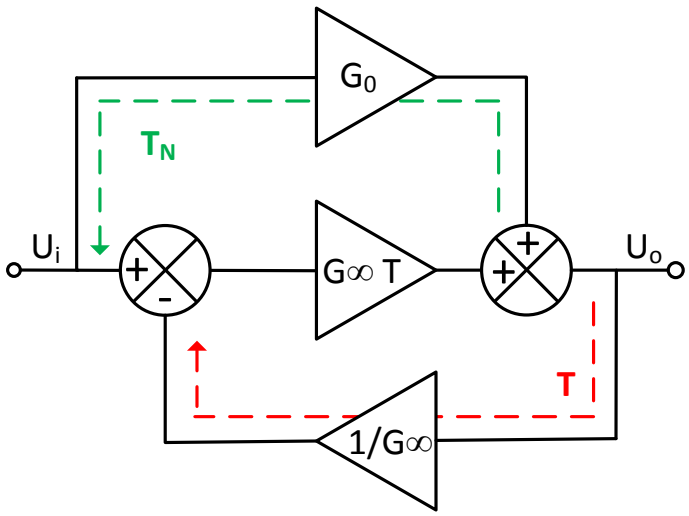


Figure 5.12: Alternative feedback model. The additional path for forward transmission is a result of the GFT.

By use of (5.8) - (5.12), (5.13) can be rewritten as:

$$A = C\frac{1+\frac{1}{E}}{1+\frac{1}{B}} \tag{5.19}$$

When the injected signal is placed inside the feedback loop and oriented to align I_y or V_y with the feedback or error signal, then (5.8) - (5.13) take on the values shown in Fig. 5.12 and (5.19) is written as:

$$G = G_\infty\frac{1+\frac{1}{T_n}}{1+\frac{1}{T}} \tag{5.20}$$

Since the closed loop transfer function, G, can be determined in a straightforward way, G_∞ and T_n can be used to validate the loop gain via (5.20). The first quantity, G_∞, is the ideal closed loop gain and is determined by adjusting the injected signal to a point that the error signal fed back into the forward gain path is nulled. By letting the source impedance $Z_S \Rightarrow 0$, a simplified expression for G_∞ is obtained:

$$G_\infty = Z_{DS}||Z_f \cdot \frac{-g_m R_L Z_{GS}}{Z_G[(R_L+Z_D)+\frac{Z_{DS}Z_f}{Z_{DS}+Z_f}+\frac{g_m Z_{GS}Z_{DS}(Z_D+R_L)}{Z_{DS}+Z_f})]} \tag{5.21}$$

with $Z_{GS} = R_{GS}||(Ri+\frac{1}{j\omega C_{GS}})$, $Z_G = j\omega L_G + R_G$, $Z_D = j\omega L_D + R_D$, $Z_S = j\omega L_S + R_S$, $Z_{DS} = R_{DS}||\frac{1}{j\omega C_{DS}}$ and $Z_f = R_{GD}||\frac{1}{j\omega C_{GD}}$ as in the dashed boxes in Fig. 5.9.

Without the nonlinear C_{GS}, Z_{GS} is orders of magnitude larger than other quantities ($R_{GS} = 70\,M\Omega$, $R_{GD} = 100\,k\Omega$, $R_G \approx R_S \approx R_D \approx 1$) and by rearranging terms, a far simpler, approximate expression is obtained:

$$G_\infty = \frac{-Z_f}{Z_G + \frac{Z_G}{R_L}} \tag{5.22}$$

This expression conveys the physical meaning of G_∞, it is the ideal closed loop gain of the network and similar to the well known gain expression of an inverting op-amp. In contrast, the null loop gain, (5.12), describes the non-idealities of the network. This transfer function is:

$$T_n = \frac{Z_f(Z_S - Z_{GS}Z_{DS}g_m)}{Z_{GS}(Z_S + Z_{DS} + Z_S Z_{DS}g_m) + Z_S Z_{DS}} \tag{5.23}$$

If $Z_S \Rightarrow 0$, then the null loop gain is simply $-g_m Z_f$, an expression that represents the signal path through the gain element and back through the non-ideal forward signal path of Fig. 5.12. For T_n, it is also interesting to look at the simplified result when $Z_S \neq 0$ and C_{GS} and R_i are not removed from the model. Since $Z_f Z_S \ll Z_f R_{GS} Z_{DS} g_m$, T_n reduces to:

$$T_n = \frac{-g_m Z_f}{1 + g_m Z_S + \frac{Z_S}{Z_{GS}}} \tag{5.24}$$

This expression shows the null loop gain accounts for the feedback behavior due to the source impedance (negative feedback) as well as the $R_{GD}||\frac{1}{j\omega C_{GD}}$ signal path. By using T, T_n, and G_∞ and (5.20), G is calculated and is identical to the directly-simulated closed loop transfer function (V_O/V_{IN}), proving that the dual-injection technique is valid with non-ideal injection locations.

5.3 Application to Single and Multiple Stage PA Stability Analysis

The goal of this work is to develop a tool that is easily implemented in existing microwave circuit simulators to allow instability predictions in MMICs during the design process. In this section, we present measured results from single and two-stage PA examples to test the technique.

5.3.1 Stability Example with a Commercial S-Band Amplifier

The CREE CGH40006P-TB GaN 6 W demo board shown in Fig. 5.13 is used to demonstrate the analysis technique. The gate bias line resistance is intentionally modified to make the amplifier

unstable. The injection point and output voltage node are chosen to be the gate and drain of the transistor, respectively. The results do not change if the output node is the RF output port. The transfer function, A in (5.8), is considered to be linear around a specific operating point. Since the design does not use intentional feedback, any loop gain above 0 dB is unwanted and may cause oscillations. The demo board is simulated from 50 to 6000 MHz in ADS to cover the designed operating bandwidth of the amplifier. The layout and element values were taken from the manufacturer's datasheet and a nonlinear model was provided.

In order to introduce instabilities in a controlled way, the gate bias resistor, nominally 150 Ω, is reduced and the resulting loop gain with values 150, 10, and 0 Ω is shown in Fig. 5.14. With 0 Ω on the bias line, there is a phase crossing of the loop gain at -180° and a gain margin of merely 0.4 dB. However, if one adds a resistor of 10 Ω, there is a gain margin of 5 dB. The nominal value of the resistor removes the peaking in the loop gain entirely with 20 dB of gain margin. To test the simulations, the gate bias line resistor is replaced with a 0Ω resistor and the device is biased. The gate voltage is set to the same value that would be needed for 100 mA of quiescent current with a stable amplifier (V_g=-2.7 V). The PA oscillates as shown in Fig. 5.15 with a fundamental tone at 686 MHz. The difference between the simulated and measured oscillation frequency is approximately 16 MHz or 2.4%. Next, the bias line resistor is replaced by a 10 Ω resistor. The amplifier showed no signs of oscillation under any bias condition or RF input power in both simulation, Fig. 5.14, or in measurement. The nominal 150 Ω resistor further increases the gain margin and also shows no signs of instability.

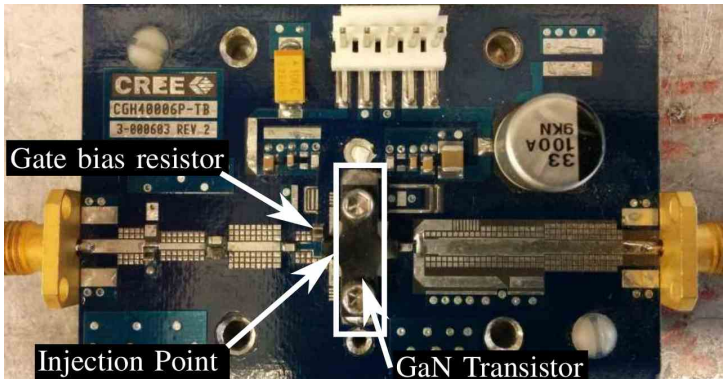


Figure 5.13: CREE demonstration board for the CGH40006P 6 W GaN transistor. The gate bias resistor was removed to cause the amplifier to become unstable.

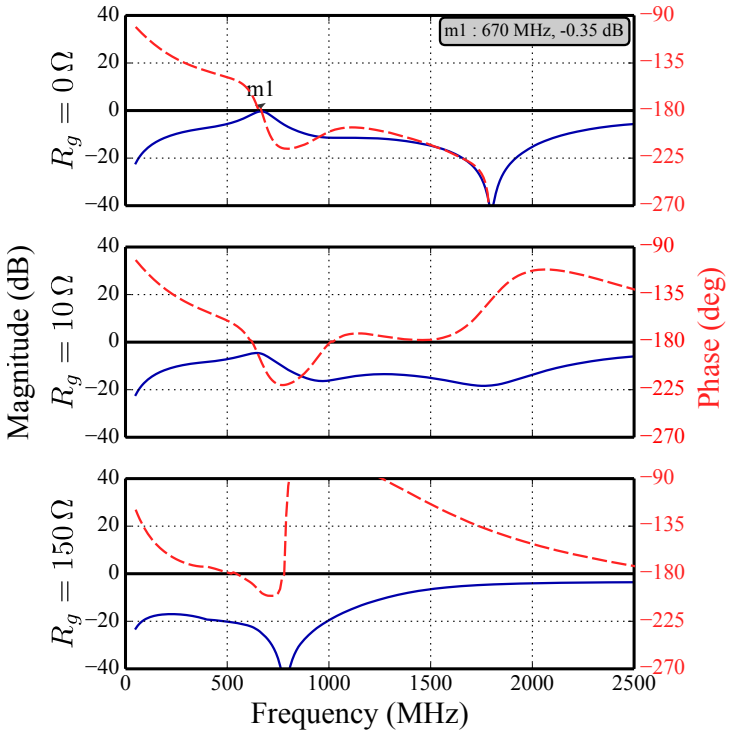


Figure 5.14: Simulated loop gain of the demonstration board at 0 dBm input power; magnitude (solid line) and phase (dotted line). With R_g=0 Ω, the phase passes through 180° at approximately 670 MHz while the amplitude is at -0.4 dB. This shows a high probability of oscillation. However, with R_g=10 Ω, the gain margin increases to 5 dB and a 150 Ω resistor eliminates the peaking in the loop gain.

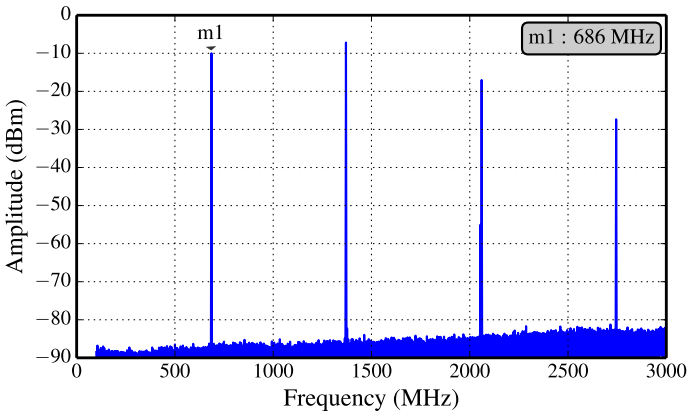


Figure 5.15: Measured power spectrum of the CREE development board. The frequency of oscillation is at 686 MHz with a bias of V_g=-2.7 V and a 0 Ω resistor on the gate bias line. The amplifier is designed to work from 500 MHz to 6 GHz and the harmonics of the oscillation are also visible at the output.

A commercially available stability analysis program that uses single current-source injection, AMCAD STAN [103], was utilized to validate the technique. In STAN, a large-signal harmonic balance analysis of the nonlinear circuit is performed and then linearized around an operating point. The resulting transfer function of the linearized circuit is expressed as:

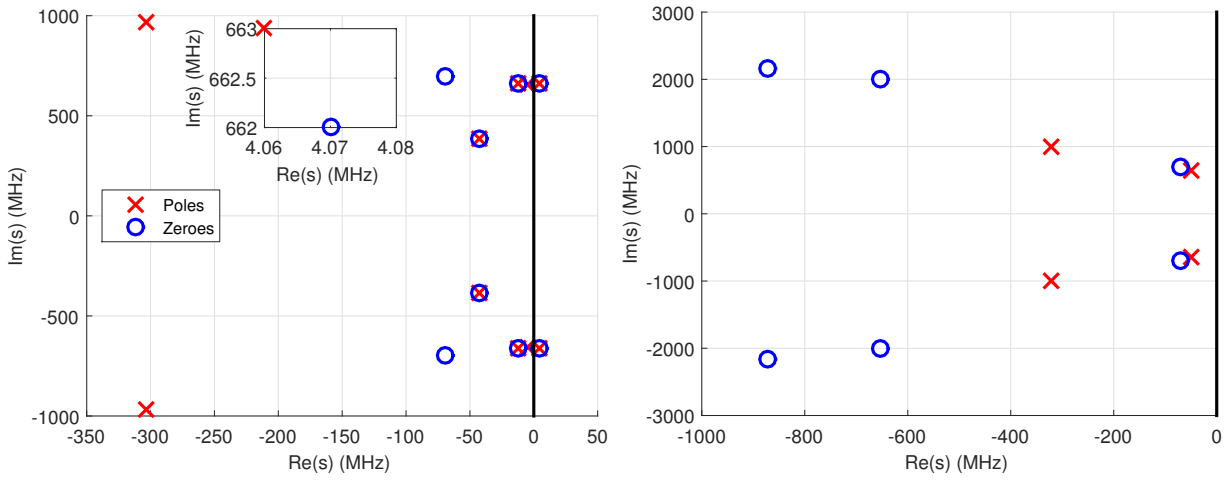
$$H(s) = \frac{v_{in}(s)}{i_{in}(s)} \tag{5.25}$$

where v_{in} and i_{in} are the voltage and current measured at the injection node. For power amplifier analysis, a small-signal sinusoidal current source is connected at the transistor gate terminal to generate the transfer function. A polynomial fit of this transfer function, $H(s)$ is found using frequency-domain identification algorithms, [103] and can be expressed as:

$$\hat{H}(s) = \frac{\prod_{i=1}^{N_z}(s - z_i)}{\prod_{i=1}^{N_\lambda}(s - \lambda_i)}$$

where z_i and λ_i are the zeros and poles of the closed loop transfer function. In general, the poles and zeros of a transfer function are complex and the system dynamics are represented graphically

by plotting their locations on the complex s-plane. In order for a linear system to be stable, all of the poles of its transfer function must have negative real parts. Complex poles always appear as conjugate pairs since they are the roots of a real polynomial. The resulting pole-zero plots of the amplifier transfer function are shown in Figs. 5.16a and 5.16b. Right half-plane (RHP) poles appear at 662 MHz for the case of the 0 Ω gate resistor (shown with a red cross), predicting an instability at that frequency. A zero, marked with a blue circle, is seen in close proximity to the pole and appears to cancel it. The inset shows that under closer inspection, however, the pole and zero do not overlap exactly and an instability is predicted. The existence of such quasi-cancellations requires the designer to examine the poles and zeros of the transfer function carefully. The 10 Ω gate resistor simulation predicts no RHP poles and both cases agree with the dual-injection technique and measured results.



(a) (b)

Figure 5.16: Pole-zero plots of the transfer functions of the CREE evaluation board with 0 Ω (a) and 10 Ω (b) gate resistors. The single injection technique identifies RHP poles at 662 MHz that are not canceled by the nearby RHP zeroes. The inset shows the quasi-cancellation.

It should be mentioned that the simulation time for the two methods is similar because while there are three separate simulations for the dual injection technique, there is also time spent on the analytic transfer function synthesis in STAN and the net difference in the analyses is negligible.

5.3.2 Stability Example with a Two-stage X-Band GaN MMIC

A two-stage GaN MMIC PA using the TriQuint 150 nm GaN process described in [45] was designed for 10 W peak power output power at 10 GHz, Fig. 5.17. The black-box nonlinear model used for design of the MMIC was unfortunately incorrect, resulting in the fabricated chip having unstable behavior. A stable mode of oscillation was found with the first stage gate biased at V_{g1}=-3.25 V, the second stage gate at V_{g2}=-3.6 V, and the drain voltages at 15 V. The spectrum, Fig. 5.18, shows an oscillation at 4.5 GHz.

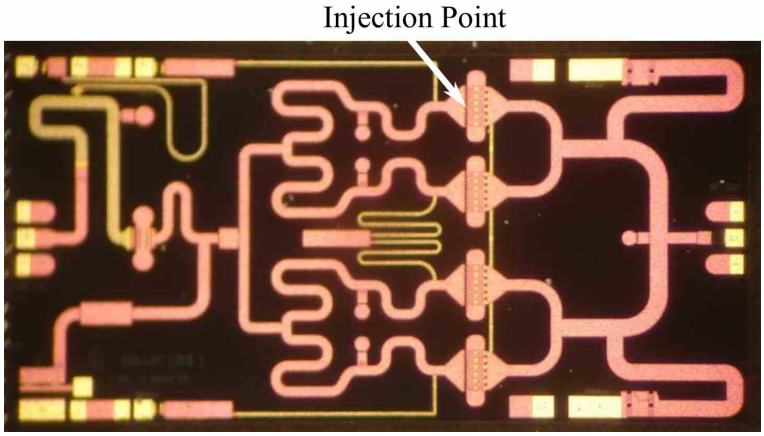


Figure 5.17: X-band two-stage GaN MMIC designed for 10 W that after fabrication, was found to be highly unstable. The chip is 4 mm × 2.3 mm. All devices are 12x100 μm.

To perform the post-fabrication diagnostics and stability analysis, a new device model was used and the circuit re-simulated in Keysight ADS. The injection node was chosen to be on the gate of one of the second stage transistors. The output measurement node was placed on the drain of the same transistor. As in the first example, the output measurement node could be placed on the output of the amplifier with similar results: any odd mode oscillations would be captured by the computed loop gain.

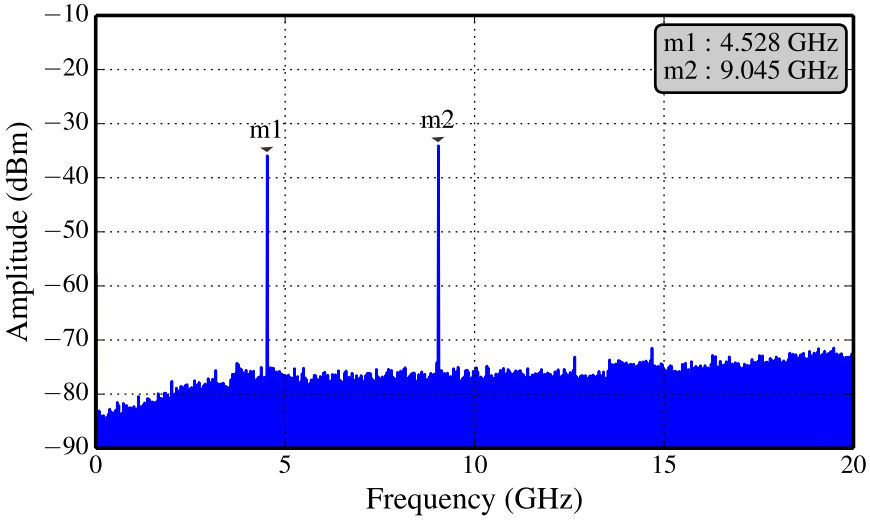


Figure 5.18: Measured power spectrum of the MMIC. The frequency of oscillation is at 4.528 GHz with a bias of V_{g1}=-3.25 V on the first stage and V_{g2}=-3.6 V on the second stage. The vertical amplitude scale is relative because of the use of a coupler at the output of the PA.

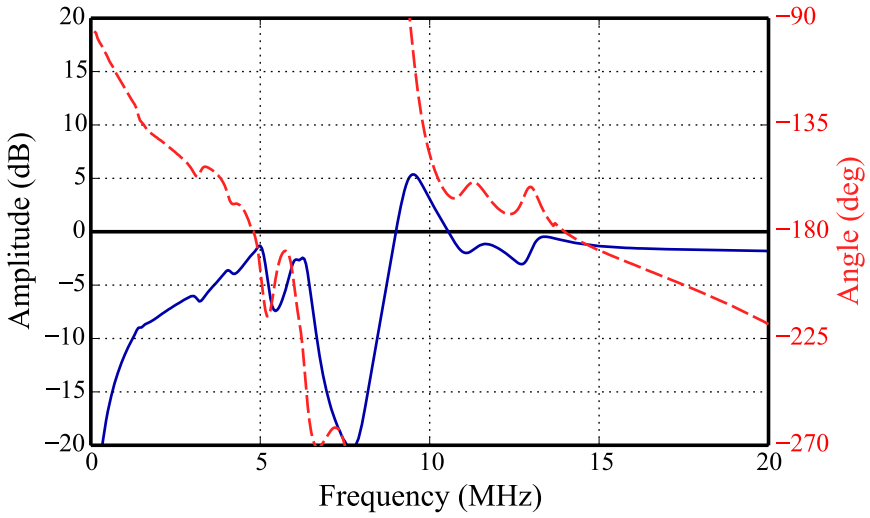


Figure 5.19: Simulated two-stage X-band GaN MMIC PA loop gain; magnitude (solid line) and phase (dotted line).

The simulated loop gain is plotted in Fig. 5.19 and shows there are two 180° phase crossings both

having amplitudes close to 0 dB. It is important to restate that the designer's discretion must be used here. The magnitude of the loop gain does not meet or exceed 0 dB yet it is close enough to suspect potential instabilities. Using such discretion, it is evident that the simulation predicted the 4.9 GHz oscillation 8.1% from the measured 4.5 GHz oscillation. The 9 GHz tone is a harmonic of the 4.5 GHz oscillation. Of note, there is no measured tone at 14 GHz which is more likely to oscillate (it is closer to encircling the $1\angle 180^\circ$ point). However, the 14 GHz oscillation may be an odd-mode oscillation: the common port (RF output) is a short for that mode and as such will not pass RF power. In addition, the even-mode loss through the output network at 14 GHz is 20 dB larger than the loss at 9 GHz. Both of these effects can add to give a much smaller tone power than the noise floor measured in Fig. 5.18.

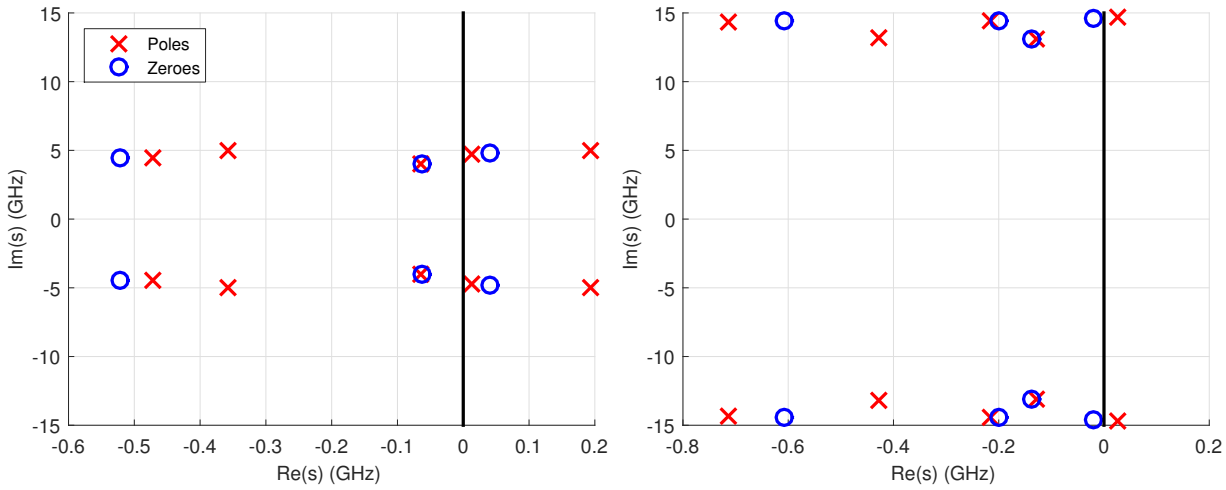


Figure 5.20: Pole-zero plots of the transfer functions of the X-band GaN MMIC PA plotted from (a) 1-6 GHz with 0 dBm input power and (b) 6 - 15 GHz with 8 dBm input power. Predicted instabilities at 4.69, 4.99 GHz in (a) and 14.67 GHz in (b) are close to measured results and verified by the dual-injection technique.

As in the S-band amplifier example, the commercially available stability analysis tool, STAN, that uses single current-source injection was used to validate the technique. The pole-zero plots

of the transfer function of the X-band amplifier are shown in Fig. 5.20a and 5.20b and predict instabilities at 4.69, 4.99 and 14.67 GHz. The RHP poles at 4.69 and 4.99 GHz are close in frequency to the predicted instability from the dual-injection technique and agree closely with the measured results. The predicted oscillation from the RHP pole at 14.67 GHz agrees closely with the dual-injection analysis.

5.4 Discussion and Conclusion

The technique of dual-injection is detailed and implemented in a HB circuit simulator and applied to circuits in linear and nonlinear operating regimes. A simple two-source injection element gives results that compare well to traditional single current injection stability analyses. The results of the analysis are conveyed in a manner that most circuit designers are familiar with (Nyquist criterion) for a single stage PA and a multistage X-Band PA. In both cases, measured instabilities are predicted by simulated instabilities following Nyquist criterion.

It is interesting to note that the loop gain functions can be generated even for the passive parts of the circuit, with the active device replaced by the dual injection network. Although this obviously results in a different loop gain, it still contains information about the behavior of the passive network, such as a resonance which could cause an instability. Therefore, the method can be used for analysis of harmonically-terminated classes of PA operation such as Class-F, since the loop gain magnitude and phase are relevant at the harmonic frequencies.

5.5 Contributions from This Chapter

The specific contributions to the field from this chapter are as follows:

- Application of dual-injection loop gain analysis to determine the stability of microwave PAs operating in linear and nonlinear modes. Validated analysis technique with measurements in single and multistage microwave PAs in a HB-based simulator.

- Validated new dual-injection technique with existing commercial stability analysis software.

Chapter 6

Millimeter-wave Component Integration Methods

Contents

6.1 Introduction

This chapter covers several important topics in millimeter-wave metallic rectangular waveguide assembly integration with active devices, such as passive waveguide assembly manufacturing, active device thermal modeling, and module thermal management. First, to reduce the cost and lead time of passive millimeter-wave waveguide assemblies, additive manufacturing (AM) is used for

fabrication of W-band waveguide structures. Next, the thermal problems that arise in millimeter-wave GaN MMICs are summarized, followed by a proof-of-concept thermal solution involving AM heat pipes.

6.2 AM for Millimeter-wave Components

This section presents several millimeter-wave dominant mode metallic rectangular waveguide components for W-band (75 - 110 GHz) fabricated using both direct metal laser sintering (DMLS) and stereolithography (SLA), in aluminum, nickel and copper alloys and metal-coated plastic (MCP). The RF performance and surface roughness are measured, and the loss due to surface roughness quantified. The measured loss at 95 GHz ranges from 0.055 dB/cm for the copper-plated plastic waveguides to 0.37 dB/cm for the nickel alloy. It is useful to think about the loss in terms of wavelengths as well. The guided wavelength of the TE_{10} mode in rectangular waveguide is given by:

$$\lambda_g = \frac{\lambda_0}{\sqrt{1 - (\frac{f_0}{f_c})^2}} \tag{6.1}$$

where λ_0 is the free-space wavelength, f_0 is the frequency of operation and f_c is the lower cutoff of the TE_{10} mode, given by $f_c = \frac{c}{2a}$ where c is the speed of light and a is the length of the broad wall of the rectangular waveguide. The guided wavelength at 95 GHz is ≈ 4 mm, and the measured loss per λ_g is 0.022 to 0.148 dB.

The motivation to study AM for microwave and millimeter-wave components is the potential for reduced cost and weight, shorter fabrication times and the ability to fabricate assembly geometries not possible with traditional split-block machining techniques [109]. AM is especially attractive for higher frequency waveguide components where product lead times are very long. There are a limited number of technologies that can provide conductor printing, most of them with roughness that is considered to be too high for low loss at frequencies above V-band. Published results include low-loss antennas and arrays in the 10-30 GHz range [110, 111], and millimeter-wave components such as W-band filters [112, 113] using a non-commercial tool with post-processing for improved

surface finish. Post processing is useful for finishing exterior surfaces but can become expensive. The focus of the work presented here is to evaluate various AM fabrication techniques for W-band WR-10 components, especially in terms of loss due to surface roughness. Results are compared for two simple components, a 10 cm straight waveguide section and a 20 dB directional coupler, using direct metal laser sintering and stereolithography with a variety of materials. Measured S-parameters are used to study the loss due to material conductivity, aperture dimension variation mismatch and surface roughness. The roughness is measured and quantified using focus-variation microscopy (FVM).

The 10 cm straight and 20 dB coupler waveguide components, shown in Figs. 6.1, 6.2, are designed in Ansoft HFSS and use standard UG-387 (MIL-DTL-3922/67E) flanges. Anti-cocking flanges were used in later designs to reduce mismatch loss at the test-DUT interface. The DMLS and SLA processes use 3D CAD models to fabricate the parts and a simplified mechanical drawing is created to specify alignment pin and hole sizes. The fabricated components are shown in Figs. 6.3, 6.4 in a variety of metals.

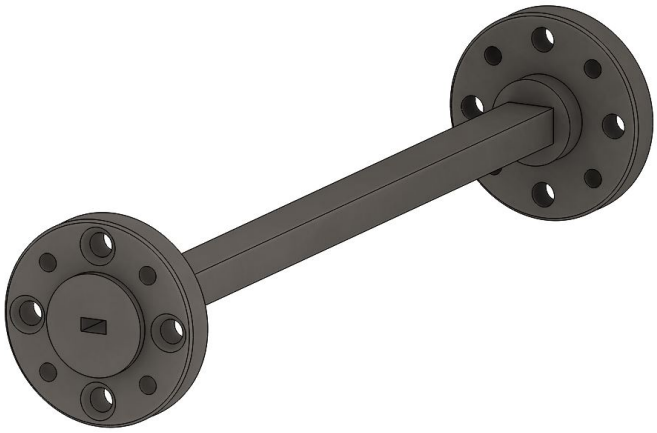


Figure 6.1: Straight 10 cm WR-10 waveguide model used for AM fabrication.

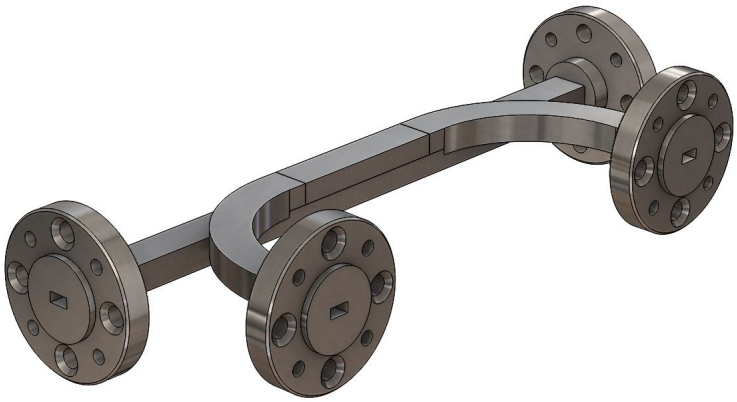


Figure 6.2: WR-10 20 dB directional coupler model used for AM fabrication.

Figure 6.3: Straight 10 cm WR-10 waveguides implemented in a variety of materials. From left to right: metal (Cu) coated plastic (MCP), GRCop-84 (Cu), Inconel 625 (Ni), and 3 AlSi10Mg with different laser settings.

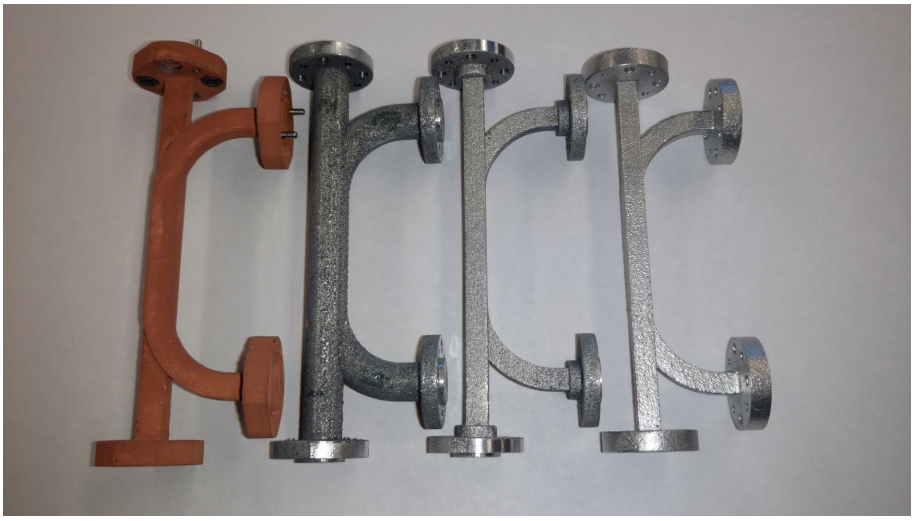
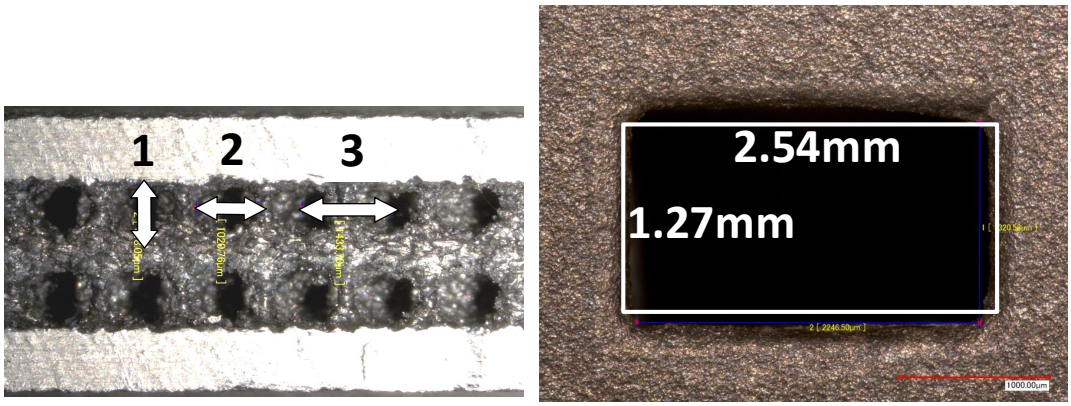


Figure 6.4: From left to right: WR-10 20 dB directional couplers in metal (Cu) coated plastic (MCP) and AlSi10Mg with different laser settings.

The DMLS process uses 20-40 μm metal particles that are sintered together with a 400 W Yb laser with a focused finite spot diameter of 200 μm that varies in both size and intensity with output power. Since waveguide features at millimeter-wave frequencies are smaller than 200 μm, different laser scanning strategies are employed. Typically, laser output power, spot speed and distance between multiple sintered lines, called hatches, are varied. In this work, two different laser scanning strategies were employed with AlSi10Mg, one with standard settings referred to as A1 and A2 (standard settings from different manufacturers) and one with higher energy density in the perimeter scan, referred to as A3. The trade-off in using higher energy density is reduced feature resolution.

As shown in Fig. 6.5a, the 20 dB coupler design uses 12 identical round coupling holes in a periodic array. The resolution of the DMLS process allows for a minimum wall thickness of 0.3 mm and a minimum feature size of 120 μm.



(a) (b)

Figure 6.5: a) Microphotograph of the interior of the 20 dB directional coupler after destructive testing. White arrows show fabricated dimensions: 1) 1020 μm hole diameter 2) a 818 μm hole diameter and 3) a 1433 μm hole-to-hole spacing. b) Aperture dimension deviation for the Cu waveguide. Inset is the correct WR-10 dimensions, as fabricated: 2.25 mm x 1.39 mm.

The DMLS fabricated 20 dB coupler design has a 0.508 mm hole diameter and a center-to-center hole spacing of 1.375 mm. Because of the SLA process limitations, a second coupler was designed with a larger hole spacing at the expense of bandwidth. All SLA results are reported for metal coated plastic with the metal being a proprietary Cu alloy.

6.2.1 Measured Performance

RF performance and surface roughness characterization are shown in this section for the waveguide components shown in Figs. 6.3, 6.4, fabricated in six different materials.

The RF performance was measured with an HP8510C and W85104A W-band frequency extenders. The S-parameters of the straight 10 cm WR-10 waveguide sections, in DMLS and SLA and with different materials, are shown in Fig. 6.6. While $|S_{11}| <$ -10 dB for nearly all components, $|S_{21}|$ varies for each material and the best performance is observed with MCP.

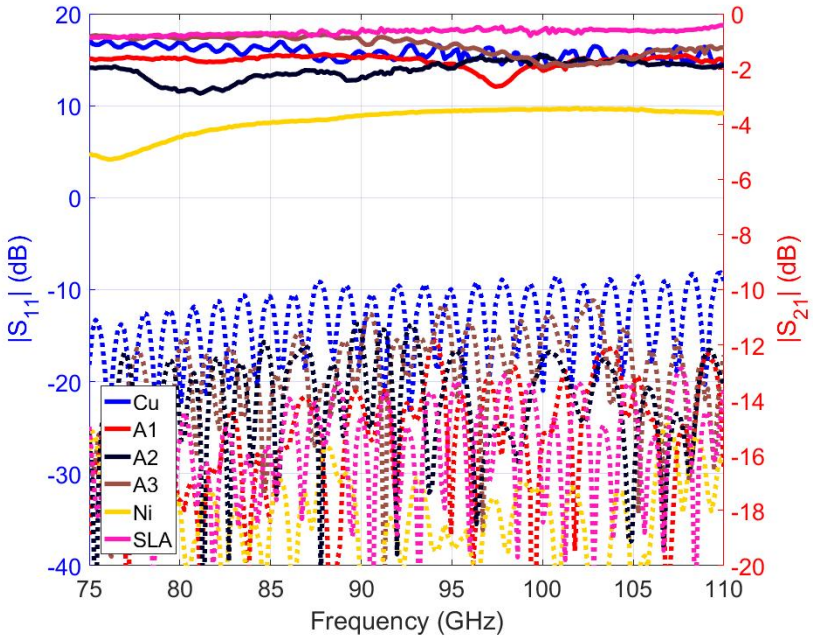


Figure 6.6: S-parameter results for the various fabricated WR-10 10 cm waveguide sections. The calibration $|S_{11}|$ was $<$ -20 dB and it is assumed the standing wave pattern is due to aperture dimension deviation and/or imperfect flange mating.

A summary of $|S_{21}|$ at the center frequency is given below for the 10 cm straight waveguide sections in various DMLS metals and the SLA metal coated plastic:

	A1	A2	A3	Cu	MCP
$\|S_{21}\|$ (dB)	-1.61	-2.27	-1.02	-1.41	-0.55

The S-parameters of the various WR-10 20 dB couplers in Figs. 6.7, 6.8 show that the best performance is again achieved with MCP. The DMLS AlSi10Mg couplers achieve close to 20 dB coupling ($|S_{31}|$ in Fig. 6.8) but insertion loss is high ($|S_{21}|$ in Fig. 6.7.) The A3 AlSi10Mg sample had no through transmission ($|S_{21}| \ll 0$ dB) and was excluded from Figs. 6.7, 6.8.

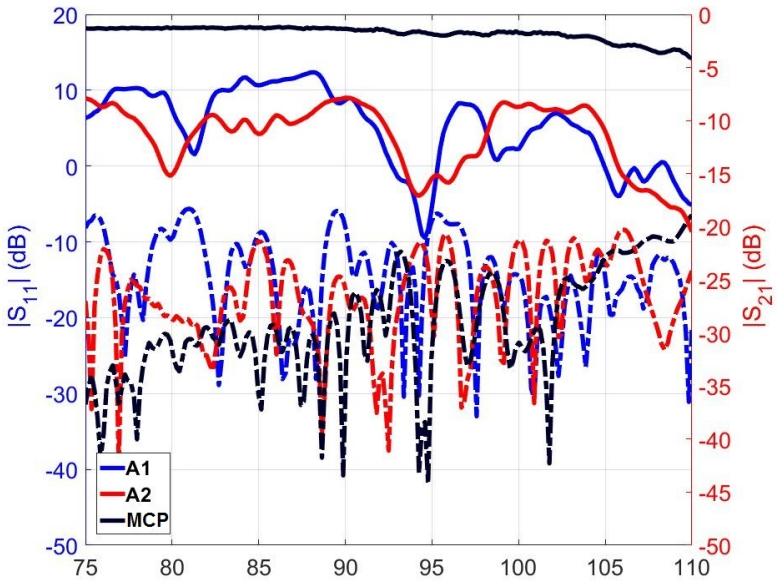


Figure 6.7: Measured $|S_{11}|$ and $|S_{21}|$ for the various fabricated WR-10 20 dB directional couplers. $|S_{11}|$ is shown in dashed lines.

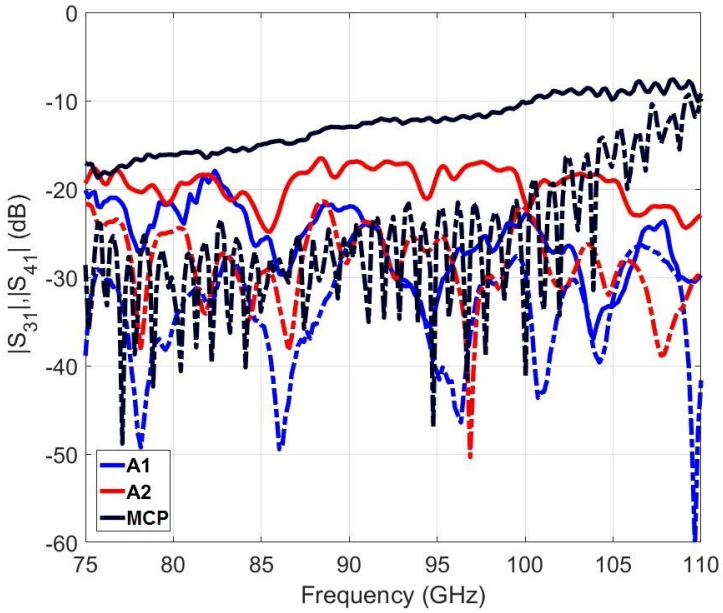
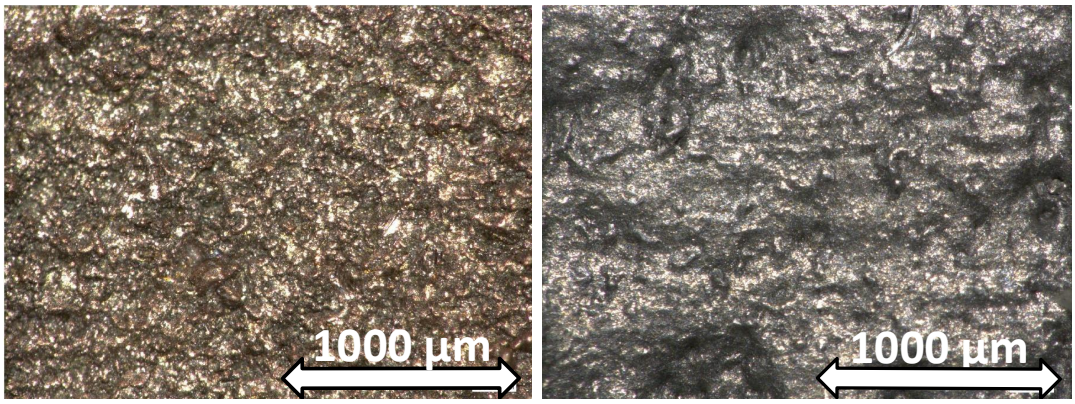


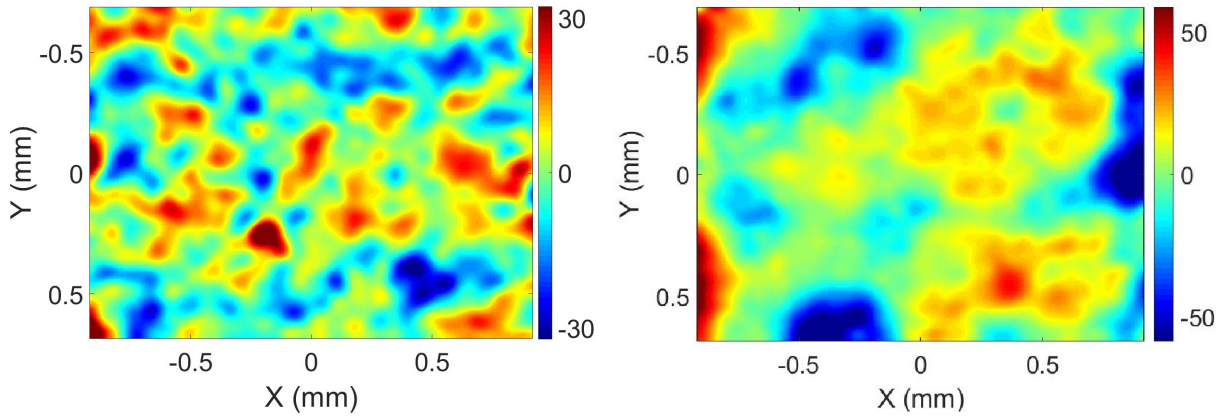
Figure 6.8: Measured coupling, $|S_{31}|$, and isolation, $|S_{41}|$, for the various fabricated WR-10 20 dB directional couplers. The isolation, $|S_{41}|$, is shown in dashed lines.

Surface roughness and realizable feature resolution are the primary limitations in AM millimeter-wave waveguide assemblies [114]. Because minimum feature resolution is often known more accurately than resulting surface roughness, this work focuses on surface roughness characterization. In [115], the spatial bandwidth limitations of FVM, an optical surface finish measurement technique, are analyzed and a measurement protocol is introduced to greatly reduce errors in the technique. The technique described in [115] is used in this work to characterize the surface finish of the AM waveguide components. Shown in Figs. 6.9a, 6.9b are the microphotographs of the waveguide interior surfaces taken during an FVM measurement. Shown in Figs. 6.10a and 6.10b is measured deviation in height of the interior of the Cu (GRCop-84) and A3 AlSi10Mg waveguides. The RMS surface roughness σ (often called R_q, R_{RMS} or S_q) and autocorrelation length L_q (often called Sal) are typically used to characterize the roughness of machined surfaces. The σ value is a measure of the mean deviation of the height and the L_q value is a measure of how the deviation is distributed laterally.



(a) (b)

Figure 6.9: a) WR-10 GRCop-84 and b) AlSi10Mg A3 10 cm waveguide section interior surface at 200x zoom.



(a) (b)

Figure 6.10: a) Measured WR-10 GRCop-84 10 cm waveguide topographical color map showing ± 30 μm height deviation. b) Measured WR-10 AlSi10Mg A3 10 cm waveguide topographical color map showing ± 50 μm height deviation.

In this work, common surface roughness measurement assumptions are made. The surface's autocovariance function (ACV) is isotropic and exponential and is modeled as:

$$ACV(\tau_x, \tau_y) = \sigma^2 e^{-\tau/L_q} \tag{6.2}$$

where σ is the RMS height variation and τ is the lag or displacement and is defined as $\tau = \sqrt{\tau_x^2 + \tau_y^2}$. Second, all height variations, σ, are assumed to follow a Gaussian distribution. Because the protocol used in the FVM measurements depends on these assumptions to produce accurate results, it is useful to plot the normalized autocorrelation of the measured surface roughness profile, as in Fig. 6.11. With the isotropic and exponential behavior of the surface roughness of the fabricated waveguide confirmed, the autocorrelation or autocovariance and RMS surface roughness can accurately be measured.

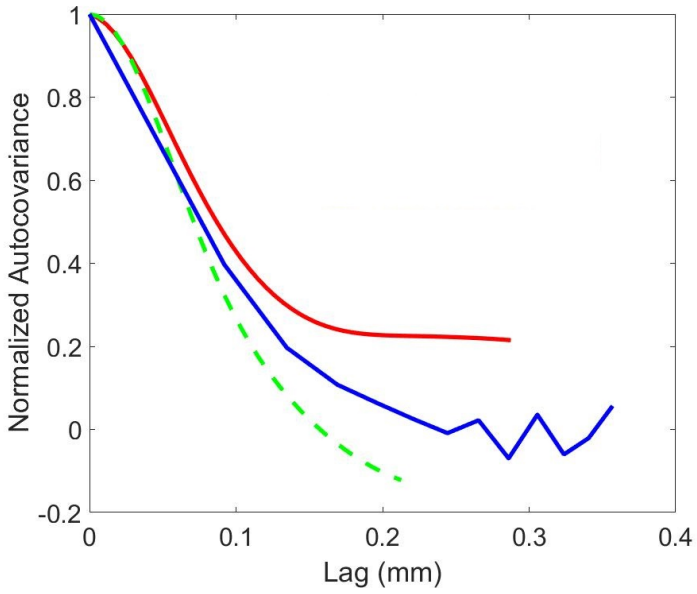


Figure 6.11: Normalized autocorrelation L_q, for GRCop-84. Autocorrelation lengths L_h, horizontal, and L_v, vertical show the computed L_q is a good fit to the ACV model before edge effects in the FOV limit affect accuracy.

Table 6.1 shows the σ and autocorrelation length, L_q for the various components. Surface roughness testing for the Ni alloy, Inconel 625, was not performed because the material is an extremely durable superalloy and successful destructive testing was not possible.

Table 6.1: Summary of AM Waveguide Surface Finish Characteristics at 95 GHz

Material	σ (μm)	L_q (μm)	α_{meas} (dB/cm)
AlSi10Mg A1	31.70	32.19	0.162
AlSi10Mg A2	12.90	N/A	0.227
AlSi10Mg A3	14.06	144.26	0.103
GRCop-84	12.50	60.85	0.141
Inconel 625	N/A	N/A	0.369
Cu MCP	9.46	199.89	0.055

6.2.2 Analysis and Conclusion

The study and modeling of energy loss at high frequencies due to rough surfaces has been a topic of research interest for more than 100 years [116]. Several models have been proposed to predict the loss due to the surface roughness of materials used in creating transmission lines, waveguiding structures, and cavity resonators. A good summary of the commonly used models is given in [34], some of which are listed below:

A commonly used approximation for determining loss due to surface roughness, named after Hammerstad and Jensen, [117], was designed to fit measured data from loss on microstrip lines and takes the form:

$$C_{SR} = 1 + \frac{2}{\pi} \arctan\left(1.4\left(\frac{\sigma}{\delta}\right)^2\right) \tag{6.3}$$

where δ is the skin depth and C_{SR} is a correction factor applied to the attenuation constant as: $\alpha_{rough} = \alpha_{smooth} C_{SR}$. A model by Filipović and Lukić in [116] is used for predicting loss in μ-coaxial lines and is an extension of the Hammerstad model:

$$C_{SR} = 1 + \frac{2}{\pi} \arctan\left(\left(\frac{\sigma}{\delta}\right)^2 \left(0.094\left(\frac{\sigma}{\delta}\right)^2 - 0.74\left(\frac{\sigma}{\delta}\right) + 1.87\right)\right) \tag{6.4}$$

A similar approximation to Eqn. (6.3), given by Groiss, Bardi, Biro, Preis, and Richter in [118] is used to calculate the loss in cavity resonators and takes the form:

$$C_{SR} = 1 + \exp\left(-\left(\frac{\delta}{2\sigma}\right)^{1.6}\right) \tag{6.5}$$

Eqns. (6.3), (6.4), and (6.5) predict loss due to surface roughness to saturate at $2\alpha_{smooth}$. A third model by Huray et al. uses the number of nodules, modeling the surface roughness as small snowballs, to approximate the surface roughness and resulting loss. That model takes the form of:

$$C_{SR} = 1 + SR\left(1 + \frac{\delta}{a} + \frac{\delta^2}{2a^2}\right)^{-1} \tag{6.6}$$

where SR is the Hall-Huray surface ratio and is given by:

$$SR = \sum_{i=0}^{j} \frac{N_i 6\pi a_i^2}{A_{smooth}} \tag{6.7}$$

where N_i is the number of snowballs of radius a_i within a certain area A_{smooth}. The ratios for all the snowballs, N, are summed up for the different radii, a_0 to a_j [34].

The approximations in Eqns. (6.5),(6.6) are used in popular EM structure simulation software, such as HFSS. From the measured surface roughness values in Table 6.1, it is seen that the predicted loss saturates at $2\alpha_{smooth}$ ($\delta_{Cu} = 0.22\,\mu$m at 95 GHz, $\sigma_{Cu} = 58\text{x}10^6$ S/m) for the Hammerstad, Groiss, and Filipović model. The measured data from the AM waveguide components shows the loss, shown in Table 6.1 as α_{meas}, near $4\alpha_{smooth}$, much higher than the predicted $2\alpha_{smooth}$. Because of the widespread use of Eqn. 6.3 in commercial EM simulators, simulated surface roughness loss is not accurate (predicted losses are too small) for very rough surfaces ($\sigma \gg \delta$).

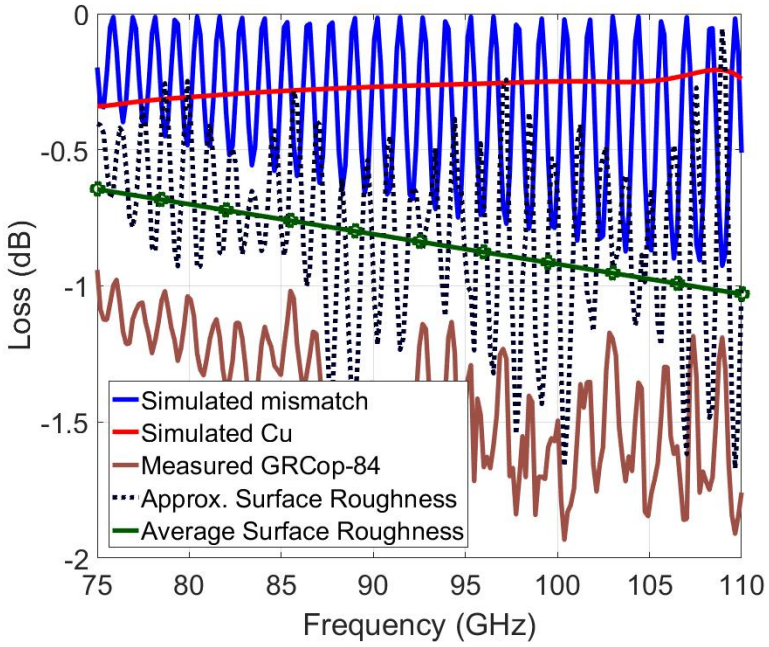


Figure 6.12: Different loss mechanisms for GRCop-84 AM waveguide. The surface roughness loss is approximated by subtracting simulated losses (mismatch from aperture dimension deviations and idealized Cu loss) from the measured S-parameter data. Average surface roughness loss (green) is the moving average of the calculated approximate surface roughness loss.

As fabricated, the GRCop-84 waveguide aperture, shown in Fig. 6.5b, did not meet the specified

dimensions of WR-10. The dimension deviation is a source of mismatch loss when connected to the W85104A test set. In Fig. 6.12, the approximate surface roughness loss for GRCop-84 waveguide is shown. This loss is calculated by subtracting the sum of simulated mismatch loss and simulated loss from the conductivity of copper from the measured $|S_{21}|$. A potential source of error in this loss calculation is the difference between the conductivity of the bulk material and the DMLS structure.

In conclusion, this section summarizes the performance of a several AM W-band waveguide components using common commercially available technologies. The measured loss of the fabricated components at 95 GHz ranged from 0.055 dB/cm for the MCP waveguides to 0.1 dB/cm for a common AM Al alloy with improved surface finish. The loss mechanisms introduced by the AM process are characterized and it is shown that widely used models for surface roughness loss prediction are not adequate for typical AM materials. Further work is also needed to investigate the effects of differences in conductivity for bulk and DMLS AM materials. The use of V- and U-band AM waveguides, as demonstrated in chapter 3, is the suggested frequency limit for useful, low-loss operation.

6.3 Thermal Challenges in Millimeter-wave Component Design and Additive Manufactured Heat Pipes

This section describes the thermal challenges encountered in the integration of millimeter-wave MMIC components. A widely used dual electrical-thermal equivalent circuit model for determining the thermal operating point of transistor amplifiers is presented as an introduction. A thermal analysis is then performed in a finite-element method thermal solver for some of the MMIC designs in this work, followed by a proof-of-concept solution to thermal management that incorporates AM heat pipes.

6.3.1 Thermal Analysis for MMIC Design

The thermal management of MMIC PAs is a common ground between the MMIC designer and the module integrator. The MMIC designer tries to maximize power per mm^2 and GaN has

been a major breakthrough in this respect. The goal is to then integrate MMICs on a PCB, as a hybrid circuit, or with chip and wire techniques. The challenge for the module integrator is to not only fixture the MMICs and ensure RF performance of the integrated assembly, but also to meet certain environmental test requirements. In the commercial realm, ambient operating temperatures can be between 0 and 85 °C. In military applications, the temperature range can be from -55 to +125 °C [119], [120]. As shown in Fig. 6.13, higher transistor junction temperatures result in higher failure rates. The question is how to calculate the junction temperature, T_J, from the ambient or base plate temperature.

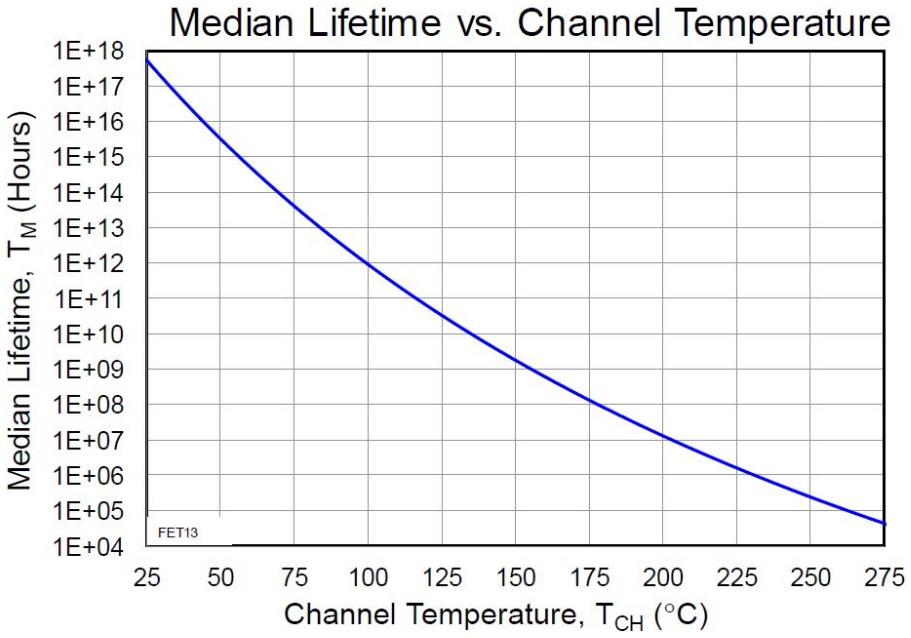


Figure 6.13: Mean time to device failure based on junction temperature for an X-band, 60-W GaN PA. MTTF > one million hours is a commonly specified standard in military and SATCOM applications. Source: [10].

The relationship between ambient temperature and device junction temperature can be better understood by use of an electrical analogy that relates dissipated power to temperature rise. This is commonly done to allow circuit designers to solve for junction temperatures without thermal modeling [121]. For both packaged devices and chip and wire solutions, the MMIC designer or

foundry will provide a thermal junction resistance that is defined as:

$$\Theta_{JA} = \frac{T_J - T_A}{P_D} \tag{6.8}$$

where T_J is the junction temperature, T_A is the ambient temperature, and P_d is the dissipated power. Instead of ohms, the thermal junction resistance has units of °C/W. The relationship is used in a equivalent circuit model as shown in Fig. 6.14.

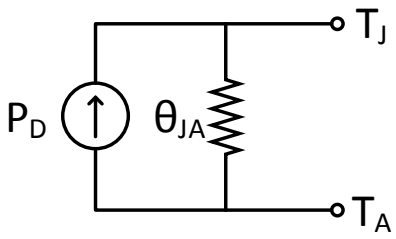


Figure 6.14: The equivalent electrical circuit model for thermal operation of a transistor amplifier. Current, resistance and voltage are analogous to dissipated power, thermal resistance, and temperature.

Where P_D is the dissipated power, Θ_{JA} is the thermal resistance from ambient to transistor junction, and T_J and T_A are the ambient and transistor junction temperatures, represented by voltages. The model is usually not that simple however and needs to account for thermal energy stored in materials as they heat up. Since temperature rise is proportional to stored energy, and stored energy is equal to the integral of the power dissipated, the ratio of heat energy to temperature rise is represented as a capacitance. The units of thermal capacitance are J/°C. A typical circuit model for a transistor amplifier thermal solution is shown in Fig. 6.15, where C_J is the junction thermal inertia, Θ_{JSo} is the thermal resistance between the transistor junction and the solder connection or epoxy, Θ_{SoC} is the thermal resistance between the solder and the case, usually very small, C_{Case} is the thermal inertia of the transistor case or packaging, Θ_{CHs} is the thermal resistance between the case and the heat sink and last the thermal resistance to ambient and inertia of the heat sink are modeled as C_{HS} and Θ_{HA}.

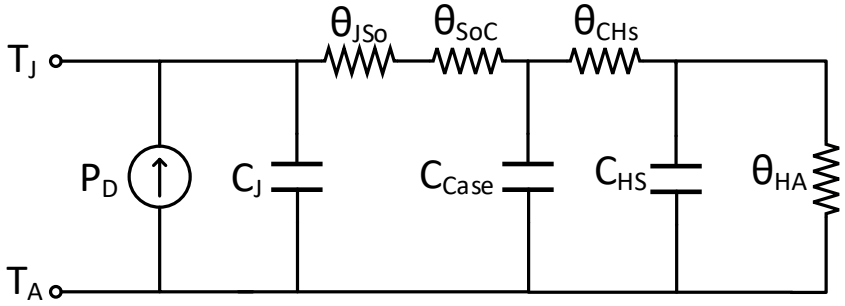


Figure 6.15: A more complex equivalent circuit model for thermal operation. The thermal resistances represent interfaces in the physical layout of the transistor amplifier. The capacitors represent thermal inertia of the layers between the interfaces.

By providing the various thermal resistances internal to the MMIC and maximum safe junction temperatures for long device operation, a MMIC designer or foundry helps the module integrator begin their thermal design. The module integrator then will have to decide on a passive or active solution for heatsinking that has adequate thermal transit to the ambient environment. This usually takes the form of a heat sink and DC powered fan. The details of the thermal design from MMIC package to ambient is outside of the scope of this work.

The cooperative process described above does not explain how the thermal resistances internal to the MMIC and the packaging or assembly are determined by the designer or foundry. To determine the internal thermal resistances, a simulation of the MMIC devices and layout is needed.

6.3.2 FEM Thermal Analysis

A finite element method (FEM) analysis to determine the thermal operating point of a MMIC amplifier is performed for accurate modeling. The method used in this work generates an equivalent RC network similar to the simple model described above. To perform a thermal analysis, the first step is to generate an accurate model of the FET or active devices used in the design. This is the most important step because the active devices dissipate almost all of the heat in a MMIC when low-loss passives are available. Resistors that dissipate significant heat should also be modeled but this is not common in microwave and millimeter-wave designs. After the device model is created,

a MMIC is then modeled by arranging multiple device models in the same X-Y mapping as on the MMIC. Mapping several active devices in the thermal analysis allows for the total thermal effect of the devices to be simulated. The devices are arranged on the modeled substrate with a base plate temperature equal to the system ambient temperature. A thermal analysis program designed specifically for interface to MMIC design software, SYMMIC, was used to determine the total temperature rise from base plate to transistor junction in this work [122].

Shown in Fig. 6.16 is the single transistor thermal model for the HRL T4 4x20 μm device. The upper boundary condition is an airbox above the transistor. The lower boundary condition is the baseplate which has a very high thermal conductivity and acts as a perfect heat sink. Shown in Fig. 6.17 is the mesh for the FEM simulation. The base plate in the simulation is 300 K.

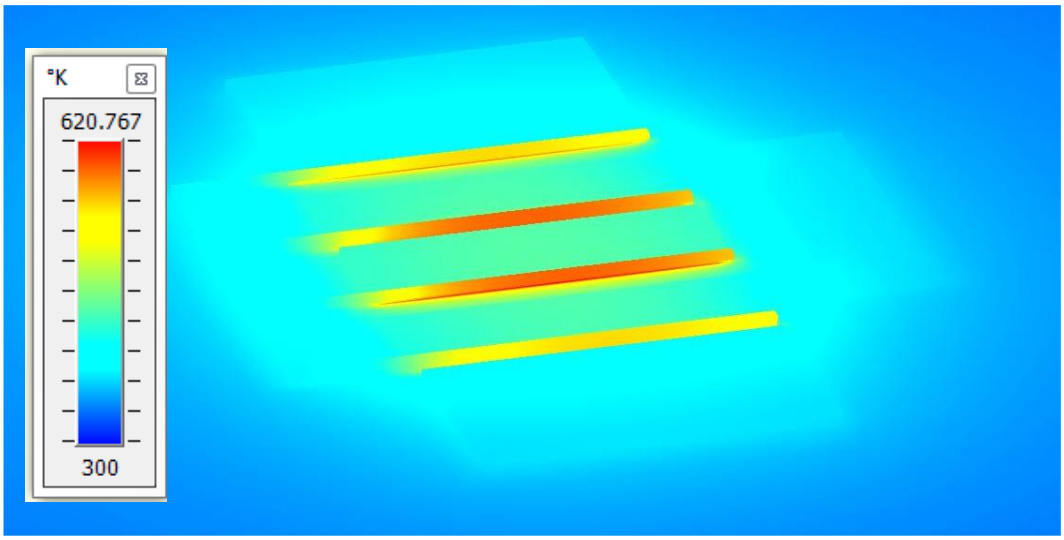


Figure 6.16: The HRL T4 4x20 μm device with 3.3 W dissipated power. The channel temperature is shown in the legend and peaks at 550 K.

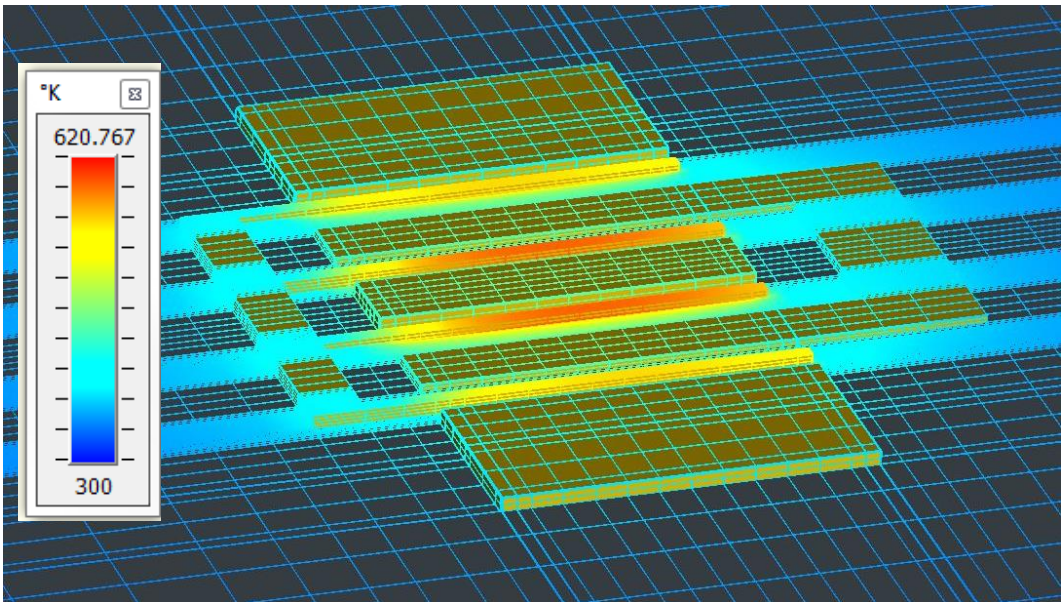


Figure 6.17: The mesh for the FEM thermal simulation of the HRL T4 4x20 μm device

Because the 235 GHz amplifiers from chapter 4 have 24 and 32 devices for the 3-stage and 4-stage amplifiers, the thermal analysis of those dice is critical. The thermal simulation setup of the 4-stage PA is shown in Fig 6.18 and the heat map of the solution is shown in Fig. 6.19.

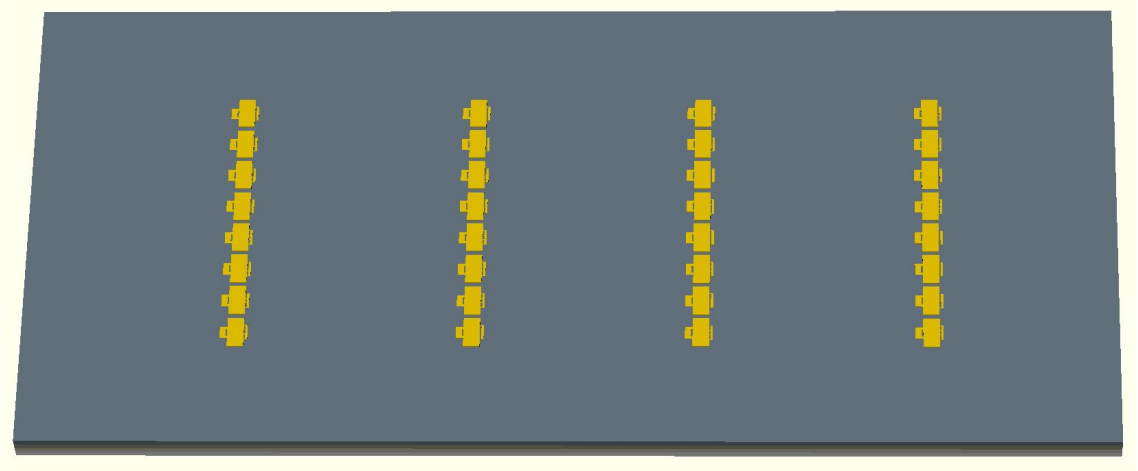


Figure 6.18: The thermal analysis simulation setup. The devices are those shown in Fig. 6.16 arranged in the same X-Y mapping as the full amplifier. The MMIC dimensions are 4.4 mm x 1.8 mm.

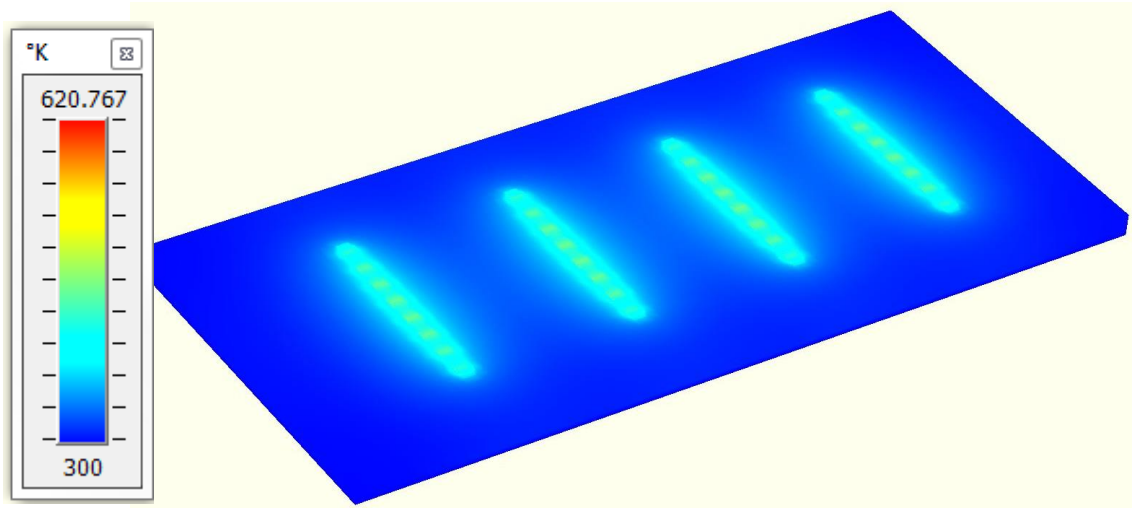
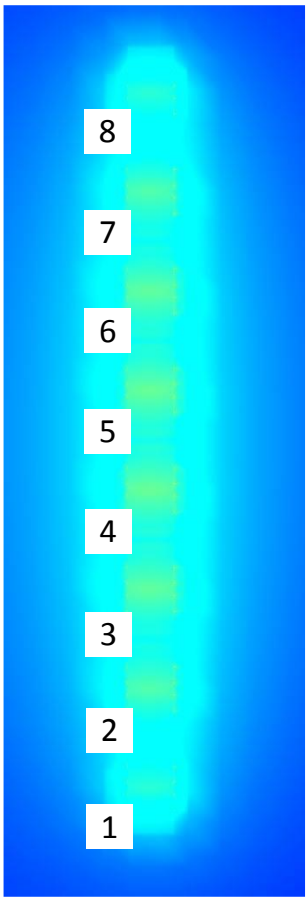


Figure 6.19: The 4-stage 8-way power combined MMIC PA thermal solution. The maximum temperature is 620 K, a 320 °C temperature rise. The MMIC dimensions are 4.4 mm x 1.8 mm.

The total temperature rise from the base plate to the junction is 320 °C. As to be expected, the middle devices exhibit the highest junction temperatures. The maximum temperature is also increased from the single device, 550 K, to 616 K due to multiple devices. A summary of the maximum device temperatures is given in Fig 6.20b.



(a)

Device #	$T_{max}\,(^{\circ}C)$
1	580.5
2	603.6
3	612.7
4	616.6
5	616.6
6	612.7
7	603.6
8	580.5

(b)

Figure 6.20: a) The device numbers for the 8-way combiner and b) the maximum device temperatures, T_{max}.

The assumption in the previous analysis is that the heat sink structure will have a large enough thermal inertia that its temperature is not affected by the mounted die and package. In the 8-way combined, 4-stage PA example, the total die area is $7.92\,\mathrm{mm}^2$. The total dissipated power is $1.3\,\mathrm{W/mm}^2$. To ensure that the heat can efficiently be transported to a larger heat sink, a method that uses the previously described AlSi10Mg DMLS AM process is investigated for integrated cooling with a heat pipe.

6.3.3 Additive Manufactured AlSi10Mg Heat Pipes

This section describes the operation of fixed-conduction heat pipes and demonstrates the performance of several proof-of-concept additively manufactured Al-alloy heat pipes.

Fixed-conduction heat pipes have four important components, an evaporation section, a condenser, the working fluid, and a sealed adiabatic section that allows the working fluid to transport heat between the evaporator and condenser. A simple representation of the main components is shown in Fig. 6.21.

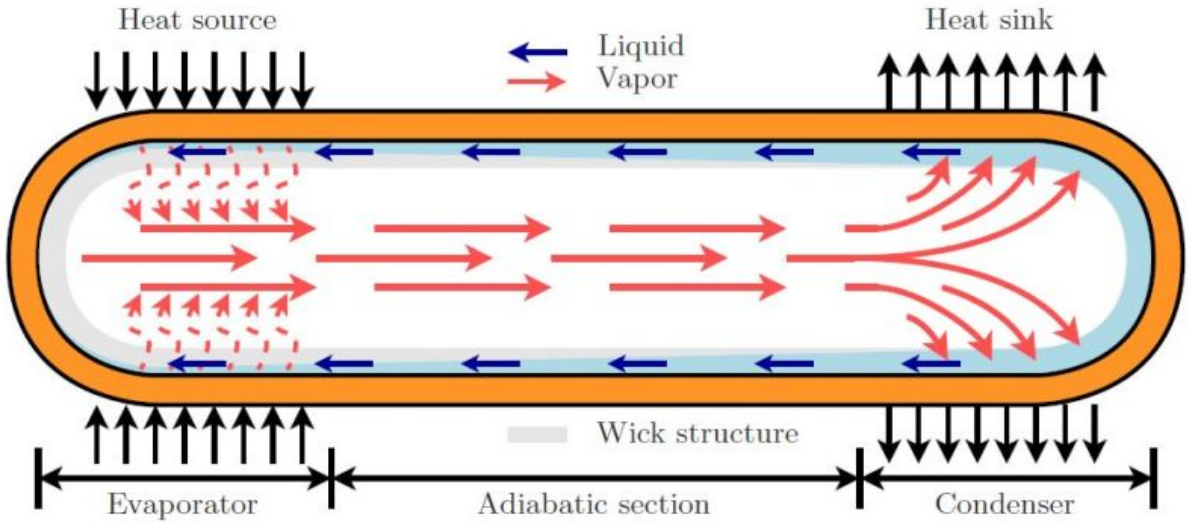


Figure 6.21: The operation of a fixed-conduction heat pipe. Source: [11].

The operation of the heat pipe is as follows. First, application of heat to the evaporator section causes some of the working fluid to evaporate and the saturation condition results in a difference in vapor pressure which causes vapor to flow to the condenser. The condenser is connected to a heat sink where the latent heat is released to the surrounding area. The heat removed through the heat sink causes the working fluid to condense back to a liquid state and gravity or a wicking structure that uses cohesion allows for the working liquid to return to the evaporator where the process begins again. There are no moving parts in a simple fixed-conduction heat pipe, the pumping action is provided by the removal of latent heat. The operation of the heat pipe can also be understood as

a closed system that utilizes a high thermal conductivity section (created by a working fluid) to transfer heat efficiently from a source to a sink.

In this application, the heat source is an IC that generates a high heat density and the sink is a larger area heat sink with either active or passive cooling. Water filled copper heat pipes are now in use in mass produced various consumer electronics such as cell phones, laptops, and desktop computers [123]. Aluminum and aluminum alloy heat pipes have been an area of research and development in the aerospace sector for several years and utilize a variety of working fluids excluding water. Because of the encouraging results in the AM waveguide section with Al-alloys, aluminum heat pipes are the focus of the work in this section.

Design of a heat pipe can range from a few simple steps to a complicated process depending on the power levels and mode of operation. For the simple proof-of-concept demonstrated here, the material, AlSi10Mg, was selected because of its widespread use in AM. This led to the first decision in the design process, which working fluid to use. The choice of which working fluid to use depends on the working pressure, fluid properties, capillary pumping limit and thermal conductivity required. The working fluid must also be compatible with the pipe material and not cause a chemical reaction that produces non-condensable gas as a byproduct, as this would eventually stop heat transport. A summary of the compatible working fluids is given in Table 6.2 from [124]. Ammonia has the best overall combination of thermophysical and derived properties for Al heat pipes [125]. Ammonia also has a high liquid transport factor, wicking height, thermal conductivity and low kinematic viscosity ratio [125].

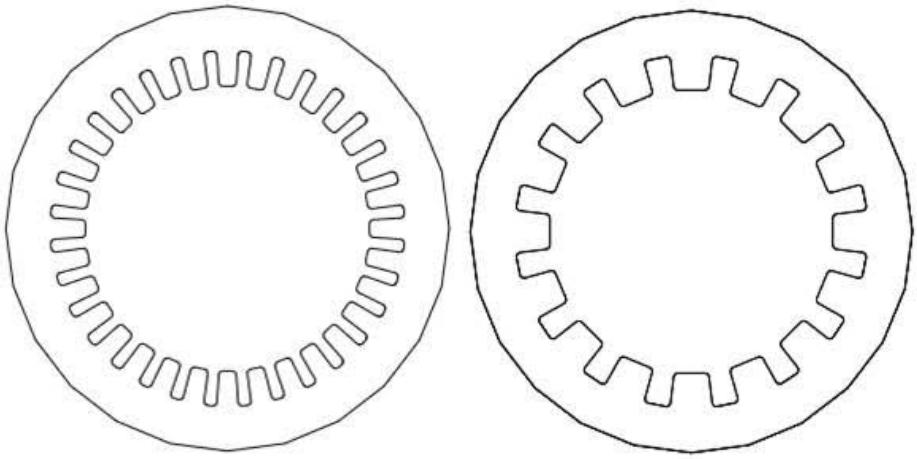
To test the proof-of-concept heat pipes with a similar fluid, acetone was used as it is easier to handle and not as caustic. The next step in the design is create a suitable wicking structure for the working fluid.

Shown in Figs. 6.22a, 6.22b are the profiles of the AlSi10Mg heat pipe wick structures. In Fig. 6.22a, referred to as Pipe 1, there are 32 teeth of width 0.8 mm. The number of teeth in Pipe 1 was the maximum allowed with the minimum feature size limit of the AM process. The idea behind maximizing the number of teeth was to maximize the surface area. Wicking structures

Table 6.2: Compatibility of Working Fluids and Heat Pipe Materials

Working Fluid	Useful Range(K)	Compatible Material	Incompatible Material
Water	303-550	SS, Cu, Silica, Ni, Ti	Al, Inconel
Ammonia	213-373	Al, SS, CRS, Fe, Ni	N/A
Methanol	283-403	SS, Fe, Cu, Brass, Silica, Ni	Al
Acetone	273-393	Al, SS, Cu, Brass, Silica	N/A
Sodium	873-1473	SS, Ni, Inconel, Nb	Ti
Mercury	523-923	SS	Mo, Ni, Ta, Inconel, Ti, Nb
Lead	1670-2200	W, Ta	SS, Ni, Inconel, Ti, Nb

with greater surface area can return more condensed working fluid to the evaporator faster. In Fig. 6.22b, referred to as Pipe 2, the number of teeth are reduced by half and the width is increased to 1.6 mm. A third design was created using the wick profile from Pipe 2 with an experimental porous surface to increase surface area and is referred to as Pipe 3.



(a) (b)

Figure 6.22: a) Heat Pipe 1 wick profile. The total outside diameter (OD) is 10 mm. (b) Heat Pipe 2 wick profile. The number of teeth is reduced and the spacing between doubled.

A summary of the important parameters of the heat pipes is given in Table 6.3.

To test the heat pipes, all three wick variations were filled 30% with acetone according to the total internal volume in Table 6.3. The pipes were heated on one side (the evaporator) with a

Table 6.3: Summary of Heat Pipe Parameters

Pipe	No. of Teeth	Internal Vol. (mL)	Working Fluid Vol. (mL)
1	16	10	3
2	32	9	3
3	32	8.4	2.5

20 W load from a power resistor and DC power supply. A picture of the heat pipe, power resistor and heat sink is shown in Fig. 6.23.

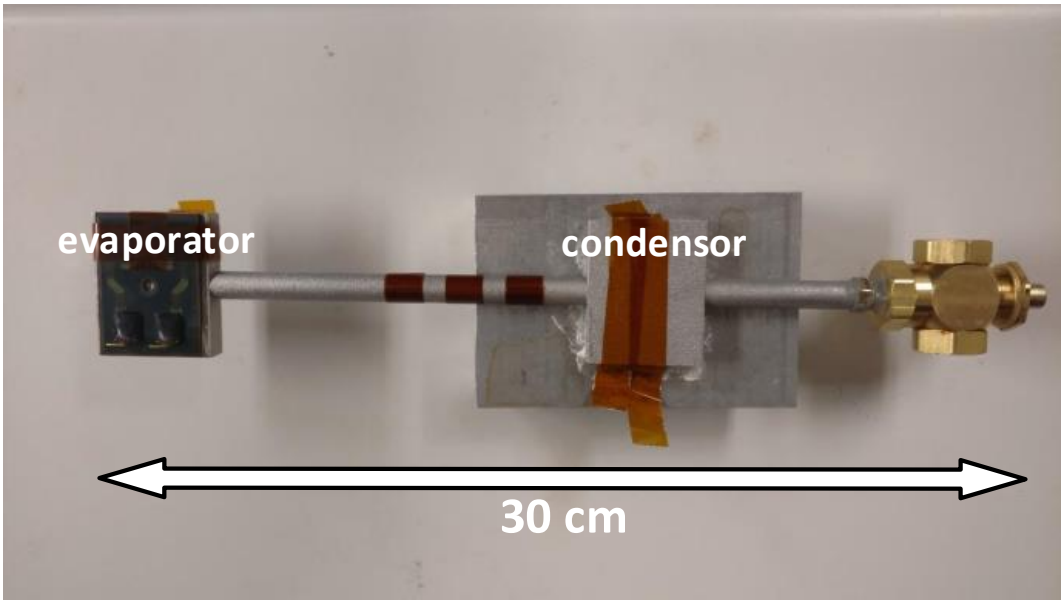


Figure 6.23: Setup for heat pipe testing. The thermocouples are attached to the outside of the condenser and evaporator. The temperature difference between the evaporator and condenser is ΔT. The total pipe length is 30 cm.

The temperature difference between the condenser and evaporator, ΔT, was measured over 1000 seconds. An ideal heat pipe would transfer the heat from evaporator to condenser without a temperature difference, $\Delta T = 0$. In Fig. 6.24, ΔT between the evaporator and the condenser sections is shown and a start up condition exists where the pipe does not conduct heat other than through metal conduction, which is very poor for a hollow metal pipe. The various wick structures

have different amounts of time before they start to conduct heat via the working fluid. Once the working fluid starts to evaporate and cycle in the heat pipe, ΔT is very small, less than 5 °C and often less than 2 °C. Running the test in reverse, starting with a high temperature and letting the heat pipe cool down, results in a very small ΔT until the system reaches room temperature. As shown in Fig. 6.24, Pipe 3 has the lowest maximum ΔT and was chosen for further testing.

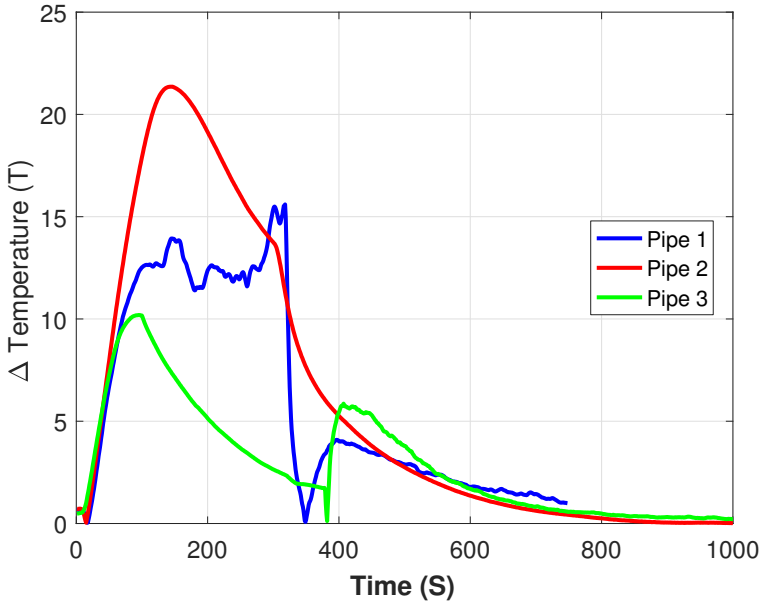


Figure 6.24: ΔT for different heat pipe wick structures over time with a 20 W thermal load.

In Fig. 6.25 Pipe 3 was tested with various dissipated powers. The heat pipe shows low ΔT from 10 to 40 W, and transfers heat from the evaporator to the condenser faster than the condenser can transfer it to the environment, resulting in a negative ΔT. Because the heat pipe is a two-phase heat transfer system the thermal conductivity, expressed in W/m-K, is not constant. The heat equation relates heat flux, thermal conductivity, and ΔT as:

$$q = -k\Delta T \tag{6.9}$$

where q is the the rate of flow of heat energy or heat flux, k is the thermal conductivity and ΔT is the temperature difference. For 40 W through an area of $5^2\pi = 78.54\,\text{mm}^2$, the measured heat flux is 509 $\frac{kW}{m^2}$. Referring to Fig. 6.25 for Pipe 3, ΔT ranges from 2 to 10°C. The resulting thermal

conductivity ranges from 51 kW/m-K to 254 kW/m-K. The thermal conductivity of a commercially available heat pipe ranges from 10 - 10,000 times the conductivity of a pure copper pipe, which is 400 W/m-K. The AM heat pipe results from this section are therefore close in performance to commercially available solutions.

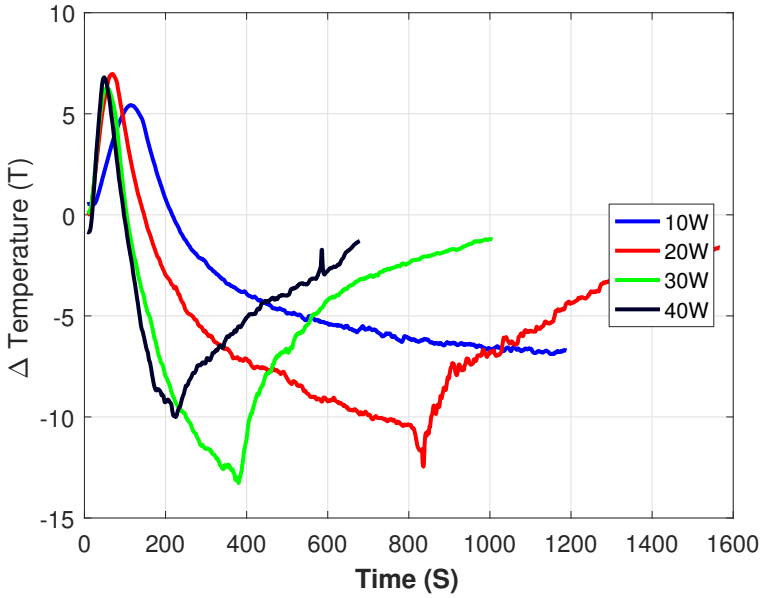


Figure 6.25: Pipe 3 ΔT for various thermal loads. The thermal conductivity is a function of dissipated power and varies over the power range.

6.4 Conclusion

In conclusion, this section has shown that heat pipes and millimeter-wave waveguides can be fabricated from the same commonly used material and processing techniques found in commercial DMLS AM. The increased power handling of GaN combined with the low-efficiency of miliimeter-wave active components requires new techniques for solid state power amplifier thermal management. There are multiple ways to include such heat pipes in a PA module design. The heat pipes demonstrated in this section have a 10 mm OD. Typical single MMIC PAs are on the order of 5 mm x 5 mm, meaning the heat pipes should be reduced in size by half to fit directly under individual MMICs. In that configuration, multiple heat pipes could be fabricated in one block of

AlSi10Mg and heat from different MMICs could be routed to different heat sinks. Hybrid or chip and wire combined MMIC PAs could benefit from a single heat pipe similar in diameter to the one demonstrated because as the MMICs are much smaller than the demonstrated heat pipe, the DC bias board, off-chip bypass capacitors, and off-chip combining structures greatly increase the total minimum size where heat needs to be removed.

6.5 Contributions from This Chapter

The specific contributions to the field from this chapter are as follows:

- Demonstrated several W-band AM waveguides using commercially available DMLS and SLA processes. Measurement of loss due to surface roughness in AM waveguides. Measurements of surface finish were made using FVM and it was shown that commonly used EM models do not predict loss due to surface roughness correctly.
- Demonstration of AM acetone-filled AlSi10Mg heat pipes in a shared process with proven millimeter-wave waveguide assemblies. The AM heat pipes demonstrated thermal conductivities of 51 to 254 kW/m-K, which matches the performance of commercially available heat pipes.

Chapter 7

Future Work, Summary and Contributions

Contents

This chapter briefly discusses some of the possible directions for future work that builds on the results of this thesis. The main focus for potential future work is in further development of millimeter-wave GaN MMIC design techniques and component integration using the benefits of AM where appropriate. A new application for the stability analysis detailed in Chapter 5 specifically for millimeter-wave amplifiers represents a potentially extensive area of research. As active circuits continue to operate at higher and higher frequencies, stability will become more of a problem. The problem is not the devices themselves but the massively increased bandwidth over which the millimeter-wave devices must be stabilized. This chapter concludes with a summary of the contributions that are made in the thesis, in order of their appearances in the proceeding chapters.

7.1 Future work in Millimeter-wave MMIC Design and Fabrication

Fabrication issues with the MMICs in Chapter 3 and 4 limited the reported results in this work. The most obvious direction for future work based on this thesis would be to test newly fabricated versions of the same circuits when the processes become more stable and mature. The

main problem in attempting research involving millimeter-wave MMICs is that the fabrication is very expensive and slow. This leads to fewer opportunities to refine designs during the duration of a typical PhD compared to work at X-band or low GHz. The experience of working closely with the foundries on in-development fabrication processes was valuable but had many inherent risks. The fabrication processes used in this work to explore the MMIC designs reported some of the best results in terms of f_T, output power, efficiency and gain currently available at millimeter-wave frequencies. However, the performance of the transistor devices is not yet routinely repeated. Future work in this area would be contingent on process stabilization and yield improvement.

From a design standpoint, a particularly important area of research in millimeter-wave GaN amplifier design is the stability of the circuits, as already stated. As the available gain and output power at millimeter-wave frequencies improves and f_t of the devices goes up, there is more risk for instabilities at frequenices below the operating frequency. Eliminating the risk of instabilities out of band is an iterative process that occurs when the in-band performance is already verified. Recently there has been work reported that focuses on the stability of single transistors at millimeter-wave frequencies. Because any transistor with more than two gate fingers is no longer symmetrical and small physical distances in substrates with $\epsilon_r = 10$ translate to significant electrical lengths, oscillations can occur in devices without any external feedback. The analysis of W-band LNAs with oscillations that occur inside the transistors for multi-finger HEMTs is discussed in [12]. The frequencies in [12] are not obscure, they are in fact in the middle of newly allocated spectrum in the 71-76 and 81-86 GHz range, making the results relevant to many future designers. The asymmetrical nature of multi-finger HEMTs is shown in Fig. 7.1 where the two-finger device is inherently symmetric yet larger devices are not due to air bridges between source fingers. The simulation technique is shown in Fig. 7.2. The reported stability analysis in Chapter 5 could be used to analyze multi-finger transistors as well, similar to the setup in Fig. 7.2.

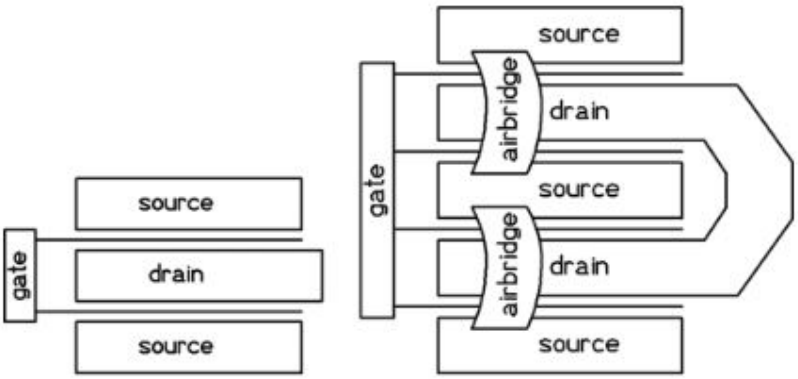


Figure 7.1: A symmetrical two finger HEMT shown on the left. Scaling the device for power handling or thermal management creates asymmetrical devices and can cause oscillations. Source: [12]

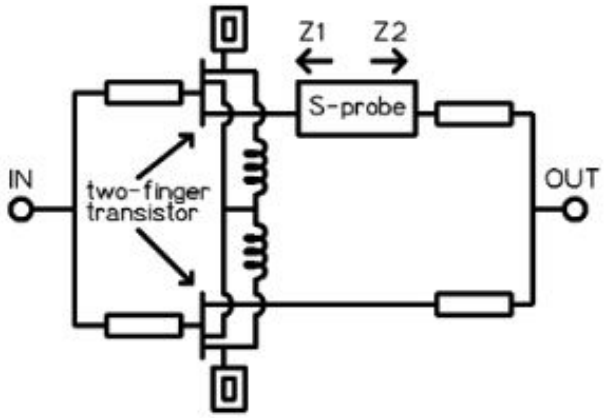


Figure 7.2: The simulation setup for determining the stability of asymmetric devices. Instead of a S-probe, the stability analysis in chapter 5 could be used to validate stability. Source: [12]

A similar analysis for multi-finger FETs is reported in [126]. The application in [126] is high power FETs with large gate-to-gate spacing (pitch) for thermal concerns.

7.2 Future work in AM Integration

The results in the AM integration chapter show what is currently possible with commercially available DMLS and SLA manufacturing processes for W-band components. Because of the trade-off between feature size and surface finish, W-band and higher frequency waveguide components, beyond straight waveguide and open structures such as parabolic or aperture-based antennas, are not yet practical. The limits of the AM processes are not as critical in the V-band (50-75 GHz) range and results of an 11 cm straight waveguide fabricated in maraging steel, shown in Fig. 7.3, are promising. As discussed in chapter 3, the potential new uses for V-band systems means that AM V-band waveguide components could become very widespread. In particular, if the commercial market for V-band satellite based internet service develops as predicted, large volumes of V-band AM waveguide assemblies would be needed. The current widespread use of heat pipes in satellite thermal management means that AM heat pipes represent a potential extensive research area.

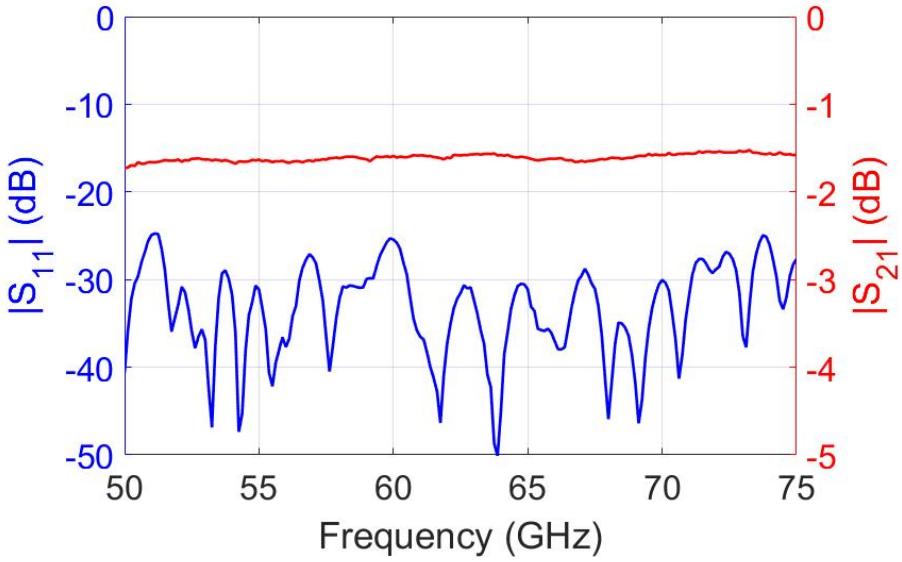


Figure 7.3: S-parameters for a 11 cm straight waveguide section fabricated in maraging steel.

7.3 Summary and Contributions

In summary, the work presented in this thesis addresses several important aspects in the analysis, design and fabrication of microwave and millimeter-wave GaN MMICs and components. Specific contributions from Chapters 2 - 6 are summarized below. Published results are summarized after each affiliated contribution.

- Chapter 2 - Efficiency-Enhancement Techniques for X-Band GaN MMIC PAs - contains three different demonstrated GaN MMIC amplifier designs that address efficiency enhancement:

  An X-band output harmonic injection amplifier with $P_{out} = 3.6\,\mathrm{W}$ and efficiency improved from 36 to 50% at 10.6 GHz and 48 to 70% at 10.6 GHz. The output harmonic injection $2f_0$ driver operates at 20 GHz and had 27 dBm of output power, 8 dB of gain and a PAE=59%. Results from this section of the chapter are reported in [127]. Previous results at 2.45 GHz showing an improvement in linearity and efficiency with harmonic injection were published in [46].

  A Doherty power amplifier operating at 10 GHz with an output power of 4.2 W and PAE $>$ 47%. For a 10 MHz OQPSK signal, the ACPR was measured to be > 30 dBc at maximum output power. The supply modulation experiment shows a Doherty power amplifier operating with $> 40\%$ PAE at more than 6 dB back off from maximum power. Results from this section of the chapter are reported in [128].

  A Class-E amplifier fabricated in a $f_T > 300$ GHz process was demonstrated. The measured PAE at 9 GHz was $> 55\%$ and the design shows the efficiency limitations of a high-f_T process.

- Chapter 3 - Analysis and Design of a Reverse-Channel V-band VCO - contains the design, fabrication and testing of a U- and V-band voltage controlled oscillator. The oscillator design process is explained from a circuit and layout standpoint for an advanced GaN

MMIC process. AM and traditionally machined WR-15 and WR-19 housings were designed, created and assembled and show the feasibility of AM components at millimeter-wave frequencies. A U-band and V-band microstrip-to-waveguide transition was designed and integrated on-chip with the VCO. The measured results show operation in the 40.99 to 42.88 GHz range with reduced output power due to a low g_m and incomplete ground plane due to fabrication problems.

- Chapter 4 - Analysis and Design of 235 GHz GaN-on-SiC Amplifiers - contains analysis, design and measurement of two power combined, multistage PAs. The analysis of even- and odd-mode operation for symmetrical power combiners was detailed and the stability analysis technique introduced in Chapter 5 was used to analyze potential even- and odd-mode instabilities without the need for additional EM simulations. A CPW-to-waveguide transition was designed and integrated on the 2nd PA design to allow for easier waveguide integration and to avoid the use of bondwires. The fabricated 3-stage PA was measured at HRL in the 200-260 GHz range and showed a similar $|S_{11}|$ and $|S_{21}|$ compared to simulation, with a reduced gain due to a lower f_t due to fabrication problems.

- Chapter 5 - Stability Analysis in Microwave Circuits - details a new method of analyzing stability in microwave PAs. The method is compared to existing techniques, including a commercially-available software package, and it is shown that the new method can avoid errors associated with single current injection based techniques. The method is validated on single- and two-stage amplifiers and predicts measured oscillations in those circuits. The technique is being used in the research group as an additional stability check for new PA designs.

- Chapter 6 - Millimeter-wave Component Integration Methods - contains the results of work on W-band AM waveguide components. Surface roughness is measured using FVM and it is shown that widely used models for predicting loss due to surface roughness are not accurate for the very rough surfaces typically created with AM techniques. The thermal analysis of

the millimeter-wave 4-stage power combined amplifier from Chapter 4 is presented and an AM heat pipe solution for transfering heat is demonstrated. Results from the chapter are reported in [129].

Bibliography

[1] C. Campbell, *Microwave Monolithic Power Amplifier Design, Wiley Encyclopedia of Electrical and Electronics Engineering.* John Wiley and Sons, Inc (Published Online), April 2013.

[2] EOS GmbH, "General Functional Principle of Laser-Sintering," http://www.eos.info/additive_manufacturing/for_technology_interested.

[3] Agilent Technologies, "Wireless LAN at 60 GHz - IEEE 802.11ad Explained," http://www.cs.odu.edu/~cs752/papers/milli-008.pdf.

[4] A. Margomenos, M. Micovic, C. Butler, B. T. Holden, D. T. Chang, C. McGuire, and D. H. Chow, "Low Loss, Cu Damascene Interconnects and Passives Compatible with GaN MMIC," *IEEE MTT-S International Microwave Symposium Digest*, 2013.

[5] T. Lacrevaz, B. Flechet, A. Farcy, J. Torrens, M. Gros-Jean, C. Bermond, T. Vo, O. Cueto, B. Blampey, G. Angenieux, J. Piquet, and F. de Crecy, "Wideband Frequency and In-Situ Characterization of High Permittivity Insulators for HF Integrated Passives," *Microelectric Engineering*, vol. 83, pp. 2184–2188, 2006.

[6] M. Siracusa, Z. Lemmios, and D. M. Maki, "Advanced Processing Techniques for GaAs Monolithic Integrated Circuits," *International Electron Device Meeting*, 1980.

[7] K. Shinohara, D. C. Regan, Y. Tang, A. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. Fung, A. Schmitz, T. C. Oh, S. J. Kim, P. S. Chen, R. G. Nagele, A. Margomenos, and M. Micovic, "Scaling of GaN HEMTs and Schottky Diodes for Submillimeter-Wave MMIC Applications," *IEEE Trans. on Electron Devices*, vol. 60, no. 10, 2013.

[8] M. Micovic, D. Brown, D. Regan, J. Wong, J. Tai, A. Kurdoghlian, F. Herrault, Y. Tang, S. D. Burnham, H. Fung, A. Schmitz, I. Khalaf, D. Santos, E. Prophet, H. Bracamontes, C. McGuire, and R. Grabar, "Ka-Band LNA MMICs Realized in $f_{max} < 580$ GHz GaN HEMT Technology," *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2016.

[9] A. Platzker and W. Struble, "Rigorous Determination of the Stability of Linear N-Node Circuits from Network Determinants and the Appropiate Role of the Stability Factor K of Their Reduced Two-Ports," *Third International Workshop on Integrated Nonlinear Microwave and Millimeterwave Circuits*, 1994.

[10] Qorvo, "TGA2312-FL 9-10 GHz 60 Watt GaN Power Amplifier," http://www.qorvo.com/products/p/TGA2312-FL, 2017.

[11] Thermacore Corp., "Multi-Kilowatt Heat Pipe Heat Sink Performance," http://www.thermacore.com/news/multi-kilowatt-heat-pipe.aspx, 2017.

[12] M. Varonen, R. Reeves, P. Kangaslahti, L. Samoska, J. Kooi, K. Cleary, R. Gawande, A. Akgiray, A. Fung, T. Gaier, S. Weinreb, A. Readhead, C. Lawrence, S. Sarkozy, and R. Lai, "An MMIC Low-Noise Amplifier Design Technique," *IEEE Trans. on Microwave Theory and Techniques*, vol. 64, no. 4, 2016.

[13] S. Marsh, *Practical MMIC Design*. Artech House, 2006.

[14] R. S. Pengelly and J. A. Turner, "Monolithic Broadband GaAs FET Amplifiers," *IEEE Electronic Letters*, vol. 12, no. 10, 1976.

[15] V. Radisic, W. R. Deal, K. M. K. H. Leong, X. B. Mei, W. Yoshida, P.-H. Liu, J. Uyeda, A. Fung, L. Samoska, T. Gaier, and R. Lai., "A 10-mW Submillimeter-Wave Solid-State Power-Amplifier Module," *IEEE MTT-S International Microwave Symposium Digest*, vol. 58, no. 7, pp. 1903–1909, July 2010.

[16] Y. Kawasaki, K. Shirakawa, Y. Ohashi, and T. Saito, "60-GHz Monolithic Oscillator Using InGaP/InGaAs/GaAs HEMT Technology," *IEEE MTT-S International Microwave Symposium Digest*, 1995.

[17] V. Radisic, K. M. K. H. Leong, X. Mei, S. Sarkozy, W. Yoshida, P.-H. Liu, J. Uyeda, R. Lai, and W. Deal, "A 50 mW 220 GHz Power Amplifier Module," *IEEE MTT-S International Microwave Symposium Digest*, pp. 45–48, May 2010.

[18] M. Micovic, A. Kurdoghlian, H. P. Moyer, P. Hashimoto, A. Schmitz, I. Milosavljevic, P. J. Wiladsen, W. S. Wong, J. Duvall, M. Hu, M. Wetzel, and D. H. Chow, "GaN MMIC Technology for Microwave and Millimeter-wave Applications," *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2005.

[19] A. M. et al, "GaN Technology for E, W and G-Band Applications," *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2014.

[20] I. Kallfass, J. Antes, T. Schneider, F. Kurz, D. Lopez-Diaz, S. Diebold, H. Massler, A. Leuther, and A. Tessman, "All Active MMIC-Based Wireless Communications at 220 GHz," *IEEE Trans. on Terahertz Science and Tech*, vol. 1, no. 2, 2011.

[21] Z. Griffith, M. Urteaga, P. Rowell, and R. Pierson, "190-260 Ghz High Power, Broadband PAs in 250nm InP HBT," *2015 IEEE Compound Semiconductor Integrated Circuit Symposium*, 2015.

[22] H. Wang, L. Samoska, T. Gaier, A. Peralta, H.-H. Liao, Y. Leong, S. Weinreb, Y. C. Chen, M. Nishimoto, and R. Lai, "Power-Amplifier Modules Covering 70-113 GHz Using MMICs," *IEEE Trans. on Microwave Theory and Techniques*, 2001.

[23] I. Kallfass, P. Pahl, H. Massler, A. Leuther, A. Tessmann, S.Koch, and T.Zwick, "A 200 GHz Monolithic Integrated Power Amplifier in Metamorphic HEMT Technology," *IEEE Microwave and Wireless Component Letters*, 2009.

[24] K. J. Herrick, K. W. Brown, F. A. Rose, C. S. Whelan, J. Kotce, J. Laroche, and Y. Zhang, "W-band Metamorphic HEMT with 267 mW Output Power," *IEEE MTT-S International Microwave Symposium Digest*, 2005.

[25] J. Hacker, M. Urteaga, D. Mensa, R. Pierson, M. Jones, Z. Griffith, and M. Rodwell, "250 nm InP DHBT Monolithic Amplifiers with 4.8 db gain at 324 GHz," *IEEE MTT-S International Microwave Symposium Digest*, 2008.

[26] S. Sarkozy, M. Vukovic, J. Padilla, J. Chang, G. Tseng, P.Tran, P. Yocom, W. Yamasaki, K. Leong, and W. Lee, "Demonstration of a G-Band Transceiver for Future Space Crosslinks," *IEEE Trans. on Terahertz Science and Tech.*, vol. 3, no. 5, 2013.

[27] D. Ingram, Y. Chen, J.Kraus, B. Brunner, B. Allen, H. Yen, and K. Lau, "A 427 mW, 20Amplifier," *1999 IEEE RFIC Symposium*, 1999.

[28] J.-H. Tsai and T.-W. Huang, "A 38-46 GHz MMIC Doherty Power Amplifier Using Post-Distortion Linearization," *IEEE Microwave and Wireless Component Letters*, 2009.

[29] P. Harati, A. Tessmann, D. Schwantuschke, R. Henneberger, and I. Kallfass, "E-band Transmitter with 29 dBm RF Power for Satellite Communication," *Proc. of 46th European Microwave Conference*, 2016.

[30] Cree Corporation, "Cree Silicon Carbide Substrates and Epitaxy," https://www.macrogroup.ru/sites/default/files/uploads/catalog/silovaya_electronika/CREE/matcatalog.pdf, 2017.

[31] I. Angelov, H. Zirath, and N. Rorsman, "Validation of a Nonlinear Transistor Model by Power Spectrum Characteristics of HEMTs and MESFETs," *IEEE Trans. on Microwave Theory and Techniques*, 1995.

[32] AWR Corporation, "Advanced Compatible Angelov HEMT Model," https://awrcorp.com/download/faq/english/docs/Elements/ANGELOV2C2.htm#angelov2c2_ref1.

[33] Keysight Technologies, "Agilent EEHEMT1 Model Equations," http://edadocs.software.keysight.com/display/iccap2012/Agilent+EEHEMT1+Model+Equations.

[34] S. Edstaller, "Additive Manufacturing for mm-Wave Waveguide Components," 2016.

[35] SwissTo12 Corp., http://http://www.swissto12.com/.

[36] X. Shang, P. Penchev, C. Guo, M. J. Lancaster, S. Dimov, Y. Dong, M. Favre, M. Billod, and E. de Rijk, "W-band Waveguide Filters Fabricated by Laser Micromachining and 3D Printing," *IEEE Trans. on Microwave Theory and Techniques*, vol. 64, no. 8, 2016.

[37] A. Bleicher, "LTE-Advanced is the Real 4G," http://spectrum.ieee.org/telecom/standards/lte-advanced-is-the-real-4g, 2013.

[38] Markets and Markets (Markets&Markets.com), "Mobile Phone & Smartphone Market Global Forecast (2010-2015)," 2011.

[39] Visiongain Corporation, "Global LTE Base Station Market 2013-2018: The Next Generation Infrastructure for 4G Mobile Telecommunications," 2013.

[40] O. Jardel, J. Mazeau, S. Piotrowicx, D. Caban-Chastas, E. Chartier, E. Morvan, P. Dueme, Y. Mancuso, and S. L. Delage, "Gan Power MMIC for X-band T/R Modules," *Microwave Integrated Circuits Conference (EuMIC)*, pp. 17–20, 2010.

[41] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power Amplifiers and Transmitters for RF and Microwave," *IEEE Trans. on Microwave Theory and Techniques*, vol. 50, 2002.

[42] A. AlMuhaisen, J. Lees, S. C. Cripps, P. Tasker, and J. Benedikt, "Wide Band High-Efficiency Power Amplifier Design," *European Microwave Integrated Circuits Conference*, 2011.

[43] A. Dani, M. Roberg, and Z. Popovic, "PA Efficiency and Linearity Enhancement Using External Harmonic Injection," *IEEE Trans. on Microwave Theory and Techniques*, vol. 60, 2012.

[44] P. Colantonio, F. Giannini, G. Leuzzi, and E. Limiti, "Harmonic Tuned PAs Design Criteria," *IEEE MTT-S International Microwave Symposium Digest*, 2002.

[45] S. R. Schafer, M. P. Litchfield, A. Zai, C. Campbell, and Z. Popovic., "X-Band MMIC GaN Power Amplifiers Designed for High-Efficiency Supply-Modulated Transmitters," in *IEEE MTT-S International Microwave Symposium Digest*, 2013, pp. 1–3.

[46] A. Dani, M. Coffey, and Z. Popovic, "Efficient Linear Supply-Modulated PA with Harmonic Injection," *Proc. of 43rd EuMW*, 2013.

[47] C. F. Campbell, K. Tran, M. Kao, and S. Nayak, "A K-Band 5W Doherty Amplifier MMIC Utilizing 0.15um GaN on SiC HEMT Technology," *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2012.

[48] A. Zai, "Efficient Supply-Modulated Transmitters for Variable Amplitude Radar," Ph.D. dissertation, 2015.

[49] A. Zai, D. Li, S. Schafer, and Z. Popovic, "High-Efficiency X-Band MMIC GaN Power Amplifiers with Supply Modulation," *IEEE MTT-S International Microwave Symposium Digest*, 2014.

[50] P. T. Theilmann, J. J. Yan, C. Vu, J. Moon, H. P. Moyer, and D. F. Kimball, "A 60 MHz Bandwidth High Efficiency X-Band Envelope Tracking Power Amplifier," *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2013.

[51] P. Colantonio, F. Giannini, R. Giofre, and L. Piazzon, "Experimental Results of an X-band MMIC Doherty Power Amplifier," *Microwave and Optical Technology Letters*, vol. 53, no. 11, 2011.

[52] E. L. P. Colantonio, F. Giannini, *High Efficiency RF and Microwave Solid State Power Amplifiers*. John Wiley and Sons, Inc, 2009.

[53] D. Kang, J. Choi, D. Kim, and B. Kim, "Design of Doherty Power Amplifiers for Handset Applications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 58, pp. 2134–2142, 2010.

[54] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty Power Amplifier," *Microwave Magazine*, vol. 7, no. 5, pp. 42–50, 2006.

[55] N. O. Sokal and A. D. Sokal, "Class E - A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. SC-10, no. 3, 1975.

[56] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Artech House, 2006.

[57] K. A. Jaggers, "V-Shaped Gate GaAs MESFET for Improved High-Frequency Performance," *IEEE Electronic Letters*, vol. 11, 1976.

[58] T. B. Mader, "Quasi-Optical Class-E Power Amplifiers," Ph.D. dissertation, 1995.

[59] T. Mader and Z. Popovic, "The Transmission Line High-Efficiency Class-E Amplifier," *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 9, 1995.

[60] J. Leckey, "A New Current Dependent Gate Charge Model for GaN HFET Devices," *Proc. of 11th European Microwave Integrated Circuit Conference*, 2016.

[61] N. Ramanan, B. Lee, and V. Misra, "Device Modeling for Understanding AlGaN/GaN HEMT Gate-Lag," *IEEE Trans. on Electron Devices*, vol. 61, no. 6, 2014.

[62] D. K. Choi and S. I. Long, "A Phyisically Based Analytic Model of FET Class-E Power Amplifiers - Designing for Maximum PAE," *IEEE Trans. on Microwave Theory and Techniques*, vol. 47, no. 9, 1999.

[63] ——, "The Effect of Transistor Feedback Capacitance in Class-E Power Amplifiers," *IEEE Trans. of Circuits and Systems, I*, vol. 50, no. 12, 1999.

[64] M. A. Y. Medina, "RF Power Amplifier for Wireless Communications," Ph.D. dissertation, University of Leuven, June 2008.

[65] M. A. Y. Medina, D. Schreurs, and B. Nauwelaers, "RF Class-E Power Amplifier Design Based on a Load Line-Equivalent Capacitance Method," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 3, 2008.

[66] FCC, "Revision of Part 15 of the Commission's Rules Regarding Operation in the 57-64 GHz Band FCC-13-112," https://apps.fcc.gov/edocs_public/attachmatch/FCC-13-112A1_Rcd.pdf, 2013.

[67] Boeing Defense and Space, "Boeing Satellites - Milstar II," http://www.boeing.com/defense-space/space/bss/factsheets/government/milstar_ii/milstar_ii.html, 2010.

[68] Northrop Grumman Corporation, "Milstar Payloads," http://www.northropgrumman.com/Capabilities/MilstarPayloads/Pages/default.aspx, 2017.

[69] P. B. de Selding, "Boeing Proposed Big Satellite Constellations in V- and C-bands." http://spacenews.com/boeing-proposes-big-satellite-constellations-in-v-and-c-bands/, 2016.

[70] C. Henry, "FCC Gets Five New Applications for Non-geostationary Satellite Constellations," http://spacenews.com/fcc-gets-five-new-applications-for-non-geostationary-satellite-constellations, 2017.

[71] Space Exploration Technologies Corp., "FCC Petition, Purpose of Experiment," https://apps.fcc.gov/els/GetAtt.html?id=185534&x=, 2016.

[72] A. Toprak, M. T. Haliloglu, Y. Durmus, O. A. Sen, and E. Ozbay, "Effect of Gate Field Plate and γ-Gate Structures on RF Power Performance of AlGaN/GaN HEMTs," *Proc. of 10th European Microwave Integrated Circuits Symp.*, 2015.

[73] J. Papp and Y. Koyano, "An 8-18 GHz YIG-Tuned FET Oscillator," *IEEE Trans. on Microwave Theory and Techniques*, vol. 28, 1980.

[74] P. Brand, "Tunable Low Noise GaAs FET Oscillators at 13 GHz," *13th European Microwave Conference*, 1983.

[75] P. C. Wade, "Novel FET Power Oscillator," *IEEE Electronic Letters*, vol. 14, 1978.

[76] F. S. Correra and E. Camargo, "18 GHz Reverse Channel HEMT Oscillator," *IEEE MTT-S International Microwave Symposium Digest*, 1990.

[77] K. M. K. H. Leong, W. R. Deal, V. Radisic, X. B. Mei, J. Uyeda, L. Samoska, A. Fung, T. Gaier, and R. Lai, "A 340-380 GHz Integrated CB-CPW-to-Waveguide Transition for Sub Millimeter-Wave MMIC Packaging," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 6, pp. 413–415, June 2009.

[78] OML Inc., "Average Atmospheric Absorption of Millimeter Waves," https://www.omlinc.com/images/pdf/Library/References/41-090507_Atmospheric_Aborption_Millimeter_Waves.pdf.

[79] P. Siegel, "THz for Space: The Golden Age," *IEEE MTT-S International Microwave Symposium Digest*, 2010.

[80] A. Pazmany and M. Wolde, "A Compact Airborne G-Band Water Vapor Radiometer and Retrievals of Liquid Cloud Parameteres from Coincident Radiometer and Millimeter Wave Radar Measurements." *Mircorwave Radiometry and Remote Sensing of the Environment*, 2008.

[81] Information, M. o. I. A. Communication Council, and Communications, "Report on the Efficient Use of Frequency Bands for Mobile Phones." [Online]. Available: http://www.soumu.go.jp/main_sosiki/joho_tsusin/policyre-ports/joho_tsusin/bunkakai/pdf/081211_1_si1-2.pdf

[82] H. Song and T. Nagatsuma, "Present and Future of Terahertz Communications," *IEEE Trans. on Terahertz Science and Tech.*, vol. 1, no. 1, 2011.

[83] M. I. Skolnik, *Introduction to Radar Systems*, 3rd ed. McGraw-Hill, 2001.

[84] B. Wallace, "DARPA MMW System Programs and How They Drive Technology Needs," http://www.ece.ucdavis.edu/dmrc/files/2014/09/Bruce_wallace_darpa_web.pdf, DARPA, 2014, dMRC Millimeter-Wave Technology Workshop.

[85] B. Hwang, N. Lim, J.-H. Park, S. Jin, M. Kim, J. Jung, B. Kwon, J. Hong, J. Han, D. Kwak, J. Park, J.-D. Choi, and W.-S. Lee, "Development of 38nm Bit-Lines using Copper Damascene Process for 64-Giga Bits NAND Flash," *IEEE Advanced Semiconductor Mfg. Conference*, 2008.

[86] M. Inohara, I. Tamura, H. Koike, Y. Enomoto, S. Arakawa, T. Watanabe, E. Ide, S. Kadomura, and K. Sunouchi, "High Performance Copper and Low-k Interconnect Technology Fully Compatible to 90 nm-node SOC Applications," *IEDM, International Electron Device Meeting*, 2002.

[87] M. Roberg and C. Campbell, "A Novel Even and Odd-Mode Symmetric Circuit Decomposition Method," *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2013.

[88] J. M. Rollett, "Stability and Power-Gain Invariants of Linear Twoports," *IRE Trans. Circuit Theory*, vol. 9, pp. 29–32, Mar. 1962.

[89] L. Samoska, K.-Y. Lin, H. Wang, Y.-H. Chung, M. Aust, S. Weinreb, and D. Dawson, "On the Stability of Millimeter-Wave Power Amplifiers," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 1, 2002, pp. 429–432.

[90] A. Platzker, W. Struble, and K. T. Hetzler, "Instabilities Diagnosis and the Role of K in Microwave Circuits," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1185–1188, 1993.

[91] S. Kassim and F. Malek, "Microwave FET Amplifier Stability Analysis Using Geometrically-Derived Stability Factors," *Intelligent and Advanced Systems (ICIAS), 2010 International Conference on*, pp. 1–5, 2010.

[92] W. Struble and A. Platzker, "A Rigorous Yet Simple Method for Determining Stability of Linear N-Port Networks," *IEEE GaAs IC Symposium*, 1993.

[93] V. Rizzoli and A. Lipparini, "General Stability Analysis of Periodic Steady-State Regimes in Nonlinear Microwave Circuits," *IEEE Trans. on Microwave Theory and Techniques*, vol. 33, no. 1, pp. 30–37, Jan 1985.

[94] R. G. Freitag, "A Unified Analysis of MMIC Power Amplifier Stability," *IEEE MTT-S International Microwave Symposium Digest*, pp. 297–300, 1992.

[95] C. Barquinero, A. Suarez, A. Herrera, and J. L. Garcia, "Complete Stability Analysis of Multifunction MMIC Circuits," *IEEE Trans. on Microwave Theory and Techniques*, vol. 55, no. 10, pp. 2024–2033, 2007.

[96] R. D. Middlebrook, "Measurement of Loop Gain in Feedback Systems," *International Journal of Electronics Theoretical and Experimental*, vol. 38, no. 4, pp. 485–512, 1975.

[97] S. Mons, R. Quere, T. Peyretaillade, and J. Obregon, "Nonlinear Stability Analysis of MMIC Power Amplifiers," in *Microwave Conference, 1998. 28th European*, vol. 2, Oct 1998, pp. 114–118.

[98] S. Dellier, R. Gourseyrol, G. Soubercaze-Pun, J. Collantes, A. Anakabe, and K. Narendra, "Stability Analysis of Microwave Circuits," in *Wireless and Microwave Technology Conference (WAMICON), 2012 IEEE 13th Annual*, April 2012, pp. 1–5.

[99] A. Suarez, V. Iglesias, J. M. Collantes, J. Jugo, and J. L. Garcia, "Nonlinear Stability Analysis of Microwave Circuits Using Commercial Software," *IEEE Electronics Letters*, vol. 34, no. 13, pp. 1333–1335, 1998.

[100] R. D. Martinez and R. C. Compton, "A General Approach for the S-parameter Design of Oscillators with 1 and 2-Port Active Devices," *IEEE Trans. on Microwave Theory and Techniques*, vol. 40, no. 3, pp. 569–574, Mar 1992.

[101] A. Suarez and R. Quere, *Stability Analysis of Nonlinear Microwave Circuits*, 1st, Ed. Artech House, 2003.

[102] S. Dellier, "Software Simplifies Stability Analysis," *Microwave and RF Magazine*, vol. 5A-054, 2012.

[103] J. M. Collantes, "Expanding the Capabilities of Pole-Zero Identification Techniques for Stability Analysis," *IEEE MTT-S International Microwave Symposium Digest*, June 2009, Boston.

[104] R. D. Middlebrook, "Null Double Injection and the Extra Element Theorem," *IEEE Transactions on Education*, vol. 32, pp. 167–180, Aug. 1989.

[105] ——, "The General Feedback Theorem: A Final Solution for Feedback Systems," *IEEE Microw. Mag.*, vol. 7, no. 2, pp. 50–63, 2006.

[106] F. Wiedmann, https://sites.google.com/site/frankwiedmann/loopgain, Feb. 2014.

[107] H. Nyquist, "Regeneration Theory," *Bell Systems Technical Journal*, vol. 11, pp. 126–147, Jan. 1932.

[108] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics, 2nd Edition*, 2nd ed. Springer, 2004, pg. 362 - 368.

[109] J. Montejo-Garai, I. O. Saracho-Pantoja, C. A. Leal-Sevillano, J. A. Ruiz-Cruz, and J. M. Rebollar, "Design of Microwave Waveguide Devices for Space and Ground Application Implemented by Additive Manufacturing," *2015 Intl. Conf. on Electromagnetics in Adv. Appl.*

[110] J. Thornton, B. Dalay, and D. Smith, "Additive Manufacturing of Waveguides for Ku-Band Satellite Communications Antenna," *IEEE Electronics Letters*, vol. 48, no. 25, 2012.

[111] A. Dimitriadis, M. Farve, M. Billod, J. Ansermet, and E. de Rijk, "Design and Fabrication of a Lightweight Additive-Manufactured Ka-Band Horn Antenna Array," *2016 10th Euro. Conf. on Antennas and Propagation*, 2016.

[112] M. D'Auria, W. J. Otter, J. Hazell, B. T. Gillatt, C. Long-Collins, N. M. Ridler, and S. Lucyszyn, "3-D Printed Metal-Pipe Rectangular Waveguides," *IEEE Trans. on Components, Packaging and Manufacturing Tech.*, vol. 5, no. 9, 2015.

[113] B. Zhang and H. Zirath, "3D Printed Iris Bandpass Filters for Millimeter-Wave Applications," *IEEE Electonics Letters*, vol. 51, no. 22, 2015.

[114] B. Zhang, Z. Zhan, Y. Cao, H. Gulan, P. Linner, J. Sun, T. Zwick, and H. Zirath, "Metallic 3D Printed Antennas for Millimeter-and Submillimeter Wave Applications," *IEEE Trans. on Terahertz Science and Tech.*, vol. 6, no. 4, 2016.

[115] E. N. Grossman, M. Gould, and N. Mujica-Schwann, "Robust Evaluation of Statistical Surface Topography Parameters Using Focus-Variation Microscopy," *Surface Topography: Metrology and Properties*, vol. 4, no. 3, 2016.

[116] M. V. Lukic and D. S. Filipovic, "Modeling of 3D Surface Roughness Effects With Application to μ-Coaxial Lines," *IEEE Trans. on Microwave Theory and Techniques*, vol. 55, no. 3, 2007.

[117] E. Hammerstad and O. Jensen, "Accurate Models of Computer Aided Microstrip Design," *IEEE MTT-S International Microwave Symposium Digest*, 1980.

[118] S. Groiss, I. Bardi, O. Biro, K. Preis, and K. R. Richter, "Parameteres of Lossy Cavity Resonators Calculated by the Finite Element Method," *IEEE Trans. on Magnetics*, vol. 32, no. 3, 1996.

[119] Maxim Integrated Corp., "Temperature Range Summary," https://www.maximintegrated.com/en/markets/military-aerospace/temperature-range-summary.html, 2017.

[120] Intel Corp., "Enhanced Temperature Device Support," https://www.altera.com/products/common/temperature/ind-temp.html, 2017.

[121] D. B. Rutledge, *The Electronics of Radio*. Cambridge University Press, 2008.

[122] J. Fiala, M. R. Overholt, and S. Motakef, "Thermal Considerations in a Low Cost T/R Module Design," *35th Annual GOMACTech Conference*, 2010.

[123] IFIXIT Corp., "Samsung Galaxy S7 Teardown," https://www.ifixit.com/Teardown/Samsung+Galaxy+S7+Teardown/56686, 2016.

[124] A. Faghri, "Heat Pipes: Review, Opportunities, and Challenges," *Frontiers in Heat Pipes*, vol. 5, 2014.

[125] B&K Engineering, *Heat Pipe Design Handbook*, 1979, vol. I.

[126] V. Zomorrodian, M. Roberg, T. Nguyen, and W. Gaieski, "Stability Analysis of Multi-Finger GaN FET Cells for High Power MMIC Design," *IEEE MTT-S International Microwave Symposium Digest*, 2016.

[127] A. Dani, M. Coffey, and Z. Popovic, "4W x-Band High Efficiency MMIC PA with Output Harmonic Injection," *Proc. of 44th European Microwave Conference*, 2014.

[128] M.Coffey, P. Momenrookdai, A. Zai, and Z. Popovic, "A 4.2-W 10-GHz GaN MMIC Doherty Power Amplifier," *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2015.

[129] M. Coffey, S. Verploegh, S. Edstaller, S. Armstrong, E. Grossman, and Z. Popovic, "Additive Manufactured W-band Waveguide Components," *IEEE MTT-S International Microwave Symposium Digest*, 2017.