A 4-W K-Band 40% PAE Three-Stage MMIC Power Amplifier

Maxwell R. Duffy*, Gregor Lasser*, Michael Roberg†, and Zoya Popović*
*Department of Electrical, Computer, and Energy Engineering, University of Colorado, Boulder, CO, USA
†Infrastructure and Defense Products, Qorvo, Richardson, TX, USA

***Abstract*—This paper presents the design and measured continuous wave (CW) performance of a three-stage K-band MMIC power amplifier with greater than 4 W peak output power and a peak power added efficiency (PAE) ranging from 40-45 %. The output power exceeds 3.2 W over the frequency range of 18 to 24 GHz with less than 1.5 dB variation. The MMIC is implemented in Qorvo's 150-nm GaN on SiC process. The three stage architecture enables greater than 20dB of saturated gain from 18.5-24 GHz.**

***Index Terms*—Power amplifiers, efficiency, GaN, MMIC, broadband**

I. Introduction

oOne of the standard frequency ranges for satellite communications is K band, spanning approximately 18-27 GHz [1]. For increased spectral efficiency, multi-carrier signals with over 1 GHz instantanous bandwidths and high peak-to-average power ratios (PAPR) are desired. Gallium Nitride (GaN) solid-state power amplifiers are explored for these satellite applications as an alternative to TWTs, and are therefore required to operate very efficiently. GaN-based Doherty PAs [2] and linear amplifiers [3] have been explored to this end. Published K-band GaN PAs include a single-frequency [4] and broadband two-stage designs [2], [5] in a commercial GaN-on-SiC process. Other three-stage [3], [6] and two-stage PAs [7] have been demonstrated in research GaN processes, as summarized in Table I.

The work presented in this paper demonstrates a three-stage reactively matched K-band GaN MMIC amplifier, shown in Fig.1a, fabricated in the Qorvo 150-nm process. The design maximizes efficiency while reaching a target peak output power of 4 W and peak saturated gain of 25 dB, while exceeding 3.2 W and 20 dB over the 18.5-24 GHz frequency range. The paper presents the design flow, starting with transistor sizing and network design, stability analysis, and measured results for several amplifier die.

II. Design considerations

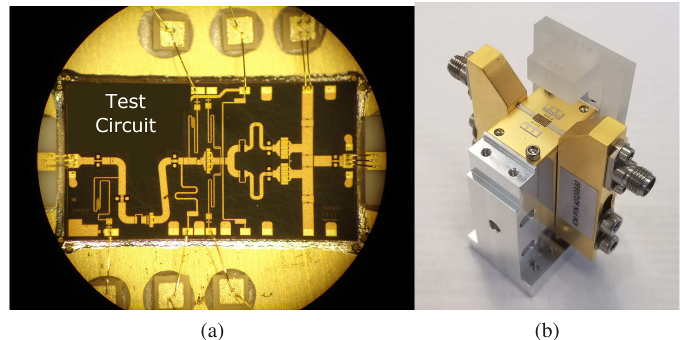
The PA design presented in this paper is implemented in the Qorvo 150-nm GaN on SiC process and targets the K band. The process uses 100 μm substrate and slot vias, and the transistors make use of internal source vias. An $8{\times}100\,\mu$m transistor with a 15/52 pitch is chosen; pairs of 15 µm spaced gates with internal source vias within the 52 µm spacing between pairs. A nonlinear model (EEHEMT in NI/AWR Microwave Office) supplied by Qorvo, validated up to 18 GHz, is extrapolated above K band. The bias point is selected to match the point of model validation, V_{D}=20 V with 100 mA/mm. Based on simulated load-pull data, this transistor can produce greater than 2 W output power at 20.5 GHz.

To meet the design target output power of 4 W, two transistors are combined in the output stage. With the specification requiring 30 dB of small-signal gain, a three stage design is selected. The chosen staging ratio for the transistors is 1:2:8. This ensures that the current draw of the two driver stages has a minimum impact on the total efficiency of the amplifier. The first and second driver stages use $4{\times}50\,\mu$m and $8{\times}50\,\mu$m transistors. The models for these devices are intended to simulate accurately operation from 18-35 GHz.

TABLE I
Comparison of Different K-Band GaN Amplifiers

Freq.	Frac. BW	P_{out}	PAE	Gain	Ref.
26	-	33.5	42	8	2017 [4]
21-23	9.1	37	48	16.7	2012 [2]
18-20	10.5	31	22	16	2014 [6]
18-19	5.4	40	30	20	2016 [7]
20.8-22.4	7.4	39.5	35	22	2016 [3]
17.2-20.2	16	40	38	18	2017 [5]
18.5-24	**26**	**36.5**	**40**	**25**	**This work**

Peak values at saturation are shown for all table entries.
Freq. (GHz), Frac. BW (%), P_{out} (dBm), PAE (%), Gain (dB)



(a) (b)

Fig. 1. (a) Photograph of the 3-stage K-band MMIC mounted on a CuMo carrier and bonded to 10-mil alumina microstrip lines at input and output. 100 pf bypass capacitors are bonded to the 6 bias pads. Three bondwires connect the amplifier RF bond pads to the alumina input and output lines. A single bondwire is used for all DC bias lines excluding the final stage where DC current draw is the highest. (b) Photograph of chip in fixture. The CuMo carrier is attached to an aluminum heat sink. The plastic mount and spring-loaded pins supply DC bias to amplifier.

978-1-5386-6502-2/18/$31.00 ©2018 IEEE

III. Amplifier Design

A. Source Pull and Load Pull

The initial source-pull characterization is simulated by driving the biased transistor with a continuous wave (CW) signal and measuring the voltage, V_1, and current, I_1, at the first harmonic at the gate of the device. Using these measurements, a fundamental impedance, Z_S, and a reflection coefficient, Γ_S, for the source of the device are calculated as:

$$Z_\text{S} = \frac{V_1}{I_1} \qquad \Gamma_\text{S} = \frac{Z_\text{S} - Z_0}{Z_\text{S} + Z_0} \tag{1}$$

This results in a "large signal" reflection coefficient. Rather than using traditional source pull scripts, this method is used to reduce simulation complexity, and is shown to be in agreement with other source-pull methods. Over the course of a load pull simulation, this value is iterated as the transistor output loading changes.

A load pull is performed at 21 GHz, the center frequency of the design band (18-24 GHz). The optimum output reflection coefficient, Γ_L, for maximum power-added efficiency (PAE) is then converted into a parallel RC network for each device at the gate and drain, and used for matching. This impedance is found from:

$$Z_\text{L} = \left(\frac{1+\Gamma_\text{L}}{1-\Gamma_\text{L}}\right) \cdot Z_0 \tag{2}$$

The conjugate of this value is then transformed into an admittance Y_L^* which is used to create an equivalent parallel R_p and C_p network:

$$Y_\text{L}^* = \frac{1}{Z_\text{L}^*} \qquad R_\text{p} = \frac{1}{\Re e\{Y_\text{L}^*\}} \qquad C_\text{p} = \frac{\Im m\{Y_\text{L}^*\}}{\omega} \tag{3}$$

This RC network is used to model the port impedance at the gate and drain of the transistor.

B. Matching Network Synthesis

In a power-combined amplifier consisting of two transistors (referred to as 1 and 2), S parameters of the passive power-combining network do not give the correct impedance at the active device ports. For the 3-port power combining network shown in Fig. 2, port 1 and 2 are the transistor drains with the port impedances found from load pull, while port 3 is the output of the network loaded with 50 Ω. Assuming equivalent sources driving ports 1 and 2 and an undriven port 3:

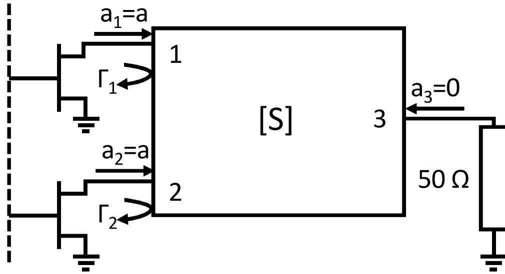


Fig. 2. Network diagram of 3-port power combiner.

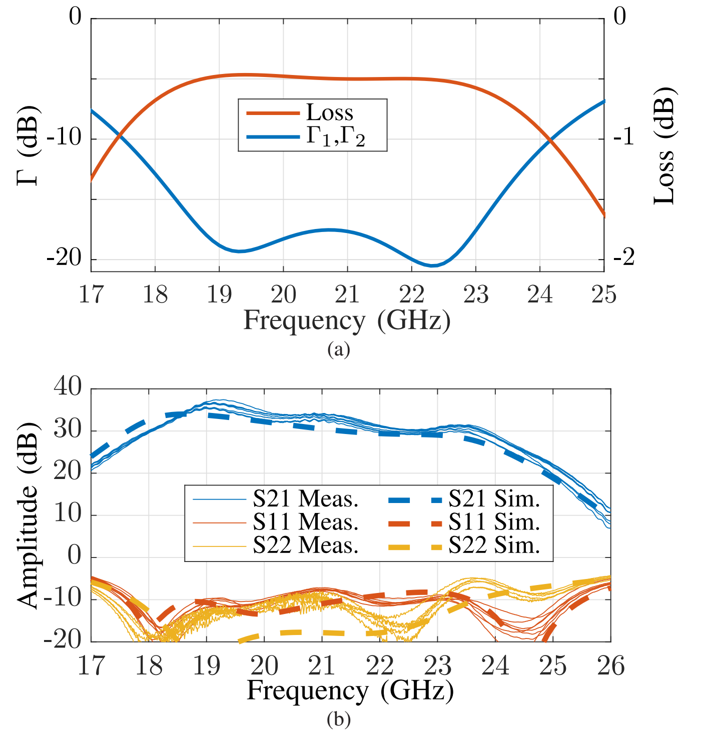


Fig. 3. (a) Simulated loss and reflection coefficients for the power combiner network in the final stage of the PA. (b) Measured S-parameters for eight chips (solid) compared to simulated S-parameter data (dashed).

$$\begin{aligned} a_1 &= a_2 = a \\ a_3 &= 0 \end{aligned} \tag{4}$$

the S-parameter representation of this three port network is:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a \\ a \\ 0 \end{bmatrix} \tag{5}$$

With the above assumptions, the reflection coefficient Γ_1, which takes into account coupling from other ports, becomes:

$$\begin{aligned} b_1 &= (S_{11} + S_{12}) \cdot a \\ \Gamma_1 &= S_{11} + S_{12} \end{aligned} \tag{6}$$

In equation (6) the reflection seen at port 1 would not be S_{11} but rather the summation of S_{11} and the leakage from port 2, S_{12}. This results in an active S-parameter for the transistor output.

S parameters are also used to estimate matching network loss, L_M, in terms of the power delivered to the load, P_DL, and the power available to the combiner, P_A:

$$L_\text{M} = \frac{P_\text{DL}}{\text{P}_\text{A}} \tag{7}$$

Using the assumptions made in (4), the power delivered to the load becomes:

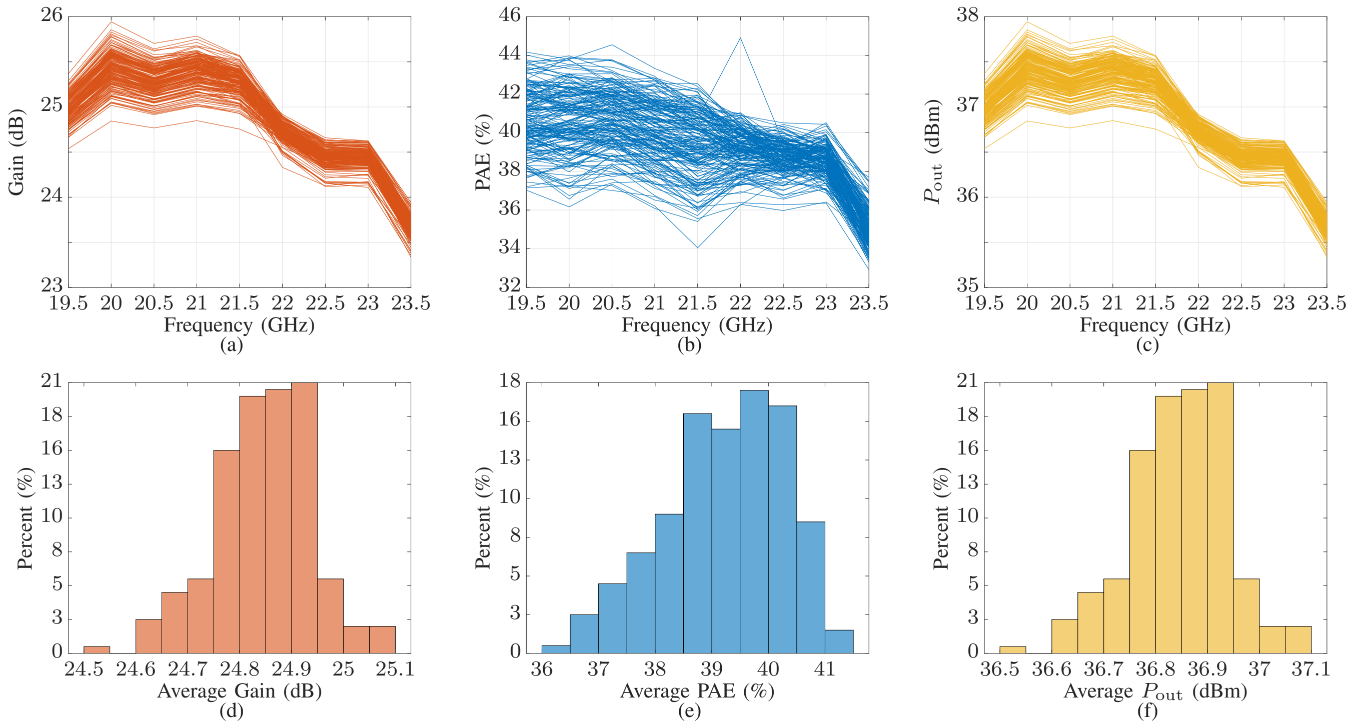


Fig. 4. Measured gain (a), PAE (b) and output power (c) vs. frequency across multiple wafers at 11 dBm input drive. Related histograms (d)-(f) show mean performance over the band.

$$P_{\mathrm{DL}} = (|b_3|^2 + |a_3|^2) = |b_3|^2 = |S_{31} + S_{32}|^2 \cdot |a|^2 \tag{8}$$

and the power available at the input ports of the combiner is found to be:

$$P_{\mathrm{A}} = (|a_1|^2 + |a_2|^2) = 2 \cdot |a|^2 \tag{9}$$

combining these the network loss can be approximated as:

$$L_{\mathrm{M}} = \frac{|S_{31} + S_{32}|^2}{2} \tag{10}$$

This analysis is illustrated in Fig. 3a, which shows the combining network loss and the reflection coefficient magnitudes at the two active device ports. Because the design is symmetric about the final stage, the two transistors see the same reflection coefficient. The same approach is followed for all three stages of the PA. Once the topology is determined, small and large signal models are used for a final optimization of the matching networks. Concurrent small and large signal optimization was performed to ensure maximum large signal performance while maintaining stability, gain flatness (small-signal gain >30 dB with ±1.5 dB flatness), and match ($|S_{11}|$ and $|S_{22}|$ <-10 dB). It should be noted that all bypass capacitors, both at gate and drain, are minimized to allow supply modulation characterization in the future.

C. Stability Analysis

The K factor is not sufficient for stability analysis of multi-stage power-combining amplifiers [8], therefore a loop-gain analysis is performed [9] under large and small signal operation at various bias points. Parallel RC and RLC circuits are used to correct for these potential instabilities and avoid directly placing a resistor in the RF path. Odd mode stability is evaluated for the the final stage and resistors added [10].

IV. Measured Performance

The amplifier measures a small signal gain of 33 dB with a ±3 dB gain variation from 18-24 GHz presented in Fig. 3b. The input return loss is better than 10 dB from 17.5-25 GHz, with good agreement between simulated and measured results for the amplifier mounted and packaged as shown in Fig. 1b. Simulations take into account a bondwire transition and the input and output of the DUT, but not the microstrip to 2.9 mm coaxial connector transition at the edges of the CuMo Carrier. All testing is done with a 20 V drain bias a 100 mA/mm quiescent current.

On-wafer pulsed performance across 5 wafers is seen in Fig. 4 for a 100 µs pulse with a 10 % duty cycle. Results for 12 dBm input drive power are shown for the fabricated chips with outliers discarded. Large signal gain varies ±1 dB from 19.5-23.5 GHz. The PAE is around 40 % and the output power >36 dBm across the band of interest. Note that some of the variation may be due to poor probe contact during testing.

Large signal VNA measurements of the chips are done using the connectorized fixture shown in Fig. 1b. The large

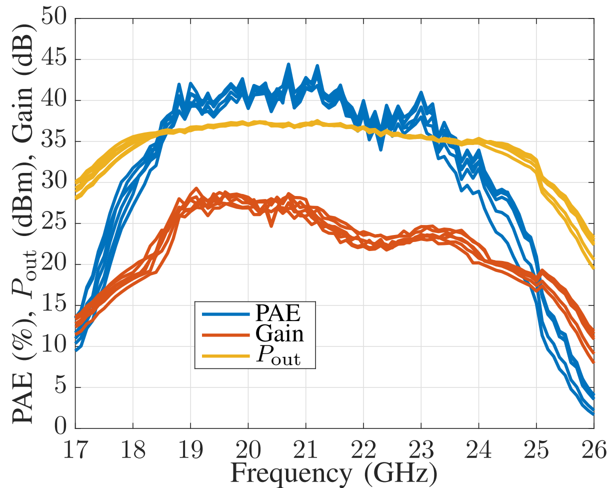


Fig. 5. Measured large signal amplifier performance at maximum PAE point.

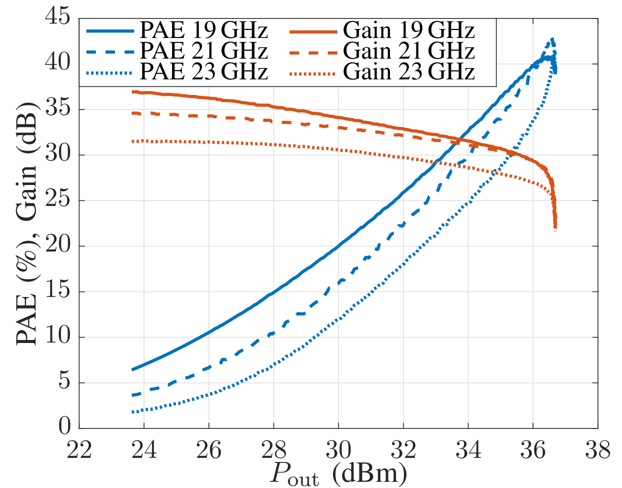


Fig. 7. Measured large signal amplifier saturation curves for three frequencies.

signal performance over frequency for the chips is shown in Fig. 5. The measurements shown a large signal gain variation of ±2.5 dB about 25 dB from 18.5-23.5 GHz. Large signal performance drops off at 18.5 GHz on the low end and 23.5 GHz on the high end with >35 % PAE for that band. Saturated output power for this band peaks above 36 dBm.

In Fig. 7 gain and PAE curves are shown for three discrete frequencies across the band. The PA saturates at the same output power point at the three frequencies and is compressed by 3-5 dB at the point of maximum PAE.

The third order carrier to interference (C/I) ratio can be seen in Fig. 6 for three tone spacings at 20 GHz carrier frequency. The C/I ratio degrades as function of tone spacing peaking just over 20 dB when the amplifier is saturated.

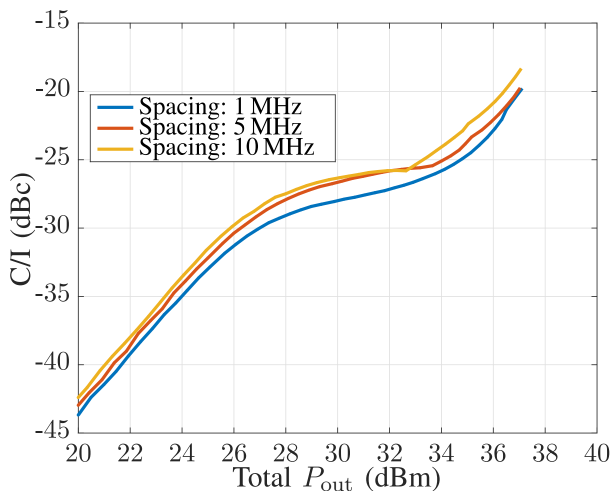


Fig. 6. Third order C/I ratio of the amplifier at 20 GHz for three tone spacings: 1 MHz, 5 MHz, and 10 MHz.

V. Conclusion

The performance and design methodology of a three stage K-band MMIC are presented. The operational bandwidth of the amplifier goes from 18.5 GHz to 24 GHz for a greater than 25 % fractional bandwidth. The MMIC shows greater than 4 W peak output, a peak efficiency exceeding 40 %, and a saturated gain greater than 22 dB.

Acknowledgment

This work was funded by Lockheed Martin award S16-025.

References

[1] B. G. Evans, *Satellite communication systems*. Iet, 1999, vol. 38.

[2] C. F. Campbell, K. Tran, M.-Y. Kao, and S. Nayak, "A k-band 5w doherty amplifier mmic utilizing 0.15 μm gan on sic hemt technology," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2012 IEEE*. IEEE, 2012, pp. 1–4.

[3] Y. S. Noh and I. B. Yom, "A linear gan high power amplifier mmic for ka-band satellite communications," *IEEE Microwave and Wireless Components Letters*, vol. 26, no. 8, pp. 619–621, 2016.

[4] M. A. Reece, S. Contee, and C. W. Waiyaki, "K-band gan power amplifier design with a harmonic suppression power combiner," in *RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), 2017 IEEE Topical Conference on*. IEEE, 2017, pp. 92–95.

[5] S. Din *et al.*, "High-power k-band gan pa mmics and module for npr and pae," in *Microwave Symposium (IMS), 2017 IEEE MTT-S International*. IEEE, 2017, pp. 1838–1841.

[6] O. Cengiz, O. Sen, and E. Ozbay, "High power k-band gan on sic cpw monolithic power amplifier," in *Microwave Conference (EuMC), 2014 44th European*. IEEE, 2014, pp. 1492–1495.

[7] C. Friesicke, P. Feuerschütz, R. Quay, O. Ambacher, and A. Jacob, "A 40 dbm algan/gan hemt power amplifier mmic for satcom applications at k-band," in *Microwave Symposium (IMS), 2016 IEEE MTT-S International*. IEEE, 2016, pp. 1–4.

[8] A. Platzker, W. Struble, and K. T. Hetzler, "Instabilities diagnosis and the role of k in microwave circuits," in *1993 IEEE MTT-S International Microwave Symposium Digest*, June 1993, pp. 1185–1188 vol.3.

[9] K. Wang, M. Jones, and S. Nelson, "The s-probe-a new, cost-effective, 4-gamma method for evaluating multi-stage amplifier stability," in *1992 IEEE MTT-S Microwave Symposium Digest*, June 1992, pp. 829–832 vol.2.

[10] R. G. Freitag, "A unified analysis of mmic power amplifier stability," in *1992 IEEE MTT-S Microwave Symposium Digest*, June 1992, pp. 297–300 vol.1.