Efficient Supply Modulated MMIC PAs for Broadband Linear Amplification

by

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Zoya Popović

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Gregor Lasser

Date _____

The final copy of this thesis has been examined by the signatories, and we

find that both the content and the form meet acceptable presentation standards

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Duffy, Maxwell Robert (Ph.D., Electrical Engineering)

Efficient Supply Modulated MMIC PAs for Broadband Linear Amplification

Thesis directed by Professor Zoya Popović

High data rate radio frequency (RF) communications require complex spectrally efficient modulation schemes, with time domain waveforms which have high peak-average power ratios (PAPR). These systems demand larger instantaneous bandwidths (>100 MHz) of the transmitters and, in these applications, the power amplifier (PA) tends consume and dissipate a large fraction of the total power. Improving the efficiency of this element is critical to overall system performance and thermal management. However the PAPR of the signal reduces the efficiency by forcing the PA to be operated away from its peak output power and thus away from the peak efficiency operation.

In this thesis efficiency enhancement is addressed through the use of supply modulation. In this approach, the supply voltage changes dynamically with the input amplitude of the modulated drive signal keeping the PA in compression, and thus operating more efficiently but normally degrading linearity. This work focuses on the design of "shaping functions", which are the relationship between the dc supply and signal envelope, to improve supply modulator efficiency without degrading amplifier linearity or system efficiency. The techniques developed are specifically meant to address the kind of broadband signals becoming prevalent in today's wireless communication systems, including cellular and satellite.

One of the challenges in supply modulation is the need for a high-speed dynamic dc supply. This work explores a method for reducing the speed requirements of the dynamic supply known as power tracking. It is shown that the power tracking method can be extended to multi-signal envelope tracking. The new approach is demonstrated with a high-efficiency octave bandwidth (2-4 GHz) GaN power amplifier. Next, multi-signal efficient amplification is shown using two 10 MHz LTE signals spaced 800 MHz apart, using a new supply modulation shaping function, and an efficiency improvement is demonstrated for a linearized PA.

Then, a method to improve linearity and gain of a drain supply-modulated PA is discussed. A two-stage GaN X-band PA is tested at 9.7 GHz, using a single discrete supply modulator for both stages.

Simultaneously, the gate biases of the transistors in the two stages are varied independently for a 20 MHz modulation bandwidth. Performing gate and drain bias modulation provides the efficiency improvement see in drain supply modulation, as well as improved linearity performance by dynamically adjusting the gain and compensating for the phase variation in saturation.

Lastly a three-stage GaN MMIC K-band PA is tested at 19.8 GHz with drain supply modulation. The discrete shaping function is designed to increase efficiency while improving linearity over that obtained with a static supply. Using several methods to reduce the switching speed requirements for the supply modulator, modulation bandwidths of 100 MHz and 250 MHz are both demonstrated. With these techniques, efficiency is improved with no degradation in linearity.

Dedication

To Robert.

Acknowledgments

This is the first part of the thesis I wrote. I did this to ensure that I would not be frustrated while doing it and thankful to everyone involved. Maybe by the time I've written this long and grueling document there will be people I wished I had not included. On the other hand there may be people I wished I did include. I am sorry that I don't have the foresight to be to able to see who I should and shouldn't be thankful to. I've only ever been good at seeing whats right in front of me.

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Chapter 1

Introduction

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1.1 Motivation and Background

Higher data rate communication systems require complex spectrally efficient modulation schemes, with time domain waveforms which have high peak-average power ratios (PAPR). In cellular applications 5G communication standards demand larger instantaneous bandwidths (>100 MHz) while simultaneously proposing a single amplifier for multiple simultaneous channels, known as carrier aggregation [1,2]. For satellite communication systems the trend to move away from single vacuum tube amplifiers (TWTs) and parabolic antennas to solid state power amplifiers (SSPAs) in large phased arrays, pictured in Fig. 1.1, is driving performance needs for individual amplifiers due to the large number of elements; a slight improvement is compounded by the number elements in the system [3]. In both of these applications the power amplifier (PA) tends to be the system element consuming, and dissipating, the most power [4]. Improving the efficiency of this element is critical to overall system performance and thermal management [5]. A problem in these systems is that

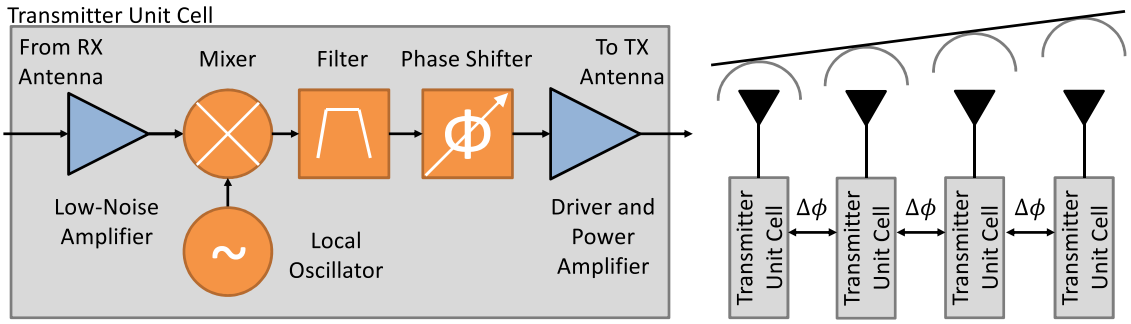


Figure 1.1: Simplified block diagram of a phased array transmitter.

the PAPR of a signal reduces the efficiency of the amplifier by forcing the PA to be backed-off from its peak power and thus away from the peak efficiency operation.

1.1.1 Communication Signals

To increase data rates, wireless communications systems are making use of more complicated modulation schemes. Doing this allows more data throughput without increasing signal bandwidth, known as "spectral efficiency". In the time domain, these communication signals can be visualized as in Fig. 1.2a. The signal has in-phase (I) and quadrature (Q) components which are are 90 degrees out of phase. Throughout this work the input signal envelope will be referred to as V_{in} and is defined:

$$V_{\text{in}} = \sqrt{I^2 + Q^2} \tag{1.1}$$

Variation of the envelope is amplitude modulation (AM). There is also a phase modulation (PM) component visualized through the instantaneous amplitude difference between the I and Q signal component. The AM and PM of the signal is best visualized on a polar plot as shown in Fig. 1.2b, where the PM is the angle of the instantaneous data points from the origin and the AM is the signal variation from a constant value. Spectrally efficiency signals, such as Quadrature Amplitude Modulation (QAM), make use of both amplitude and phase modulation.

The distribution of a signal can be visualized by its probability density function (PDF), seen in Fig. 1.3a for a noise-like signal. From looking at this plot someone familiar with statistics (or signal processing)

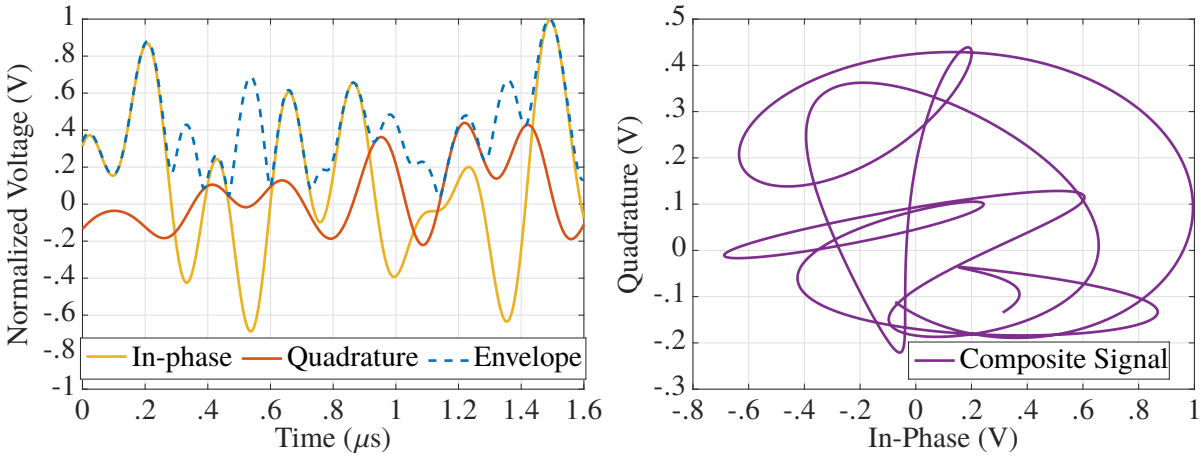


Figure 1.2: Plots showing 1.6 μs of a 10 MHz noise-like signal. (a) Decomposed signal plotted in the time domain with the envelope overlaid. (b) Polar plot as a function of the I and Q components. The instantaneous distance from the origin (0,0) is the envelope of the signal.

might be able to recognize that the amplitudes of the signal have a Rayleigh distribution. While this is meaningful, for an amplifier designer it is often more practical to think of the PDF not plotted linearly but rather logarithmically as seen in Fig. 1.3b. Though it is not always the case (ie. a bi-modal distribution) for this signal the difference between the peak probability point and the peak amplitude point (0 dB normalized) approximately corresponds to the PAPR of the signal, which here is $\sim$ 10 dB. This means that to transmit this signal linearly (defined here as not compressing any amplitude information) through an amplifier, one would have to operate the amplifier in 10 dB output power backoff (OPB).

Linearity has multiple definitions based on different ways of viewing modulated signals [6]. In the time domain, linearity will be defined in terms of error vector magnitude (EVM), normalized mean square error (NMSE), or bit-error rate (BER). Time domain linearity metrics measure the deviation of the received signal from the ideal transmit signal as seen in Fig. 1.4b-1.4a. These variations in the transmitted time domain signal lead to distortion in the frequency domain. Frequency based linearity metrics include adjacent channel power ratio (ACPR), noise power ratio (NPR), and third order intermodulation distortion (IMD3). This work mainly accesses linearity in the frequency domain due to the high cost of spectrum and importance of spectral confinement. The distortion caused by a PA can be seen in the frequency domain in Fig. 1.4c-1.4d. Note that the bandwidth of the signal expands.

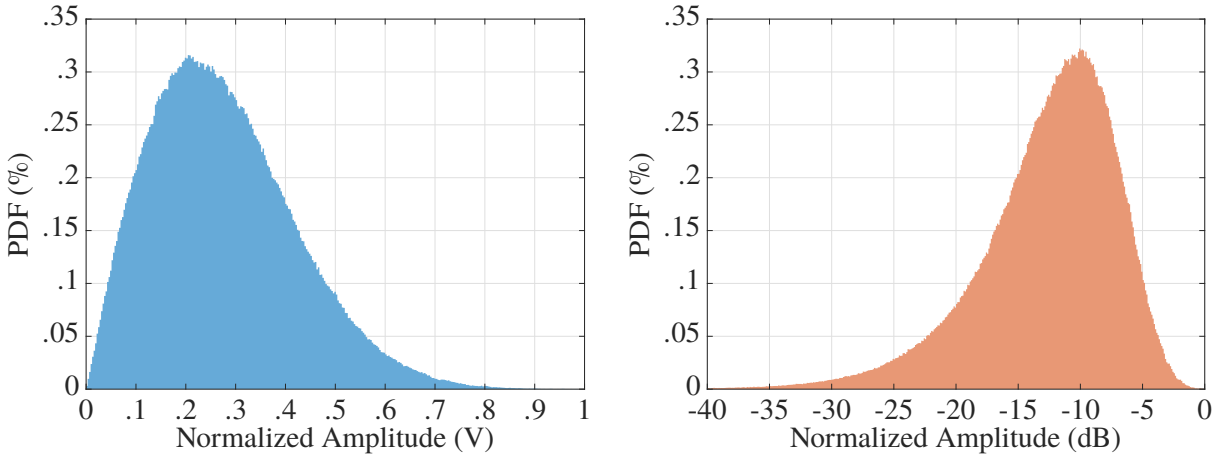


Figure 1.3: Probability density function of a complex gaussian noise-like signal with 10 dB PAPR as a function of amplitude: (a) linearly (b) logarithmically.

The main linearity metrics used in this work are NMSE, EVM, ACPR, and NPR. NMSE is defined as the difference between the input signal x and output signal y, seen in Fig. 1.4a, normalized by the input signal:

$$\text{NMSE(dB)} = 10 \cdot \log_{10} \frac{\sum_n |x(n) - y(n)|^2}{\sum_n |x(n)|^2} \tag{1.2}$$

EVM is defined in terms of a demodulated signal. The metric looks at a ratio of the deviation between the input symbol, x_{sym}, and output symbol, y_{sym}, seen in Fig. 1.4b, normalized by the input symbol. It is very similar in form to NMSE but is calculated using the information at the symbols as opposed to whole signal:

$$\text{EVM(dB)} = 10 \cdot \log_{10} \frac{\sum_n |x_{\text{sym}}(n) - y_{\text{sym}}(n)|^2}{\sum_n |x_{\text{sym}}(n)|^2} \tag{1.3}$$

EVM is also commonly shown as a percentage calculated:

$$\text{EVM(\%)} = 100 \cdot \sqrt{\frac{\sum_n |x_{\text{sym}}(n) - y_{\text{sym}}(n)|^2}{\sum_n |x_{\text{sym}}(n)|^2}} \tag{1.4}$$

ACPR, seen in Fig. 1.4d, is defined as the ratio between the average power in the main channel, P_{main}, and the adjacent channel, P_{adj}, as defined by the communication standard used:

$$\text{ACPR(dB)} = 10 \cdot \log_{10} \frac{P_{\text{adj}}}{P_{\text{main}}} \tag{1.5}$$

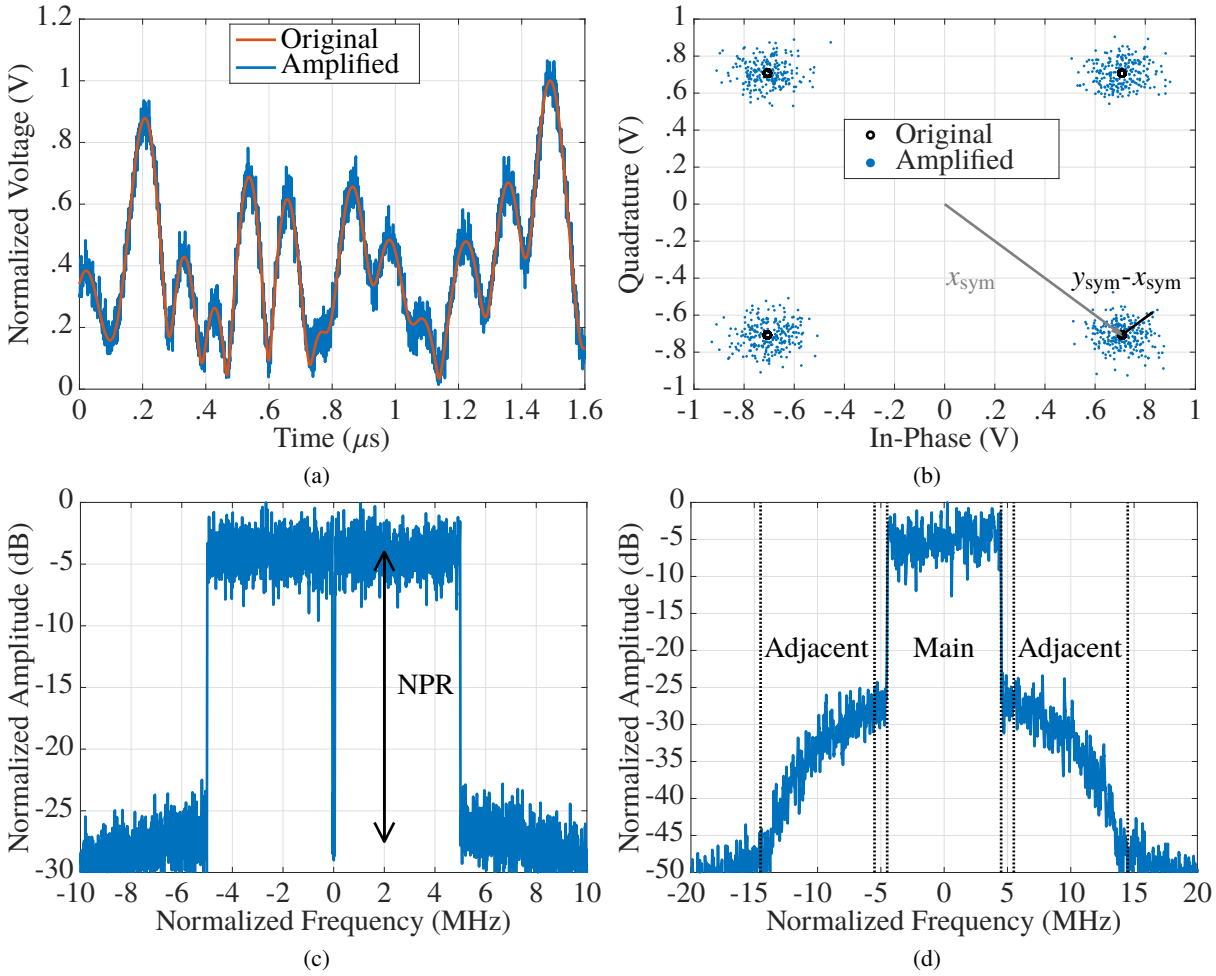


Figure 1.4: Comparison of different linearity metrics after amplification in the time domain: (a) 10 MHz signal, and (b) polar demodulated 4-QAM signal. In the frequency domain: (c) 10 MHz noise-like signal, (d) 10 MHz LTE signal.

Similarly NPR, seen in Fig. 1.4c, is the defined as the ratio between the noise-signal power, P_{main}, and the notched center frequency power, P_{notch}, which is normally notched to 1-10 % of the signal bandwidth :

$$\text{NPR(dB)} = 10 \cdot \log_{10} \frac{P_{\text{noise}}}{P_{\text{notch}}} \tag{1.6}$$

The deviation between the ideal originally generated signal and actual received signal is normally caused by transmission through an element that is non-linear, such as a PA. Though inherently non-linear a as a PA does have a (fairly) linear region, however this area of operation (particularly for an AM modulated signal) is backed-off from the peak efficiency point. The implications of this are important. An amplifier designer

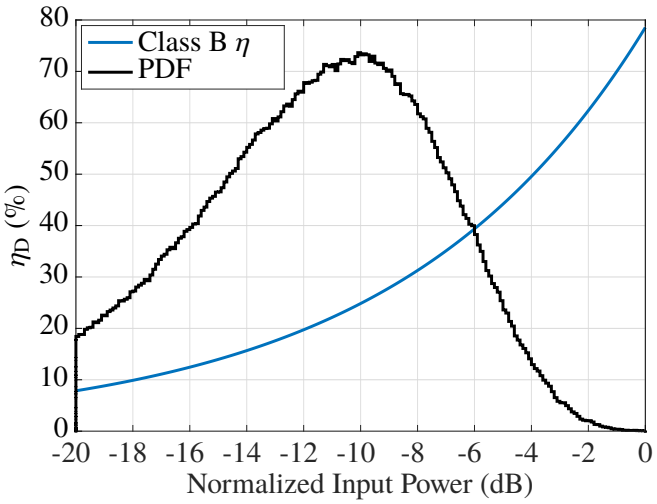


Figure 1.5: Drain efficiency for an ideal class B amplifier with PDF of a 10 dB PAPR noise-like signal overlaid.

is often interested in maximizing the efficiency of their amplifier which can be defined in multiple ways relating the RF power out (P_{out}), RF power in (P_{in}), or dc power (P_{dc}). There are two main metrics that will be used in this work drain efficiency (η_{D}):

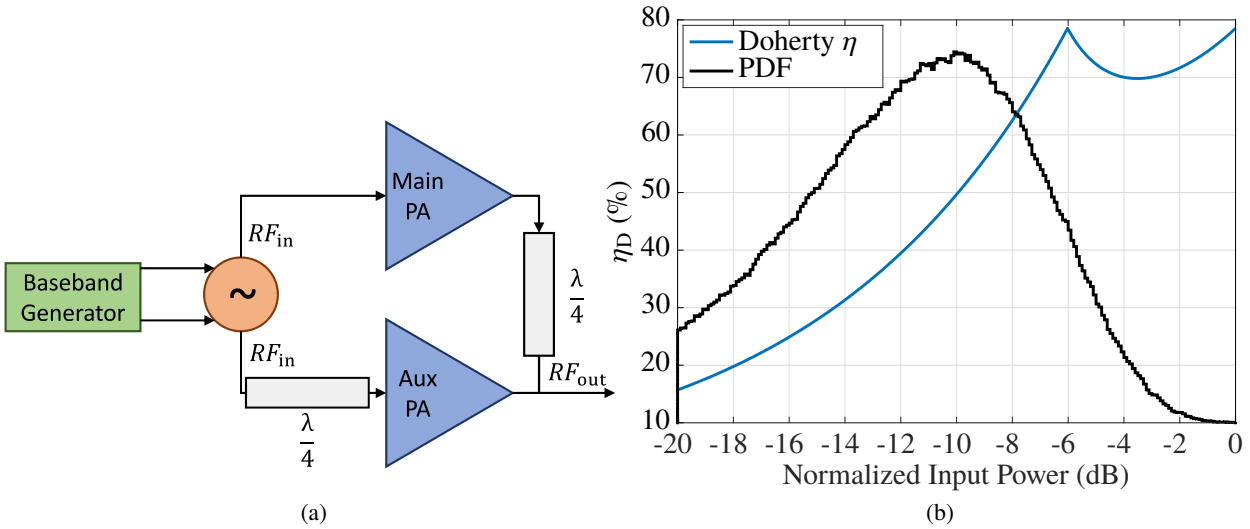
$$\eta_{\text{D}} = \frac{P_{\text{out}}}{P_{\text{dc}}} \tag{1.7}$$

and power added efficiency (PAE):

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{dc}}} \tag{1.8}$$

For an amplifier with a high gain (>20 dB), the input power, P_{in}, will be dwarfed by the output power, P_{out}, and $\eta_{\text{D}} \approx$PAE. For amplification of a constant envelope signal (no AM) as in radar, a high peak efficiency is critical. However for a modulated signal with a non-zero PAPR the efficiency in output backoff (OPBO) is the most important metric.

Taking the PDF from Fig. 1.3b and superimposing it onto PAE curves for an amplifier model one can see the disparity between the efficiency an amplifier can transmit with and the efficiency an amplifier can transmit with linearly, Fig. 1.5. An ideal class B amplifier [7, see Chapter 3] has a peak PAE of over 78.5 % but when operated with a modulated signal the average P_{out} must be reduced to prevent clipping of the signal



(a) (b)

Figure 1.6: (a) Block diagram for doherty amplifier and (b) drain efficiency for an ideal doherty PA with PDF of a 10 dB PAPR noise-like signal overlaid.

(loss of amplitude information). In this case operating the signal at a 10 dB lower P_{out} will reduce efficiency by over 50 percentage points (pp). A discussion of commonly used methods to address this follows.

It should be noted that throughout this work when modulated signals are discussed the power and efficiency being referred to are assumed to be the average values. When continuous wave (CW) results are being discussed the power and efficiency referred to are the instantaneous values. If peak performance values are being discussed the variable will be specifically annotated with a ($\wedge$).

1.1.2 Back-off Efficiency Enhancement

There are multiple ways to mitigate the reduction in efficiency during back-off operation. There are two common methods based on load-modulation: Doherty and outphasing architectures. Doherty PAs [8], seen in Fig.1.6a, are used in many cellular applications and are very popular because they are RF input - RF output amplifiers that do not require additional control circuity or a complicated drive scheme. A Doherty amplifier works by driving two (symmetric or asymmetric) transistors with a signal that is 90 ° out of phase. The "main" transistor is biased in class-AB (normally on) while the "aux" transistor is biased in class-C (normally off); the two outputs are separated by a $\frac{\lambda}{4}$ transformer. For low drive power levels the main transistor amplifies the signal. At higher power levels the peaking transistor turns on while the impedance

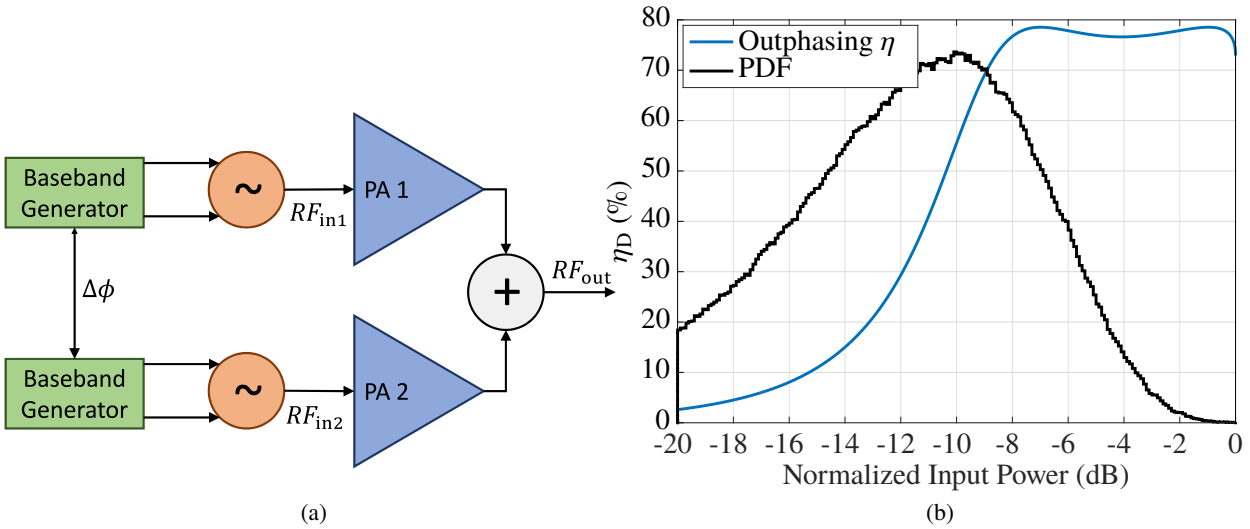
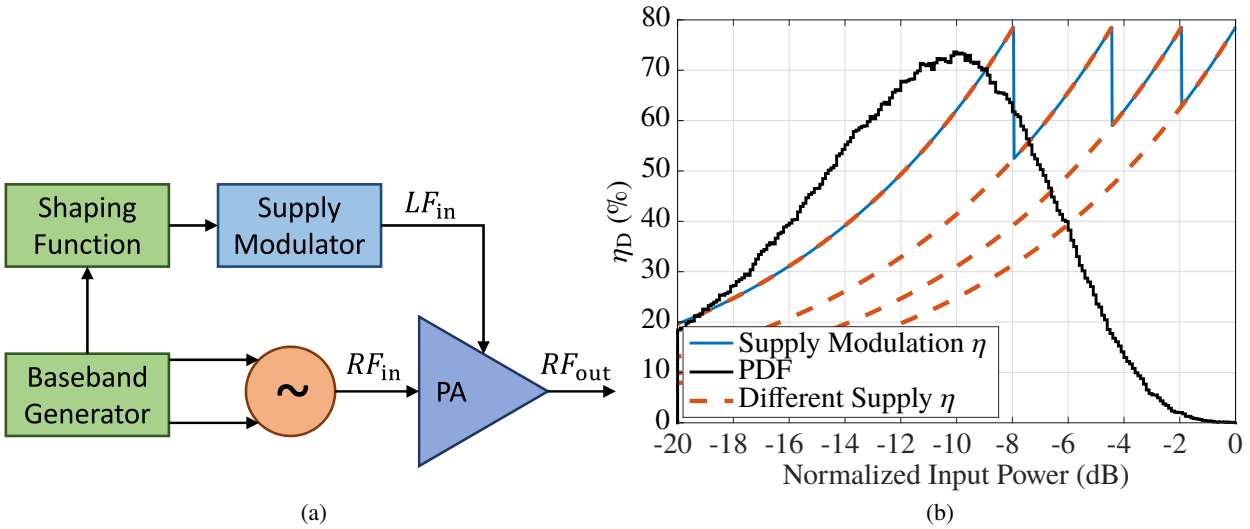


Figure 1.7: (a) Block diagram for outphasing amplifier and (b) drain efficiency for an ideal outphasing PA with PDF of a 10 dB PAPR noise-like signal overlaid.

transformer maintains operation of the main transistor. In a symmetric Doherty this results in a second peak in efficiency at the 6 dB back-off point of the amplifier as seen for an ideal case in Fig. 1.6b where average efficiency is increased by 25pp over the class-B case. Through asymmetric transistor selection the location of this second peak can be moved, for example to the 10 dB back-off point, making it more ideal for the signal shown in Fig. 1.6b. The Doherty's main limitation comes from the $\frac{\lambda}{4}$-transformer which limits the bandwidth from 10-20 % [9]. Work has performed done to over come this limit [10–13], however these are mainly implemented at lower frequencies (<6 GHz).

The outphasing (Chireix) PA [14], seen in Fig. 1.7a, is another load modulation method which has received renewed interest in recent years. An outphasing amplifier works by driving two amplifiers with a constant envelope signal into a non-isolated combiner. The phasing of the constant envelope signal is varied independently for the two transistors resulting in load modulation and a varying amplitude at the amplifier output. The outphasing combiner tends to make use of $\frac{\lambda}{4}$ transformers which are bandwidth limited. Additionally, two different RF drive signals need to be generated for the outphasing amplifier increasing system complexity by doubling hardware requirements. The drive signals are modified to have the correct phasing with an arc-cosine function, creating challenges for high instantaneous bandwidth signals [15]. An ideal outphasing PA as described in [16] is simulated in Fig. 1.7b, for B_s=.2. In this case the efficiency is



(a) (b)

Figure 1.8: (a) Block diagram for supply modulation amplifier and (b) drain efficiency for an ideal supply modulation PA with PDF of a 10 dB PAPR noise-like signal overlaid.

also improved over a class-B amplifier to approximately 60%. the second peak in efficiency could be moved further by changing the design of the outphasing combiner (the B_s). Work has been done to simplify the driving of an outphasing amplifier, through RF-input outphasing, however this has its own complications related to the design of the power splitting network [17].

This work primarily deals with efficiency enhancement through another method called supply-modulation, seen in Fig. 1.8a. In a supply modulation transmitter a dynamic supply is used with the amplifier to track the changing input signal envelope. By varying the drain supply to lower values when the drive signal is smaller, the amplifier can theoretically always be compressed and thus efficient. In Fig. 1.8b the PDF of the previously discussed noise-like signal is superimposed on top of ideal PAE curves for multiple drain voltages. Assuming that the peak PAE of each of these curves can be tracked, efficiency at 10 dB OPBO can be improved from 25 % to over 65 %.

Because supply modulation can theoretically be done on any amplifier, there is no intrinsic RF bandwidth limitation (as was the case with the load-modulated amplifiers). The bandwidth limitation is rather present in the baseband. The dynamic supply used must be able to track the envelope bandwidth of the amplifier. From (1.1) it can be seen that the square root is taken to determine the envelope of a signal resulting in an

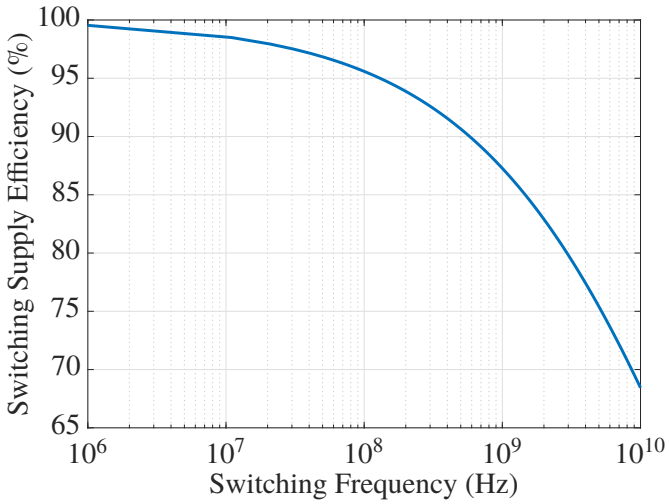


Figure 1.9: Switching supply modulator efficiency as a function of switching frequency.

infinite bandwidth. This can be seen in the series expansion of the square-root function:

$$\sqrt{x} = \sum_{n=1}^{\infty} \frac{(-1)^n(-1+x)^n(\frac{1}{2})_n}{n!} \approx a_0 + a_1x^1 + a_2x^2 + a_3x^3... \tag{1.9}$$

In reality one would only track the 5× the signal bandwidth and ignore the rest of the envelope data but even this is can be a very large amount. To effectively track the envelope of a 10 MHz signal requires a 50 MHz dynamic supply. Research has been done to overcome some of the baseband bandwidth constraints including: high switching speed integrated switching modulators and hybrid supply modulators, which will be lumped together as continuous supply modulators (CSM) [18–21], reduced switching speed discrete supply modulators (DSM) [22–24], and shaping function design [25–27]. In this work bandwidth constraints are overcome through use of DSMs, CSMs, and shaping functions (relationship between V_{in} and V_{D}) that limit the effective envelope bandwidth.

Doing supply modulation will introduce distortions into the amplifier output (these tend to be worse for a DSM versus a CSM). A main contribution of this work is looking into analog methods for linearity improvement specifically in the context of supply modulation transmitters. One important caveat to keep in mind is that the simulations in Fig. 1.8b curves assume a 100 % efficient supply modulator. In reality the efficiency of the supply, η_{SM}, will be multiplied by the efficiency of the power amplifier and this system efficiency, PAE_{S}, will be the number of greatest interest:

$$\mathrm{PAE_S} = \mathrm{PAE} \cdot \eta_{\mathrm{SM}} \tag{1.10}$$

When PAE is given it will be assumed to be ignoring the efficiency of the supply modulator circuit. When $\mathrm{PAE_{PS}}$ is given the efficiency will include the power stage efficiency of the supply modulator circuit, ignoring losses in the gate drivers. A more detailed explanation of the supply modulator circuits will be given in Chapter 3.

For the case in Fig. 1.8b the SM does not need to be very efficient to offer an improvement over a static supply, but when the need for performance is more strict (which it tends to be) supply modulator efficiency is crucial to maintaining a high system efficiency. As bandwidths (and thus switching speeds) are pushed higher, a reduction in supply modulator efficiency occurs [28, see (4.20-4.23)]. Using a simplified and optimistic model for a GaN RF transistor [29, see (30)] estimates of switching supply efficiency as a function of switching frequency can be determined, seen in Fig. 1.9.

1.2 Thesis Outline

This thesis demonstrates the design and testing of highly efficient power amplifiers for supply modulated transmitters. The specific focus of the work is on shaping function design to improve supply modulator efficiency without degrading amplifier linearity or system efficiency. The thesis is summarized as follows:

- In Chapter 2 the use of supply modulation is motivated. The benefits of supply modulation and techniques used to statically characterize an amplifier for supply modulation are discussed. This chapter serves as a foundation for the remainder of the thesis.

- Chapter 3 discusses test hardware and measurement methods. Hardware described includind amplifiers and supply modulators, as well as test benches used to characterize them. Three amplifiers, linear trackers (including gate and drain trackers), and MMIC-based discrete supply modulators are described. Measurement benches, calibration and alignment methods required to test SM-PA are presented followed by an overview of the test signals used.

- In Chapter 4 a method for overcoming the limitations of past slew rate reduction techniques, referred to as power envelope tracking, or just power tracking (PT), is investigated. First we present results for a single signal, followed by an extension to two widely separated signals. We show that the PT method used in conjunction with average SoE tracking results in a band-limited trajectory for multi-signal envelope tracking. The new approach is demonstrated with a high-efficiency octave bandwidth (2-4 GHz) GaN power amplifier. Several different trajectories for PT are designed and discussed in terms of bandwidth-reduction and linearity. The amplifier is tested using a 10-MHz LTE signal with supply modulation, and results with and without digital pre-distortion (DPD) are compared. Multi-signal efficient amplification is next shown using two 10-MHz LTE signals 800 MHz apart, using a new supply modulation trajectory, and efficiency improvement is demonstrated for a linearized PA. Then results for an X-band PA are shown with Peak SoE tracking of 3 signals at 200 MHz spacing, showing the limitations of this method as the number of signals increases.

- In Chapter 5, a method to improve linearity and gain of a drain supply-modulated PA is shown. A two-stage GaN X-band PA, described in Section 3.1.2, is tested at 9.7 GHz using a single dynamic supply modulator for both stages. Simultaneously, the gate biases of the transistors in the two stages are varied independently. An efficient discrete supply modulator, Section 3.2.2c, is used to generate the drain supply voltage, while two high-speed instrumentation amplifiers are used to drive the gates of the amplifier, Section 3.2.1b. Performing gate and drain bias modulation provides the efficiency improvement of drain supply modulation with improved linearity performance by dynamically adjusting the gain and compensating for the phase variation in saturation.

- Chapter 6 shows results for a three-stage reactively matched K-band GaN MMIC amplifier fabricated in the Qorvo 150-nm 28 V process. The design maximizes efficiency, with PAE exceeding 40 %, while reaching a target peak output power of 4 W and peak saturated gain of 25 dB. The output power exceeds 3.2 W with over 20 dB gain for the 18.5-24 GHz frequency range. Performance and design criteria are evaluated for a drain supply voltage range of 10-28 V, with a nominal bias point of 100 mA/mm for a drain voltage of 20 V. Discussed are the design flow, starting with transistor sizing and network design,

and a statistical analysis of 230 on-wafer probed amplifier chips.

- In Chapter 7 the three-stage GaN MMIC K-band PA discussed in Chapter 6 is tested at 19.8 GHz with drain supply modulation. An efficient GaN MMIC discrete supply modulator, discussed in Section 3.2.2b, is used to generate the drain supply voltage. The shaping function is designed to increase efficiency while improving linearity over that of a static supply. Using several methods to reduce the switching speed requirements for the supply modulator, a modulation bandwidth of 100 MHz and 250 MHz are both demonstrated. For 100 MHz signals with PAPR>10 dB, we demonstrate an average efficiency improvement from 14% to 20% with a simultaneous linearity improvement in NPR from 23 to 26 dB through a shaping function focused on gain linearization. For 250-MHz signal bandwidth, there is no observed degradation in NPR and the efficiency is improved by 5 percentage points.

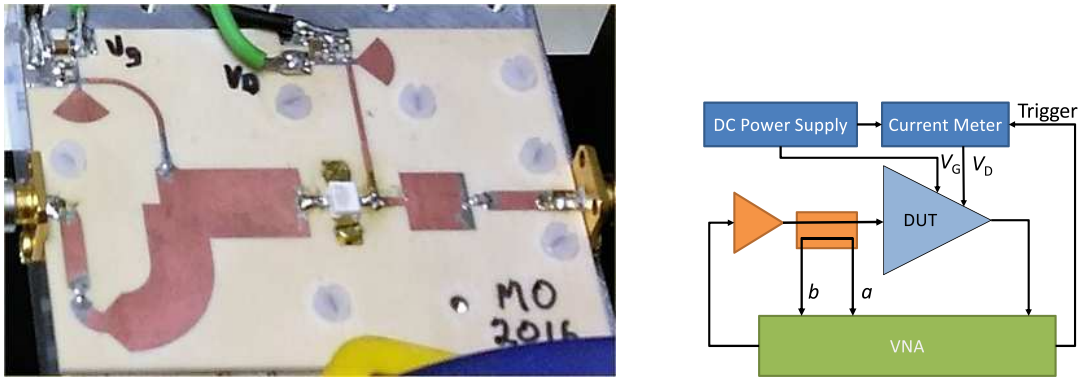
Chapter 2

Motivation for Supply Modulation

Contents

In this section static measurements are used to make estimates of dynamic amplifier performance under supply modulation operation. The results are used to discuss practical concerns of supply modulation for an amplifier originally designed and presented here [30]. The primary function of the static (CW) amplifier characterization is to develop a shaping function for use under dynamic (modulated signal) operation. Analog and digital linearization methods will be discussed to mitigate distortions introduced by supply modulation.

A shaping function (SF), sometimes also called a trajectory, is the relationship between the V_{in} of the amplifier and the V_{D} presented to the amplifier by the supply modulator. Shaping functions can be designed to maintain a certain mode of operation during supply modulation. The most common trajectories shown in this work and in the literature either aim to maintain a flat gain (constant gain or iso-gain) or aim to track the peak efficiency point of the amplifier [30–32].



(a) (b)

Figure 2.1: (a) 2.4 GHz harmonically tuned PA. (b) Simplified block diagram of setup used for testing. Forward, a, and reflected, b, waves are measured in front of the driver amplifier using a coupler.

To illustrate the importance of effective shaping function design for supply modulation, the case of the amplifier presented in [30] is discussed. The amplifier is designed using a CGH40010 10 W GaN-on-SiC transistor from Wolfspeed. The transistor has a flange package allowing easy mounting with a good electrical and thermal connection. The amplifier, shown in Fig. 2.1a, is designed to be stable with small on-chip bypass capacitors in the bias line. Bypass capacitors on the bias lines have a low-pass filtering effect. This can results in distortions to the envelope signal and a reduction in efficiency if capacitors are not made sufficiently small.

2.1 Large Signal VNA Test Bench

The amplifier is characterized on a large signal Vector Network Analyzer (VNA) measurement bench. An external coupler and driver amplifier capable of saturating the DUT were used. Using the external coupler, the measurement plane is shifted in front of the driver amplifier allowing accurate readings of S_{11} and S_{21} for the amplifier. A power calibration is performed on the VNA at the input plane of the DUT, enabling accurate knowledge of P_{in}, which, when used in conjunction with S_{21}, is used to calculated P_{out}. The output of the amplifier is attenuated heavily to ensure that the receive port of the VNA is protected, which prevented accurate measurement of S_{22} and S_{12}. A more complicated measurement bench could be used for S_{22} and S_{12}, however these parameters were not of interest here [33]. A simplified block diagram of the

setup is shown in Fig. 2.1b The purpose of this measurement setup is to quickly and accurately measure an RFPA transfer function while gathering calibrated gain and phase data for the amplifier. Using the VNA to perform a power sweep and subsequently changing frequency, V_G, and V_D allows for very quick gathering of S-parameter information which, coupled with the power calibration, gives large signal P_{out} performance. To measure efficiency in real time during the power sweep, the VNA is used to trigger multimeters measuring current at the drain of the DUT. For each sweep point the multimeter was triggered storing current data in the instruments memory. At the end of each power sweep, the multimeter's memory is read by the computer. The number of points in the power sweep was set by the memory depth of the multimeter, 201.

With this method a 201 point power, efficiency, and S-parameter measurement is performed in several seconds. The speed of these individual measurements allowed large sweeps of frequency, V_G, and V_D which could then be used to statically analyze the performance of the amplifier over supply modulation operation. The results of these measurement can be seen in Fig. 2.2.

2.2 Developing Shaping Functions

Amplifier performance under static operation does not always reflect performance during dynamic (modulated) operation. This is related to a variety of effects that occur in amplifiers only during under dynamic drive. The effects fall into two categories, memory affects and trapping effects. Memory affects tend to be related to problems the designer has control of such as bias lines, over frequency performance, and over power performance whereas trapping affects are intrinsic to the devices being used [34, 35]. Despite this known variation between static and dynamic performance static measurements are often used to create SFs.

SFs can be designed with the static measurement shown in Fig. 2.2. A flat gain SF aims to maintain a constant gain as a function of P_{out} (and thus also P_{in}) per the gain response in Fig. 2.2a. A maximum PAE SF aims to follow the maximum PAE points at each voltage level as seen in Fig. 2.2c. The SFs are superimposed on top of the static performance curves in Fig. 2.3. The solid lines show the ideal curves for a flat-gain and a maximum PAE. As can be seen the flat gain curve linearizes the gain at the expense of back-off PAE while the max PAE curve tracks the max PAE point at the expense of a linear amplitude response. Both SFs have

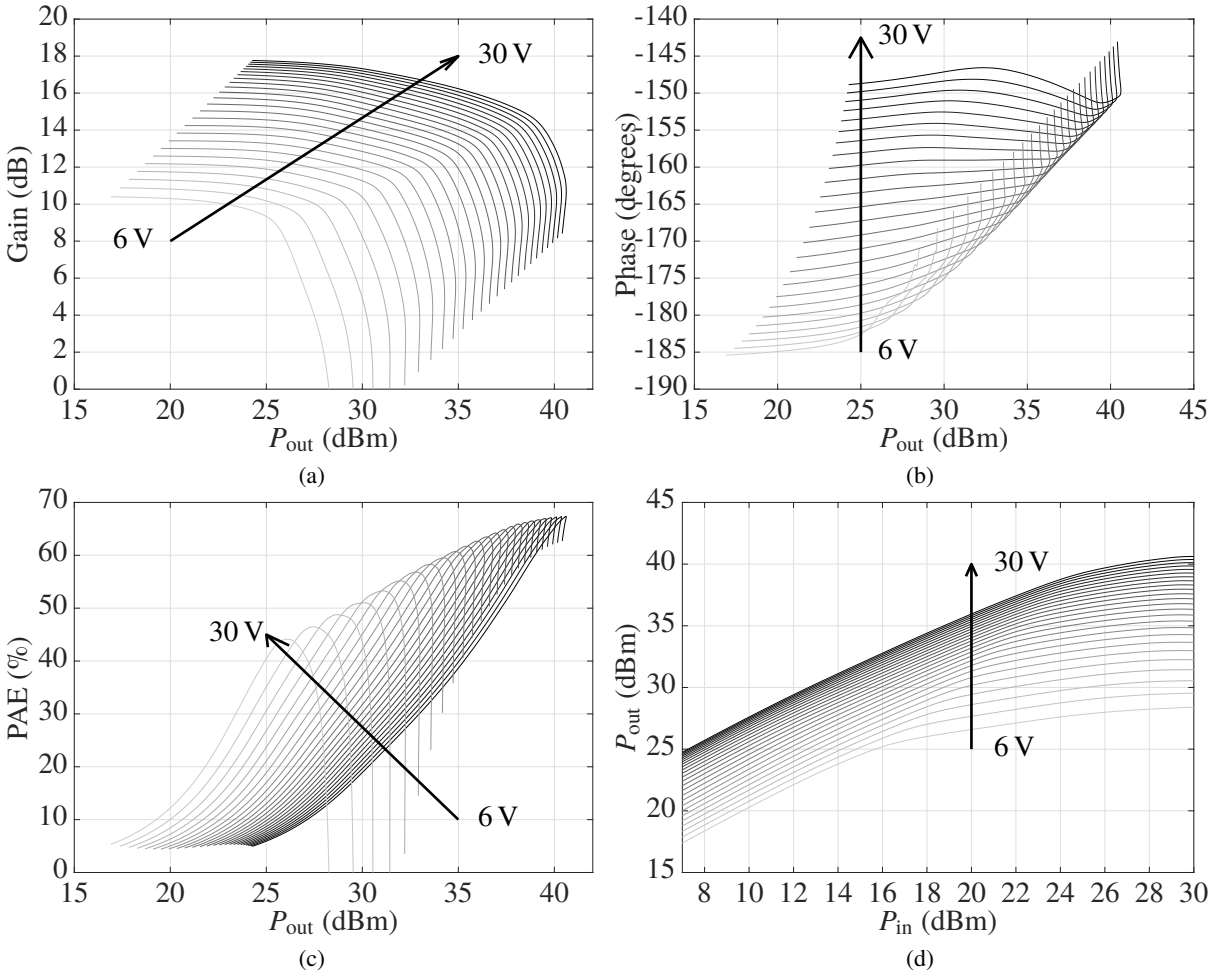


Figure 2.2: Measured (a) gain amplitude, (b) phase and (c) PAE vs. output power, as well as (d) compression curves of the PA from Fig. 2.1a shown in gray lines as a function of drain voltage (6-30 V in 1 V steps).

a negative impact on phase performance.

2.2.1 Performance Modeling

From Fig. 2.3d it can be seen that these curves have a clear $P_{out}(P_{in})$ relationship. This relationship can be used to model the performance of the amplifier with a modulated signal driving it. The model is developed using IQ data for a signal. The voltage of the IQ signal can be scaled so that it represents a certain average input power level for the amplifier. The amplitude information of the signal can then be used to map each point of the modulated signal to a certain gain, phase, and efficiency. From this information average efficiency, gain, power, and linearity can be accessed. This modeling method is used throughout this work

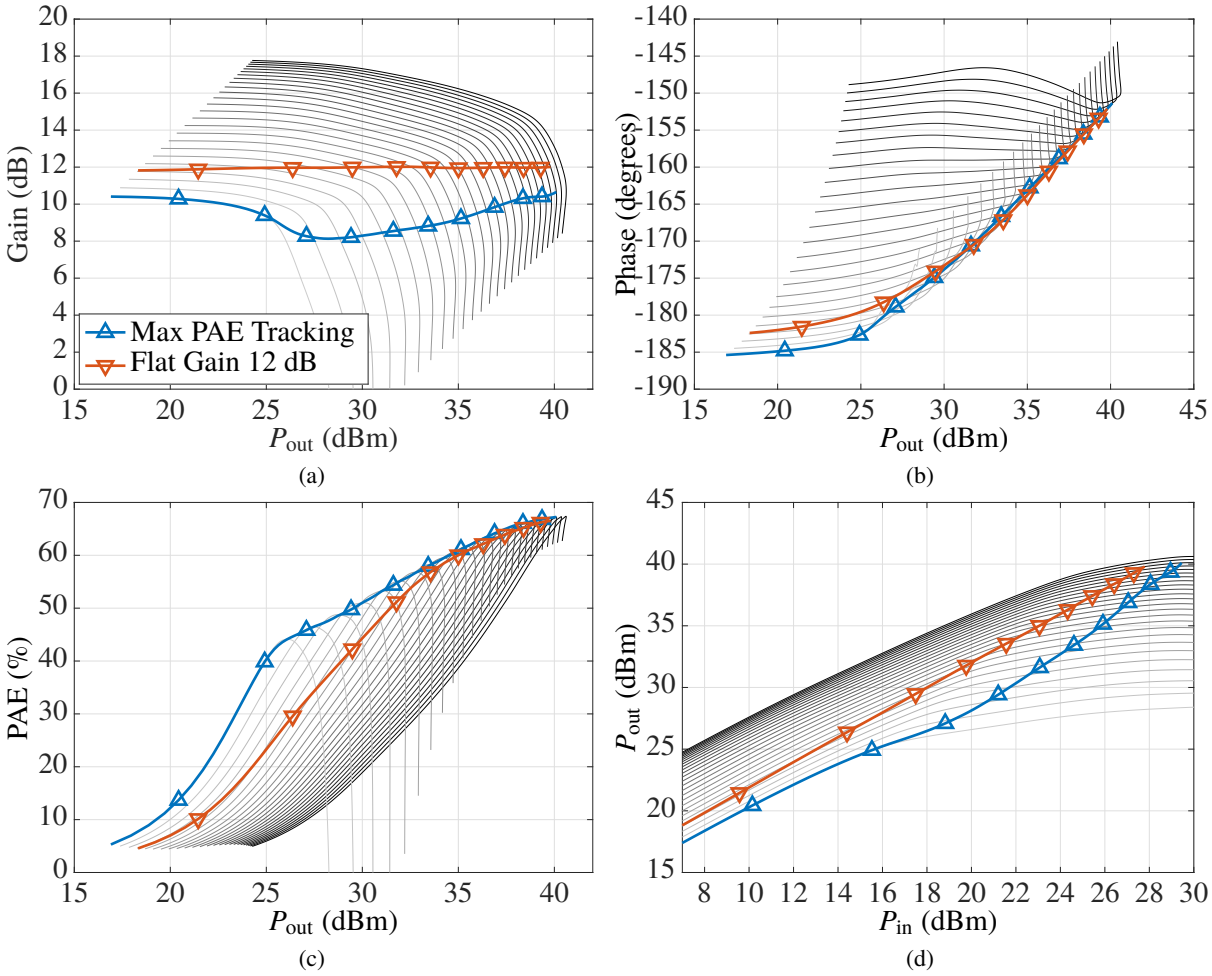


Figure 2.3: Measured (a) gain amplitude, (b) phase and (c) PAE vs. output power, as well as (d) compression curves of the PA from Fig. 2.1a shown in gray lines as a function of drain voltage (6-30 V in 1 V steps).

for analyzing the trajectories used for supply modulation. It is essentially an interpolation of the input voltage signal to the resulting output data. It is linear, does not take into account bandwidth, and (if we are to use it for supply modulation purposes) assumes that the static measurements of the amplifier directly relate to the dynamic performance of the amplifier.

Using the previously described model we can now estimate the performance of each of these shaping functions and see what the difference in performance versus the static supply. The results of these simulations can be seen in Table 2.1. The static supply case has the highest gain and best linearity with the lowest efficiency. The maximum PAE case has the lowest gain and linearity but the highest PAE. The reduction in linearity/gain can be visually observed in Fig. 2.3a where the nonlinear gain response is clear. It is something

Table 2.1: Comparison of Different Continuous Shaping Functions

Trajectory	$\overline{P}_{\text{out}}$(dBm)	Gain(dB)	PAE(%)	EVM(%)
Max PAE	31.6	9	55.2	8.8
Flat Gain = 12dB	33	12	54.2	7.3
Const V_{D}=28V:	32.4	16.3	28.8	4.6

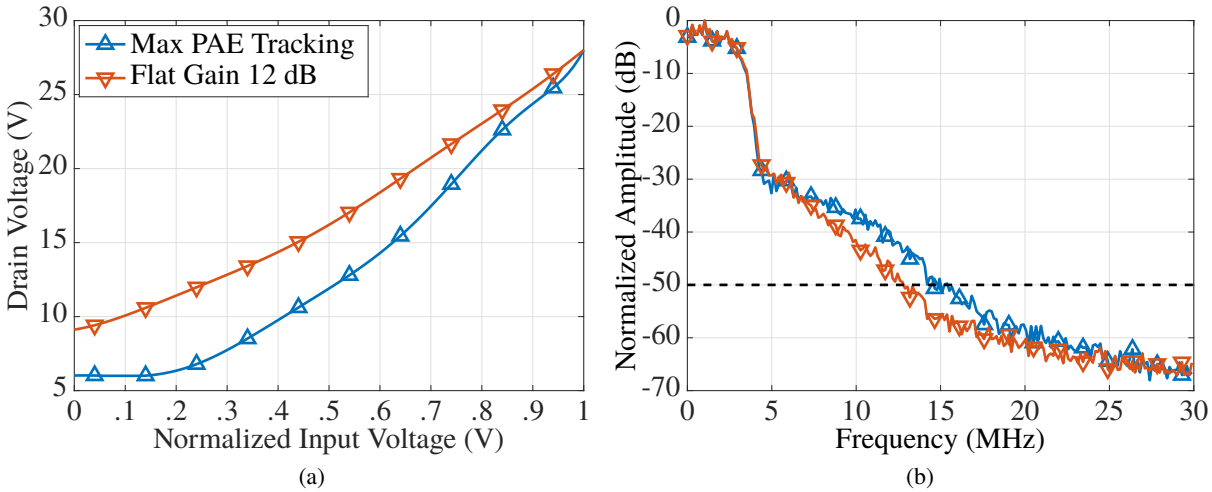


Figure 2.4: (a) Shaping functions for the amplifier shown in Fig. 2.1a. (b) The envelope bandwidth of the two shaping functions applied to a 5 MHz LTE signal.

of a paradox that tracking the peak efficiency points can sometimes reduce the gain to the detriment of the overall efficiency. This is more of a problem for single stage amplifiers than multi-stage amplifiers which tend to have high enough gain even with supply modulation.

2.2.2 Envelope Bandwidth

The differences in the SFs shown can be seen more clearly in Fig. 2.4a. In the example, though we are transmitting a band-limited 5 MHz LTE signal (4.2 MHz signal with a .8 MHz guard band), the envelope bandwidth of the resulting flat gain and max PAE trajectories exceed that bandwidth by several times as seen in Fig. 2.4b. Because the efficiency of a supply modulator is inversely proportional to its switching frequency, envelope bandwidth is critical to system efficiency. Accurately tracking a signal with a switching supply modulator usually requires a switching frequency that is five times the signal bandwidth. In supply modulation applications one normally also tracks the signal down to -50 dBc [36]. For the cases shown

this means the 5 MHz signal, which has an effective envelope bandwidth of 15 MHz, will need a 75 MHz switching frequency supply modulator to be tracked.

Minimizing the baseband bandwidth of the signal shown in Fig. 2.4b has been a topic of research for some time [25–27]. This can also be called "slew rate reduction". If the baseband bandwidth required to supply modulate an amplifier for a given signal can be reduced several benefits can be realized:

- Increases the efficiency of the supply modulator used and thus the system efficiency. For switching supply modulators switching speed and efficiency are inversely proportional.
- Allows more broadband signals to be tracked. In our example above a 15 MHz modulation bandwidth is need for a 5 MHz signal. If the modulation bandwidth can be reduced to the signal bandwidth the same supply modulator can be used for a 15 MHz signal.

Detailed explanations of the baseband bandwidth reduction techniques used in this work for continuous supply modulation will be shown in Chapter 4.

2.2.3 Developing Discrete Shaping Functions

As discussed previously, higher bandwidth signals need faster switching supply modulators which are less efficient. One way to overcome these bandwidth limitations is to use a discrete supply modulator instead of a continuous one [22–24]. The discrete supply modulator toggles between several different discrete voltage levels to approximate a continuous shaping function such as the one shown in Fig. 2.4a reducing the switching speed requirements. Discrete supply modulators, while allowing more broadband supply modulation, do have some drawbacks. Using discrete voltage levels creates discontinuities, which translate to distortions in the performance of the amplifier. This degrades linearity and will make pre-distorting the amplifier more difficult than it would be with a continuous supply. Some benefits of the discrete supply modulator is that it does not require the design of a complicated filter at its output as a buck converter would. This makes it so the impedance presented to the amplifier on the drain can be very low (as low as the impedance of the switch elements) reducing self modulation [37, 38].

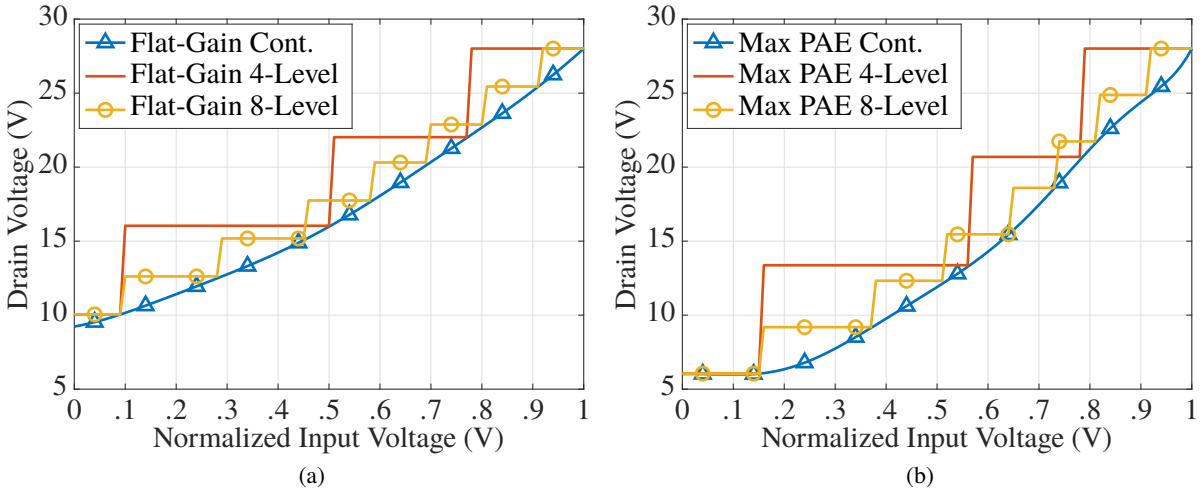


Figure 2.5: (a) Flat-gain and (b) max PAE shaping functions for a the continuous case and two (4- and 8-level) discrete cases.

Creating a shaping function for a discrete supply modulator is done throughout this work by discretization of a continuous shaping function such as the one shown in Fig. 2.5. As an example the max PAE and flat-gain trajectories are discretized here into a 4- and 8-level shaping function. These two cases are examined as these are the discrete supply modulators used throughout this work, a detailed description of their design can be found in [39, 40]. The discretized voltages are always higher than they would be if continuous tracking is used. This is to prevent clipping from having too low of a drain voltage for a given input voltage. The 8-level shaping function does a much better job of approximating the continuous trajectory as the expense of more complexity and more switching events.

To look further at what is happening for these discrete shaping functions we will again examine the performance of the flat-gain shaping functions as we did in Fig. 2.3. These shaping functions are superimposed on to static measurement data, shown in in Fig. 2.6. The discontinuities in the plots correspond to transition points for the discrete voltage levels. It is interesting to note that while the functions are continuous in terms of input power (Fig. 2.6d), they are discontinuous in terms of output power (Fig. 2.6a-2.6c). These gaps mean that for a given discrete shaping function there are certain output powers (within the range of normal amplifier operation) that will not occur. It can be visually seen in these plots that discretization of the envelope can reduce gain flatness and increase phase variation. The 8-level shaping function is clearly

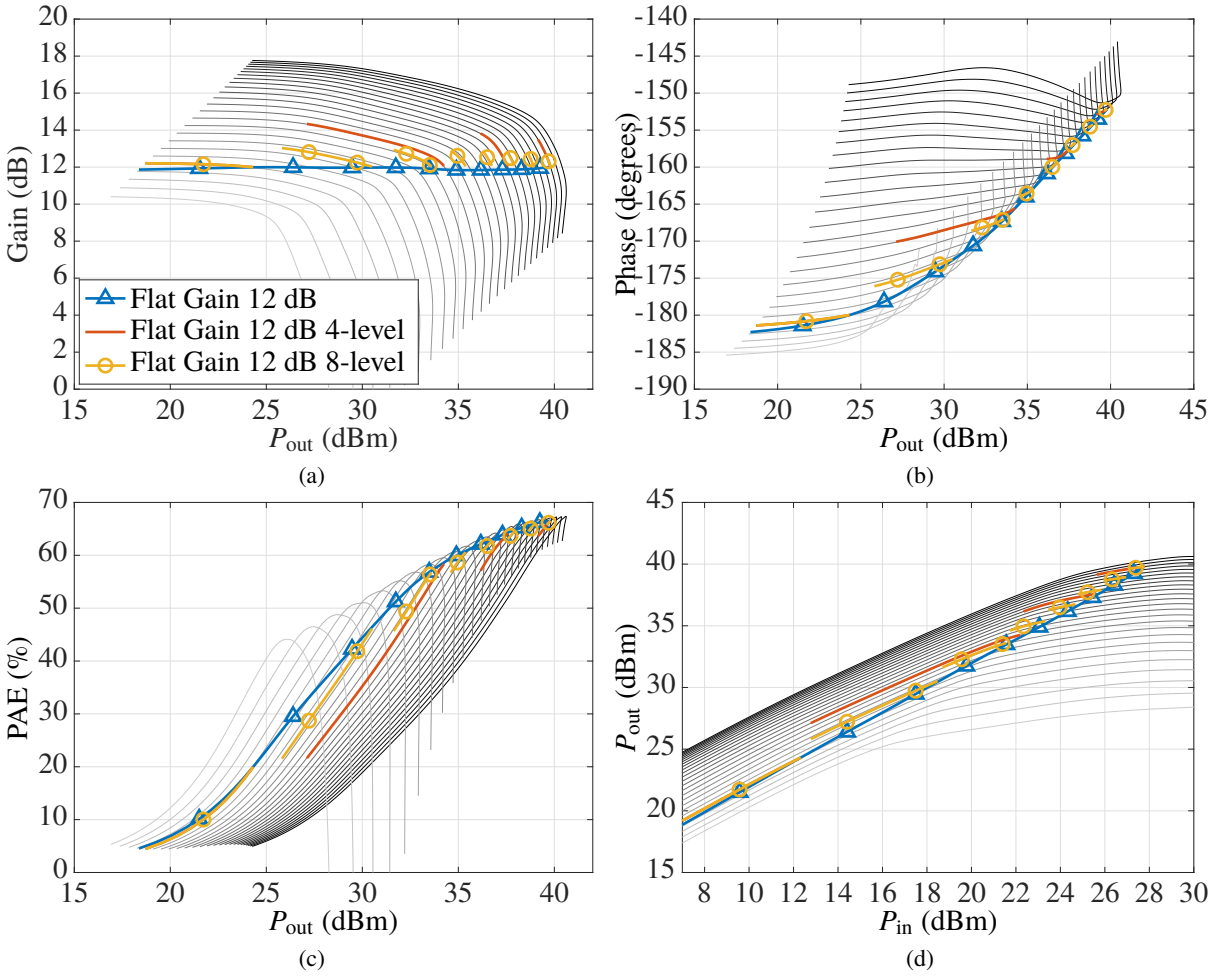


Figure 2.6: Measured (a) gain amplitude, (b) phase and (c) PAE vs. output power, as well as (d) compression curves of the PA from Fig. 2.1a shown in gray lines as a function of drain voltage (6-30 V in 1 V steps).

better tracks the gain and phase of the continuous case than the 4-level shaping function.

The performance of the continuous shaping functions shown earlier as well as the discretized versions of the shaping functions is shown in Table 2.2. When comparing the different rows note that there is a variation in output power. The cases are analyzed assuming that the of the input signal occurs at a normalized input voltage of one as seen in Fig 2.5. This sets the input power which then determines all other parameters. In simulation the discretized cases tend to have higher gain than the continuous cases as the voltage is higher than the continuous case at all points but the switching points. This same effect can cause an improvement in the linearity of the amplifier over the continuous supply case as is seen for the Max PAE SF.

Discrete supply modulation can provide comparable linearity and efficiency performance to continuous

Table 2.2: Comparison of Different Discrete Shaping Functions

Trajectory	$\overline{P}_{\text{out}}$(dBm)	Gain(dB)	PAE(%)	EVM(%)
MaxPAE	31.6	9	55.2	8.8
MaxPAE Discr. 4	33.6	11	57.7	12.8
MaxPAE Discr. 8	32.5	9.8	56.8	7.8
Flat Gain = 12dB	32.9	11.9	54.1	7.2
Flat Gain = 12dB Discr. 4	34	13	53.3	8.7
Flat Gain = 12dB Discr. 8	33.5	12.5	54	8
Const V_{D}=28V:	32.4	16.3	28.8	4.6

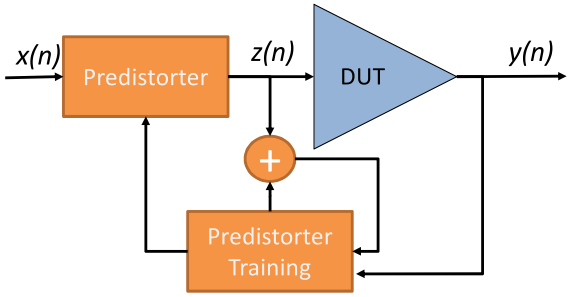


Figure 2.7: Block diagram of indirect learning algorithm predistorter.

supply modulation. Though in this simple study supply modulation is shown to under-perform compared to a static supply in terms of linearity in all cases that should also not be taken as self-evident. Supply modulation shaping functions, such as flat-gain or other linearity focused (which account for phase) shaping functions, can improve linearity to the level of or better than a static supply. If linearity needs to be improved further other digital options exist for linearization such as DPD.

2.3 Linearity Enhancement

2.3.1 Digital Pre-Disortion

DPD offers an additional method for linearizing an amplifier. Throughout this work indirect learning DPD algorithms, a block diagram of which is shown in Fig. 2.7, based on the memory polynomial are used [41].

For an indirect learning algorithm a reverse model of the amplifier is first developed. To do this a measurement is performed on the amplifier. The amplifier output, y, is compared to the input signal, x, to

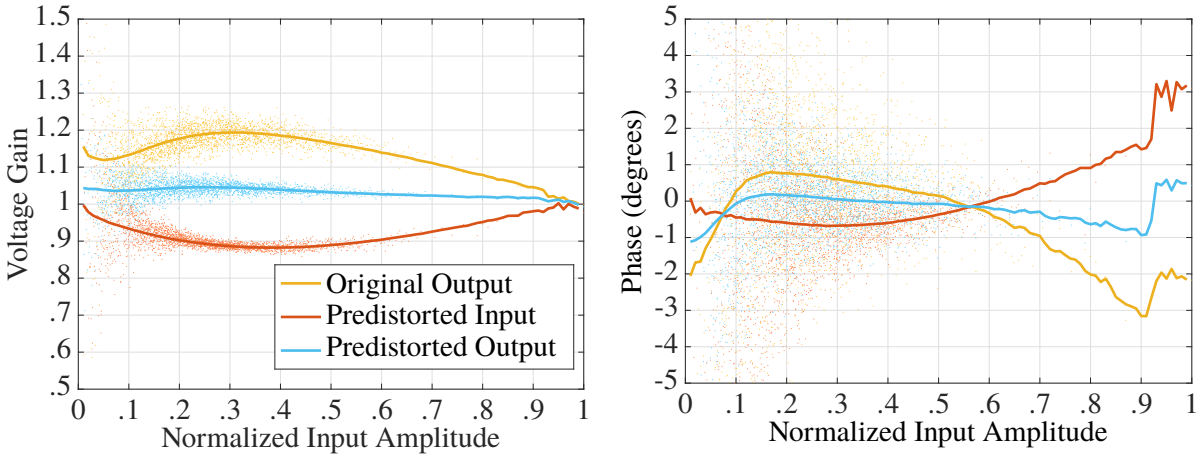


Figure 2.8: Measured (a) AM/AM and (b) AM/PM for a signal transmitted through an amplifier with and without DPD. Individual data points are shown as faded dots with a darker trendline superimposed.

generate the predistorted input, z. This is done by determining the coefficients, a, such that z has the inverse nonlinearity of y. The memory polynomial is defined by:

$$z(n) = \sum_{k=1}^{K} \sum_{q=0}^{Q} a_{kq} x(n-q)|x(n-q)|^{k-1} \tag{2.1}$$

where a_{kq} are the coefficients of the memory polynomial with k denoting the polynomial order and q denoting the memory depth. During the predistorters learning step (when $x = z$) matrix inversion is used to find the coefficients such that $z = a \cdot \mathbf{M}_y$ where $\mathbf{M}_y$ is the summation from (2.1) in terms of y:

$$\mathbf{M}_y = \sum_{k=1}^{K} \sum_{q=0}^{Q} y(n-q)|y(n-q)|^{k-1} \tag{2.2}$$

Taking this matrix and solving for a gives the coefficients describing the inverse nonlinearity of the amplifier. Once these coefficients are found they can be used in (2.1) to generate the predistorted input signal, z. When this is transmitted through the amplifier the nonlinearity of the predistorter should cancel out the nonlinearity of the amplifier, seen in Fig. 2.8.

2.3.1a Shortcomings of Digital Pre-Disortion

Though DPD is an effective linearization method it has some shortcomings. The predistorted signal experiences bandwidth expansion proportional to the polynomial order; so if a 10 MHz signal is being transmitted with a 5th order memory polynomial the predistorted signal will be 50 MHz, which can put a strain on the signal generation hardware. DPD can also be computationally intensive particularly as the number of coefficients increases.

Additionally it should be noted that a predistorter only has as much information as it is given. As slew rate reduction techniques are utilized that break the V_{in} to V_{D} relationship, as seen in Fig.2.4a, traditional predistorters will not work [36, 42–45]. This is because slew rate reduction techniques will often make it so each V_{in} does not have a unique V_{D} and as such there can be a large performance variation for the same V_{in}, introducing a kind of drain voltage dependent memory. If this is the case the predistorter needs this information to function properly, increasing predistorter complexity.

Pre-disortion is also only usable when there is access to the signal as baseband. Some applications, such as amplify-and-forward repeaters, receive and transmit a signal in the RF domain without moving into the digital domain. In these cases an analog predistortion method is needed. One such method used in this work is gate modulation.

2.3.2 Gate Modulation

Gate modulation offers the potential to improve the linearity of an amplifier while simultaneously giving some improvement in efficiency [46–50] . The amplifier from Fig. 2.1a was tested with a static drain supply with varying gate supply voltages (and thus quiescent currents). It can be seen from Fig. 2.9 that through gate modulation 5 dB of gain reduction can be produced as well as 15 ° of phase lag. This is shown for a static bias, however it can be coupled with drain modulation for even more variation. This offers a powerful tool to the person trying to linearize the amplifier. By correctly selecting the gate and drain voltage of the amplifier a flatter gain and phase response can be realized than the pure drain modulation case [51–54].

The result of modeling simultaneous gate and drain modulation can be seen in Table 2.3. Linearity and

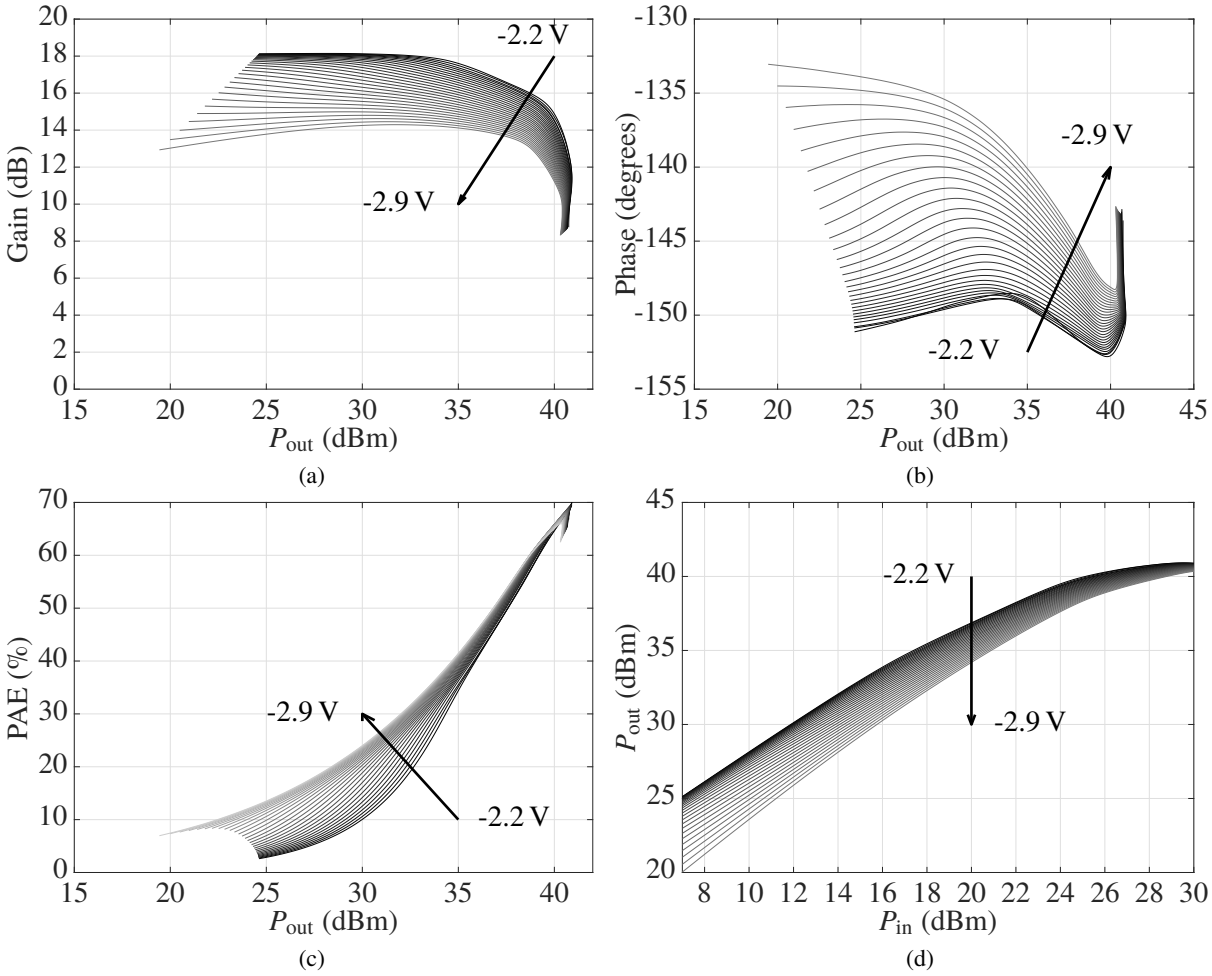
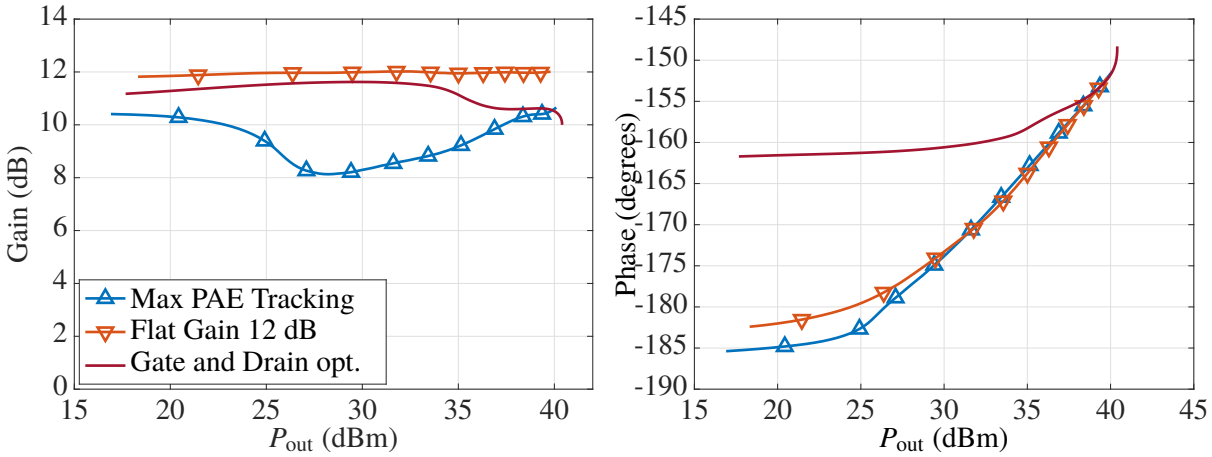


Figure 2.9: Measured (a) gain amplitude, (b) phase and (c) PAE vs. output power, as well as (d) compression curves of the PA from Fig. 2.1a shown in gray lines as a function of gate voltage (-2.2-2.9 V in .025 V steps).

Table 2.3: Comparison of Different Shaping Functions with Gate Modulation

Trajectory	$\overline{P}_{out}$(dBm)	Gain(dB)	PAE(%)	EVM(%)
MaxPAE	31.6	9	55.2	8.8
Flat Gain = 12dB	32.9	11.9	54.1	7.2
Gate and Drain opt.	34.6	10.9	56.8	4.1
Const V_D=28V:	32.4	16.3	28.8	4.6

efficiency both improve over all other cases. Linearity improves over the static supply case (by .5pp) better than any pure drain modulation case. It should be noted that gate modulation can offer benefit up to a point. As seen in Fig. 2.9, when the amplifier is compressed beyond P_{out} =40 dBm the variations produced by gate



(a) (b)

Figure 2.10: Measured (a) gain amplitude, (b) phase of the PA from Fig. 2.1a comparing drain modulation with gate and drain modulation.

modulation are greatly reduced. Gain and phase comparing static gate and gate modulated results for supply modulation are shown in Fig. 2.10. Gate modulation improves phase performance (from a 35 deg variation to a 15 deg variation) while maintaining a relatively (± .75 dB) flat gain. It can be seen that the majority of improvements in phase performance occurs for lower power levels (P_{out} <30 dBm)

2.4 Summary

In this section an overview of supply modulation is provided. Using an amplifier that was statically characterized with a VNA conclusions are made about the dynamic performance and a shaping function (trajectory) developed. Two methods of supply modulation are discussed and simulated, continuous and discrete. It is seen that supply modulation will increase efficiency, often at the expense of linearity. Several methods to mitigate non-linearities are discussed, namely digital pre-distortion and gate modulation, which can be made fully analog. The methods discussed in this section are used throughout this work.

The details presented in this chapter are contained in publication [30].

Chapter 3

Hardware Overview

Contents

Test hardware and measurement methods are described here including, amplifiers and supply modulators, as well as well as test benches used to characterize them. Three amplifiers are discussed, two in depth while a third, specifically designed as a part of this thesis, is presented but explained thoroughly in Chapter 6. Linear trackers (including gate and drain trackers), and MMIC-based discrete supply modulators are next described. Measurement benches, calibration and alignment methods required to test SM-PA are presented followed by an overview of the test signals used.

3.1 Amplifier Overview

Three amplifiers were used throughout this work. The first is a hybrid implementation from 2-4 GHz [55]. This amplifier is used for testing related to next-generation cellular communication, such as carrier

aggregation for 5G. The second amplifier is a two-stage MMIC implementation in GaN at X-band [56]. The third amplifier is three-stage MMIC implementation in GaN at K-band [57]. Testing with these amplifier was performed examining signals for satellite communication systems. The amplifiers have several commonalities:

- the amplifiers are made to be stable with small (>30 pf) bypass capacitors. This is done so the bias line will not short the low frequency envelope.
- the amplifiers are designed to have a peak efficiency point at a lower than maximum voltage level. This is done so the peak efficiency point will be higher during the average voltage level used in back-off.
- the amplifiers need to be over-designed in terms of bandwidth. Changing the drain voltage of the amplifier will shift the optimum impedance points which must be accounted for in the design, this can usually be done by designing for a larger than needed bandwidth. The consequence of this is a degradation of in-band performance.

3.1.1 Octave Bandwidth 10 W GaN PA

The broadband amplifier [55] design is based on simulated load-pull for maximum efficiency over 2-4 GHz taking into account up to the third harmonic. The sensitivity to the impedance at the fundamental frequency is examined to inform required matching for flat efficiency across the band. Fig. 3.1a illustrates the procedure that determines the region where the drain efficiency is greater than 65 %. The range from 3.5-4 GHz is, as expected, most affected by impedance variations. A trade-off in the fundamental frequency match sacrifices efficiency in the lower frequency range (2-3 GHz) which reaches over 80 % in load-pull. The matching circuits are designed with a focus on maximizing efficiency and gain in upper part of the band (3-4 GHz), resulting in a flat efficiency and gain response.

To achieve broadband matching, short transmission line sections that approximate lumped elements over the band are implemented, similar to the stepped-impedance networks in [58, 59]. The final topology is generated by constraining the number of transmission line sections to three at the output, and two at the input, with a goal of simplicity and reduced footprint. The range of microstrip line impedances is constrained

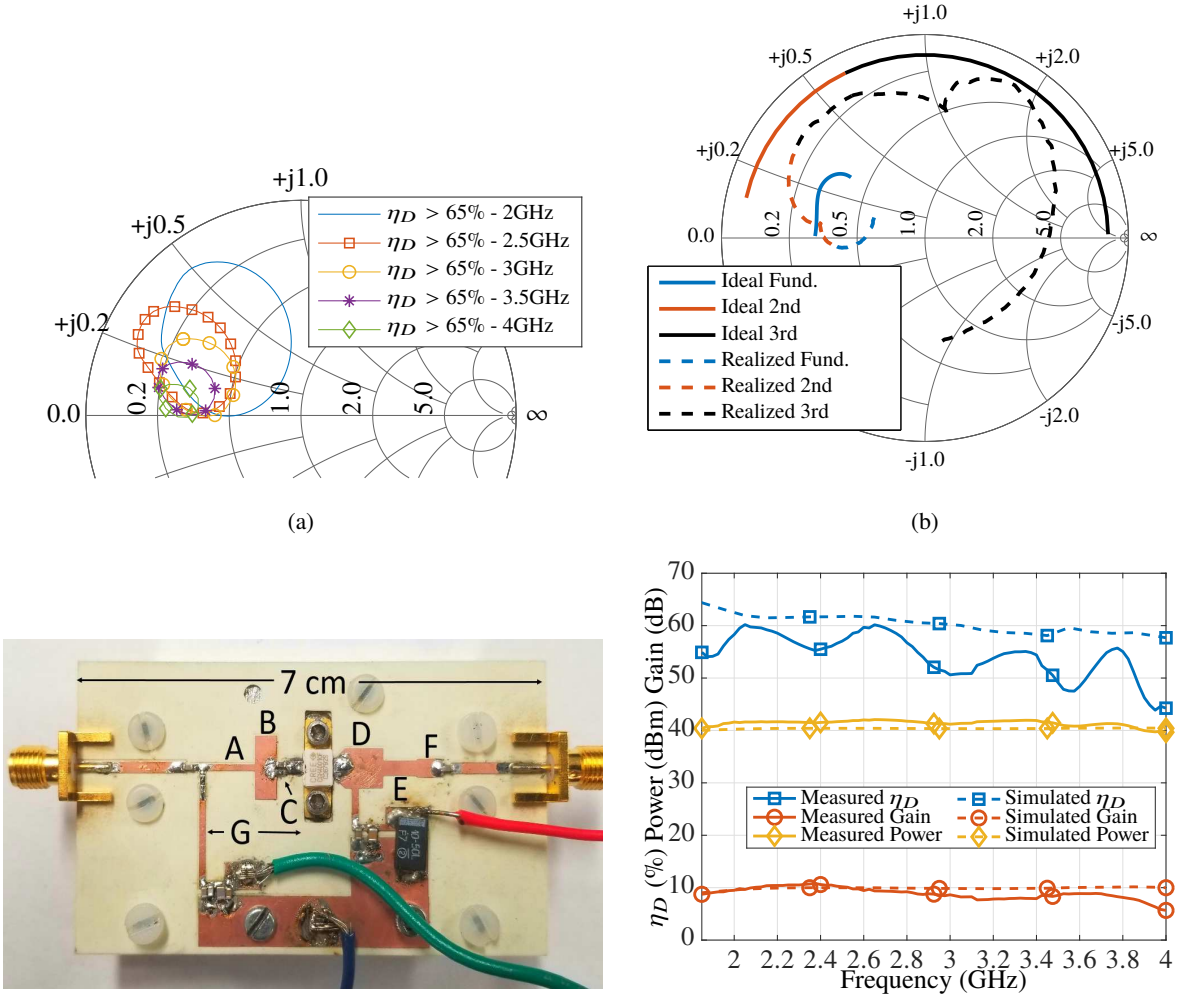


Figure 3.1: (a) Maximum drain efficiency contours of the fundamental (2-4 GHz). With increased frequency the efficiency contours shrink. (b) Output impedance targets of the fundamental (2-4 GHz), second (4-8 GHz), and third harmonic (6-12 GHz) from simulated load pull (solid). Realized impedances of output matching network (dashed). Because the second harmonic has a higher impact on efficiency than the third, it takes precedence where the two overlap. (c) Fabricated 2-4 GHz power amplifier with stepped impedance line segments of A-66 Ω, B-15 Ω, C-gate stability network, D-21 Ω, E-41 Ω, F-36 Ω, G-1.5 cm. The substrate is a 0.762 mm Rogers 4835. (d) Amplifier large signal performance at saturation over frequency. Shown are both measured (solid) and simulated (dashed) results.

between 15 and 70 Ω. The ideal terminations found from load-pull and the realized output matching network impedances are shown in Fig. 3.1b. A parallel R-C network is added in series at the gate terminal in the input match to ensure stability, with values resulting from stability analysis. The fabricated amplifier is shown in Fig. 3.1c, and the CW measured results are summarized in Fig. 3.1d.

3.1.2 X-Band 10 W MMIC GaN PA

The PA is a two-stage MMIC [56] implemented in a then experimental version of the Qorvo 150 nm GaN-on-SiC HEMT technology. The first driver stage of the PA is composed of two 8×50 μm devices, while four 10×90 μm devices are combined in the second stage, with a saturated gain greater than 20 dB at 2-3 dB gain compression. The maximum drain supply voltage is V_D = 20 V, for a total class-AB quiescent drain current I_D = 310 mA; During measurements both stages are supply-modulated.

No off-chip capacitance is added to the drain pad to enable fast supply modulation. The only bypass capacitance to this node is provided by the on-chip integrated MIM (Metal-Insulator-Metal) capacitors, for a total value of 30 pF (2x15 pf capacitors in parallel). The PA is soldered on a CuMo carrier and the input/output RF pads are wire-bonded to 50-Ω microstrip lines on alumina. The PA frequency sweep shows a bandwidth from about 9 to 10.5 GHz, with peak efficiency at 9.7 GHz. The PA measured dependence on supply voltage and frequency is summarized in Fig. 3.2b-3.2a. A picture of the amplifier can be seen in Fig 3.2c.

3.1.3 K-Band 4 W MMIC GaN PA

The K-Band amplifier [57] is implemented in the Qorvo 150-nm GaN on SiC process. The process uses 100 μm substrate and slot vias, and the transistors make use of internal source vias. For the output stage 8×100 μm transistors with a 15/52 pitch are chosen; pairs of 15 µm spaced gates with internal source vias within the 52 µm spacing between pairs. The bias point is selected to match the point of model validation, V_D=20 V with 100 mA/mm.

To meet the design target output power of 4 W, two transistors are combined in the output stage. With the specification requiring 30 dB of small-signal gain, a three stage design is selected. The chosen staging

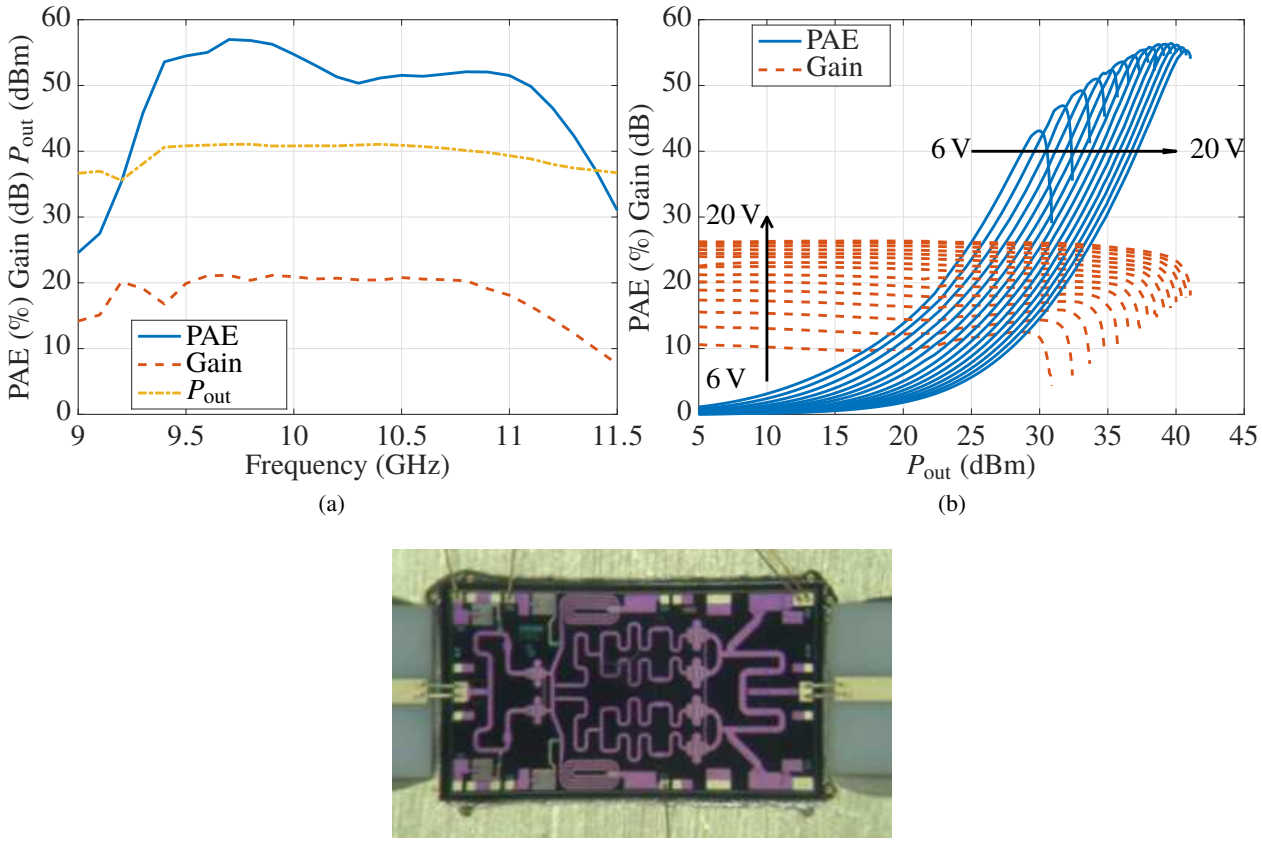


Figure 3.2: Measured performance of X-band amplifier over (a) frequency and (b) voltage at 9.8 GHz. (c) Fabricated and packaged amplifier.

ratio for the transistors is 1:2:8. This ensures that the current draw of the two driver stages has a minimum impact on the total efficiency of the amplifier. The first and second driver stages use 4×50 μm and 8×50 μm transistors. The amplifier has over 20 dB of saturated gain, over 4 W peak output power, and peak efficiencies ranging from 40-45 % from 18.5 to 24 GHz. A photo of the MMIC is shown in Fig.3.3 and a more detailed explanation of the amplifier design and characterization can be found in Chapter 6.

3.2 Supply modulators

This work makes use of four different supply modulator circuits. Two of these circuits are linear tracker implementations, one a gate and the other a drain tracker. The linear trackers are based on op-amps and are inefficient but easy to use in a test bench. Two of the supply modulator circuits are MMIC implementations.

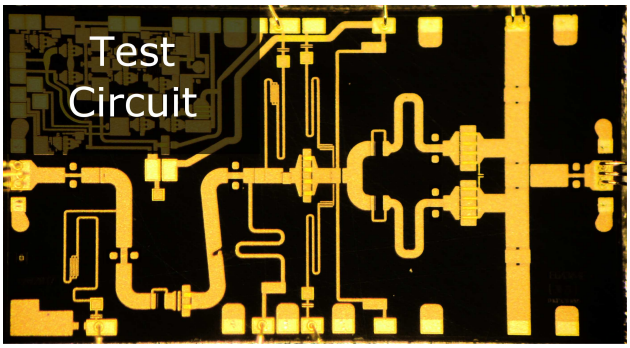


Figure 3.3: Photograph of the 3-stage K-band MMIC, 4 mm × 2 mm in size, fabricated in the Qorvo 150-nm GaN-on-SiC process. The top left part of the die is a test circuit which is not a part of the PA. The output stage devices are 8×100 μm with a nominal drain voltage of 20 V at 100 mA/mm. Three bondwires connect the amplifier RF bond pads to the alumina input and output lines. A single bondwire is used for all DC bias lines excluding the final stage where DC current draw is the highest.

These circuits are built in a version of the Qorvo GaN-on-SiC 150 nm process. GaN is used because of its attractive switching performance, low output capacitance, and on resistance [20,39,60–64]. Both MMICs are discrete supply modulators (4- and 8-level) have on chip gate drivers but the differ slightly in implementation.

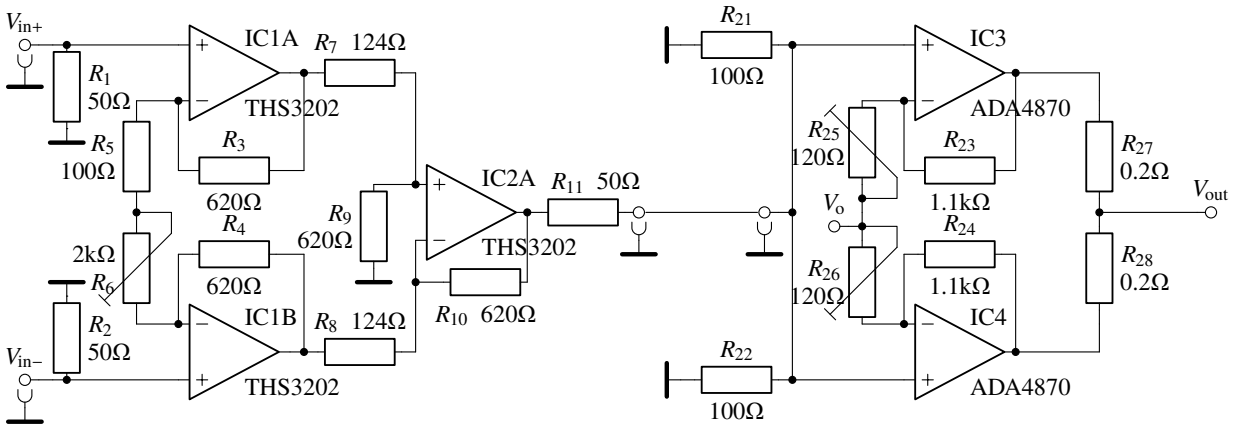
3.2.1 Linear Trackers

3.2.1a Drain Trackers

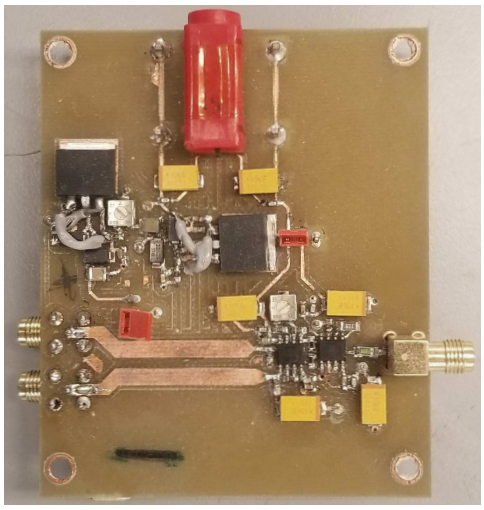
The drain tracker is based on two sub circuits, a gain stage and a power stage. The power stage makes use of the Analog Devices ADA4870 Current Feedback operational amplifier, chosen for its high current drive (1 A), slew rate (2500 V/ µs), and bandwidth (>50 MHz). For a peak output current of 2 A, two op amps are connected in parallel. A schematic of the tracker is on the right side of Fig. 3.4a and pictures in Fig. 3.4c. The maximum bandwidth capabilities of the tracker can be determined as a function of slew rate, SR, and maximum voltage swing V_{pp}:

$$f = \frac{SR}{2 \cdot \pi \cdot V_{pp}} \tag{3.1}$$

The slew rate specifications suggests that the circuit is capable of distortion-free tracking of signals with bandwidths up to 18 MHz for an output voltage swing of 6-28 V (22 V_{pp}), up to 28 MHZ for 6-20 V (14 V_{pp})),



(a)



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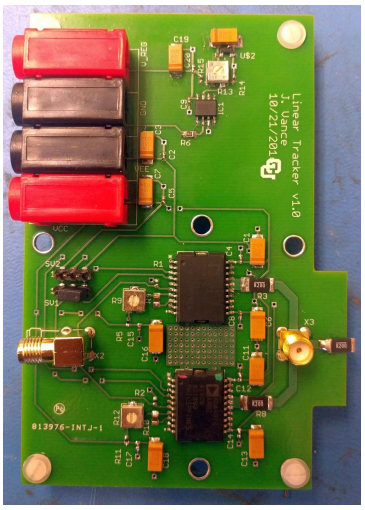


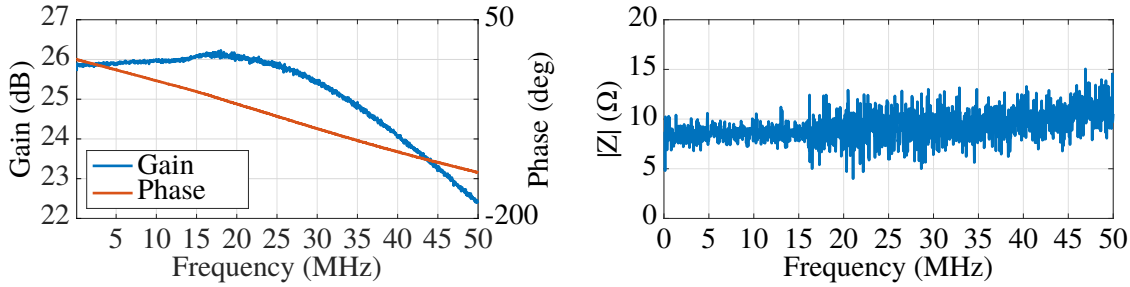
(c)

Figure 3.4: (a) Simplified circuit diagram of the linear tracker. The left side shows the differential-to-single-ended converter, the right side contains the power op-amps which create the drain voltage. The interconnect enables either single-ended or differential operation of the supply modulator. (b) Fabricated differential-to-single-ended converter. (c) Fabricated linear tracker power stage.

and up to 40 MHZ for 10-20 V (10 V_{pp})).

Two 200 mΩ series resistors, R_{27} and R_{28}, are added to each amplifier output to compensate for slight gain mismatches between IC3 and IC4, and help stabilize the op-amps from capacitive loading under various biasing conditions of the RFPA. The performance of the circuit as measured with a VNA is seen in Fig. 3.5a.

This initial circuit has some drawbacks, namely low gain and a high output impedance on the order of 10 Ω, seen in Fig 3.5b. For voltage swings greater than 14 V an additional gain stage is needed so the



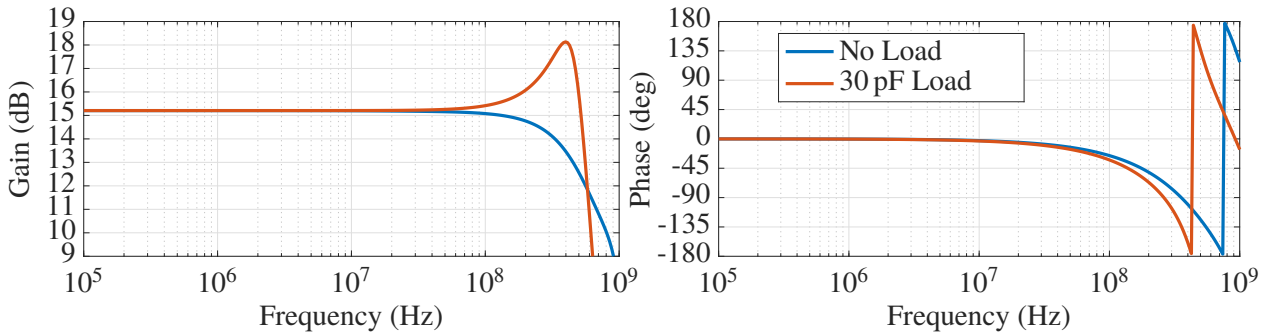
(a) (b)

Figure 3.5: Measured performance of the linear tracker power stage showing (a) gain and phase. Measurements are taken with a VNA and thus the Circuit is terminated in 50 Ω which does not reflect the real implementation where the circuit will be capacitively loaded. (b) Measured output impedance of the linear tracker. The measurement was done through an attenuator and noise can be observed in the data.

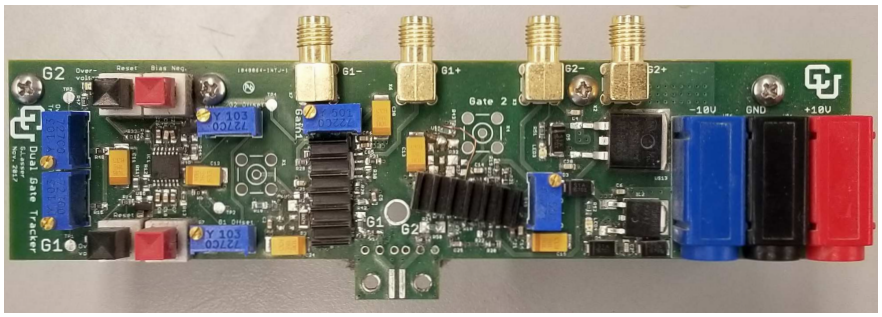
drive-signal can generate the maximum voltage swing from the power stage. This is done with a differential to single ended stage based on three THS3202 op-amps configured as an instrumentation amplifier, drawn on the left side of Fig. 3.4a. This allows for a reduced gain setting of the power stages (IC3 and IC4), resulting in a lower output impedance of the tracker, favorable for envelope tracking. A picture of the driver circuits is seen in Fig. 3.4b. No equalization is done on the linear tracker itself, since it is confirmed by measurement with a 10 MHz LTE signal that the error between the tracker and control signal is below the noise floor.

3.2.1b Gate Trackers

The gate bias circuit is designed using a similar topology to the gain stage pictured in Fig 3.4b and discussed in Section 3.2.1a. The gate bias circuit is designed to integrate with a two-stage amplifier and has two outputs. Two instrumentation amplifiers are designed with THS3202 current feedback op-amps, converting a differential drive signal to a single ended output. The differential input signals are independently terminated in 50 Ω resistors, amplified by the first stage THS3202 pair, and then level shifted with an adjustable negative offset voltage. A 5 Ω series stability resistor is connected at the board output. The resistor also reduces the Q factor of the resonant circuit formed by the bondwire and on-chip bypass capacitor (approximately 30 pF for X-Band amplifier discussed in Section 3.1.2). The simulated frequency response of the gate tracker is shown in Fig. 3.6a-3.6b. To ensure a flat frequency response within the tracking bandwidth, the tracking signal is digitally equalized, as described in Section 3.3.3c. A picture of the board can be seen in Fig. 3.6c.



(a) (b)



(c)

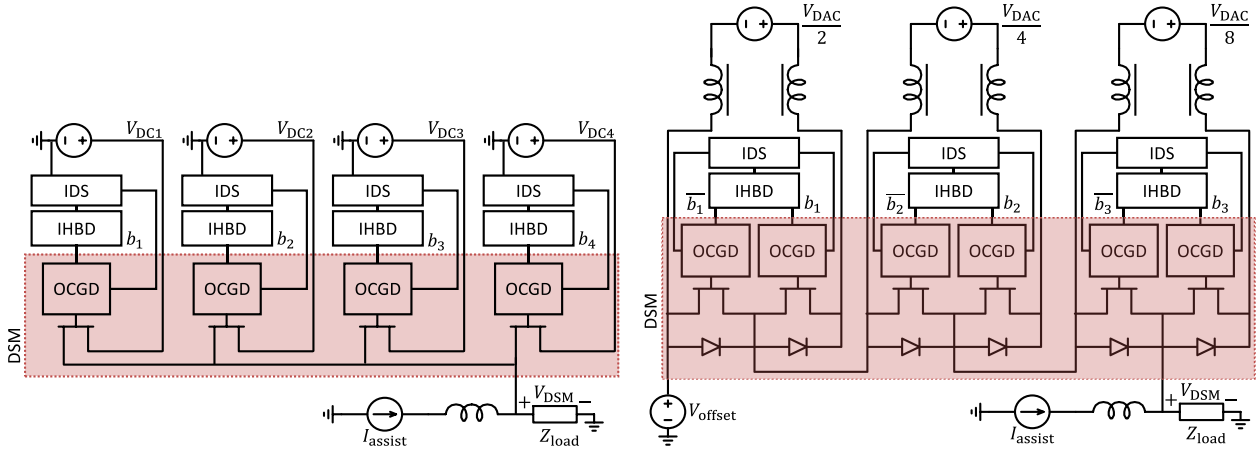
Figure 3.6: Performance over frequency of the dynamic gate supply circuit showing (a) gain and (b) phase without a load and with a 30 pF load. 30 pF is the size of the on-chip gate bypass capacitors for the amplifier this board is used with. (c) Fabricated gate tracker board.

3.2.2 MMIC Supply Modulators

The two MMIC implementations used in this work are 4- and 8-level discrete supply modulators. Both are packaged in 44-pin QFN packages. A parent board, the Multi-Level Driver (MLD), is made to provide common supply voltages and drive signals to one of the child boards which route the supply and control signals to the respective pins of the QFN packages. The parent board as well as the individual DSM circuits will be discussed here.

3.2.2a Multi-Level Driver

The multi-level driver (MLD) accepts DC voltages from external supplies and provides the necessary connections to a child board. The MLD is modular, working with two different child boards and biasing their respective DSMs as needed. For the 8-level DSM the board layout is arranged to minimize the parasitic



(a) (b)

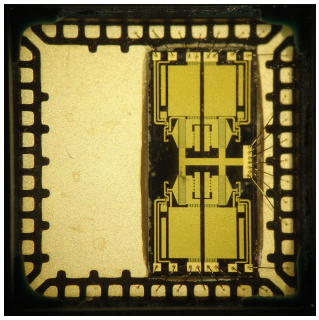
Figure 3.7: Simplified multi-level driver (MLD) with discrete supply modulator. V_{DAC} and V_{DC} supply voltages are provided externally. The board includes isolated half bridge drivers (IHBD) and isolated driver supplies (IDS). The DSMs have on chip gate drivers (OCGD) that are driven and powered by the board. Two configurations of the drive board are shown for the (a) 4- and (b) 8-level supply modulator. The 8-level topology requires an added V_{offset} and makes use of an external current-assist circuit (I_{assist}) that is routed through a choke to source current directly to the load.

capacitance from each of cell to ground, which reduces efficiency and linearity through ringing effects at each commutation.

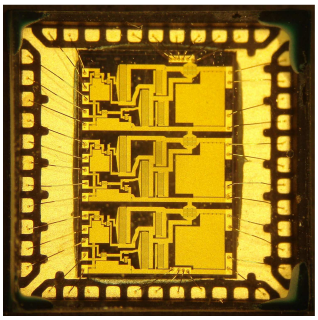
The block diagram in Fig. 3.7a shows the MLD connections for the 4-level DSM. The DSM requires four externally generated supplies ($V_{DC}n$ n={1,2,3,4}), drive signals, and auxiliary supply voltages for the on-chip gate drivers (OCGD). The MLD is split into 4 cells each feeding an individual switch.

The block diagram in Fig. 3.7b shows the MLD connections for the 8-level DSM. The DSM requires three floating supplies ($\frac{V_{DAC}}{2}$, $\frac{V_{DAC}}{4}$, $\frac{V_{DAC}}{8}$), floating drive signals, and auxiliary floating supply voltages for the OCGD. The main circuitry of the MLD is split in three cells, each feeding a half bridge with the required supply voltages based on a common potential. The switching supply voltages $\frac{V_{DAC}}{2^n}$, supplied externally, are routed to the DSM chip through common mode chokes, as shown at the top of Fig. 3.7b. These chokes isolate the half bridges from the stray capacitances of the power supplies. An offset voltage, V_{offset} which sets the lowest voltage level for the 8-level DSM is also provided externally.

For both cases the auxiliary voltages that supply the circuitry of each cell and provide the isolated driver



(a)



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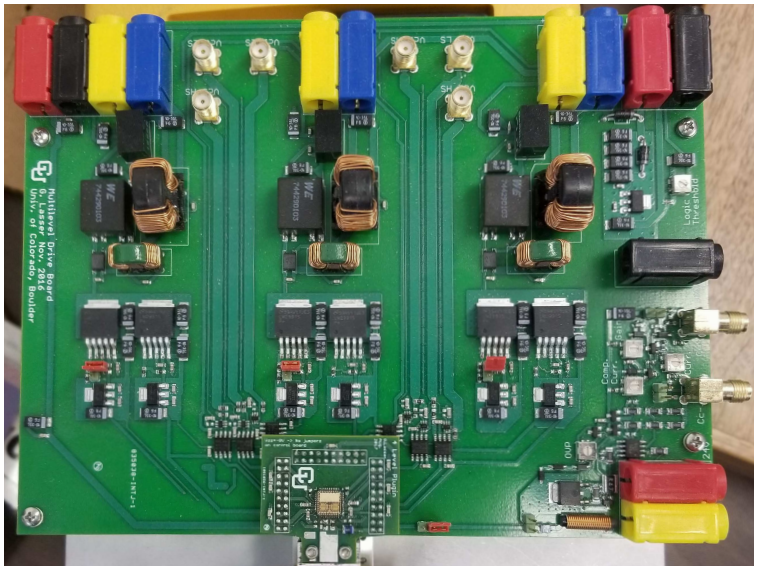


(c)

Figure 3.8: Picture of GaN integrated (a) 4- and (b) 8-level discrete supply modulators packaged in 44-pin QFN. (c) MLD with 4-level DSM child board.

supply (IDS) for the on-chip drivers are routed through common mode chokes. The digital drive signals are routed to isolated half bridge drivers (IHBD) which contain comparators for level-shifting. This is followed by separate isolator chips (ISO721M) to provide the independently shifted drive signals for the on-chip gate drivers (OCGD). The MLD contains an injection point for a current assist, I_{assist}, where the injected current is isolated from the time varying supply voltage by a series of inductors (68 nH on the carrier board, 68 nH and a 6 μH choke on the MLD). A picture of the MLD with the 4-level child board is seen in Fig. 3.8c.

3.2.2B 4-Level DSM

The discrete supply modulator (DSM) is designed in the Qorvo 150-nm Gan-on-SiC process. This process makes use of circular vias. The circuit consists of 4 hard switching transistors, which each have an R_{on} of approximately .5 Ω, connected to a single output node. Referring to Fig. 3.7a, the output voltage, V_{DSM}, is determined by:

$$V_{\text{DSM}} = \sum_{n=1}^{4} b_n V_{\text{DCn}} \tag{3.2}$$

where V_{DC} sets the step size, the b_n's are control signals $\in \{0, 1\}$ and only one switch can be active at a time.

The switches toggle between discrete voltages that are supplied externally from the MMIC. A snubber circuit is integrated on MMIC to reduce ringing associated with switching transitions. On-chip gate-drivers are also integrated in GaN to minimize the effects of parasitics on switching. Due to the lack of complementary devices in GaN the gate-driver circuit uses both active and modified active pull-up drivers, designed to minimize quiescent current draw from the driver transistors. Throughout this work composite efficiency will be quoted two ways, one incorporating gate driver losses and one without. A photo of the supply modulation circuit can be see in Fig.3.8a. A detailed discussion of the design and characterization of the DSM can be found in [39]. Measurements of the DSM into a 30 Ω load are be seen in Fig. 3.9a where it can be seen that gate-driver losses reduce efficiency by over 10pp.

3.2.2C 8-Level DSM

For the DSM GaN MMIC used in this work, three stacked half bridges are used to generate 8 discrete supply voltages [40]. Referring to Fig. 3.7b, the output voltage, V_{DSM}, is determined by:

$$V_{\text{DSM}} = \sum_{n=1}^{3} b_n \frac{V_{\text{DAC}}}{2^n} + V_{\text{offset}} \tag{3.3}$$

where V_{DAC} sets the step size, the b_n's are control signals $\in \{0, 1\}$ and V_{offset} shifts the lowest voltage level from zero.

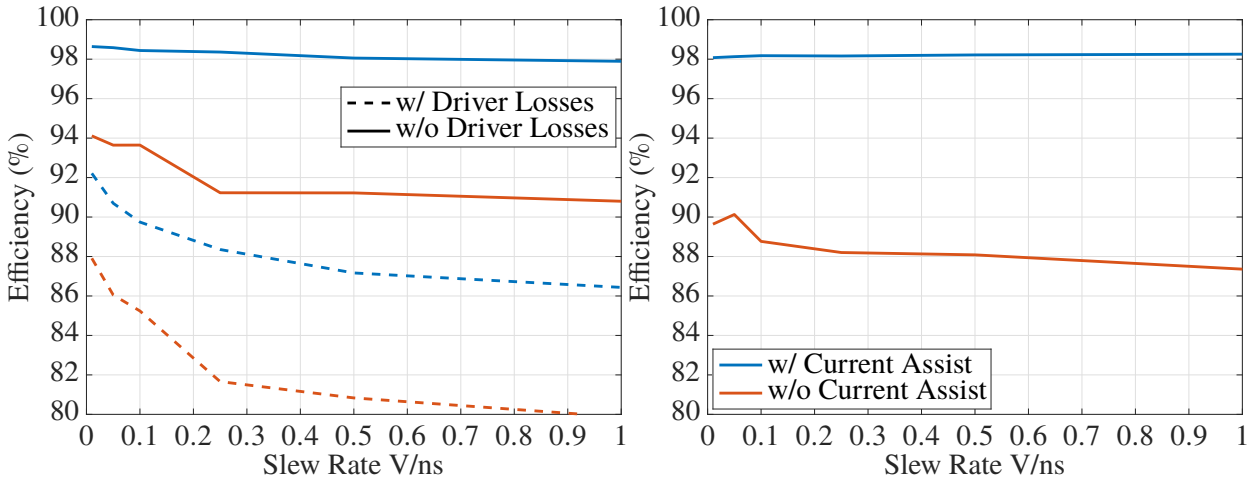


Figure 3.9: Efficiency of (a) 4- and (b) 8-level discrete supply modulator for a 100 MHz noise-like signal into a 30 Ω load. Efficiencies are shown as a function of the assumed slew rate the trajectories are made with. A higher slew rate corresponds to more switching incidents and thus lower efficiency. The shaping functions are made for the amplifier described in Section 3.1.2 at P_{in}=15 dBm. A current assist is used in both cases to improve circuit efficiency. The design of the 4-level tracker makes it so driver losses are included in raw measurements. Driver losses are here estimated and subtracted out so a fair comparison can be made to the 8-level tracker.

For the same number of levels this method requires fewer supplies than other DSM topologies [39, 65] (Section 3.2.2b). The number of supply voltages needed to produce the required drain voltage levels scales linearly, while the number of discrete drain voltage levels scales exponentially. This benefit comes with the drawback of having the conducting half-bridge switches in series at all times and the requirement of isolated drivers and supplies. To compensate for the increased conduction losses in this circuit, the sizes of the switches are increased (9.6 mm versus 3.9 mm for the design in Section 3.2.2b) when compared to similar integrated supply modulator designs done in the same 150 nm GaN process [39, 61]. This reduces the R_{on} of each switch to .33 Ω, making the total R_{on} for the 3 half bridges in series 1 Ω. While this does mitigate some of the added conduction loss in the circuit it simultaneously increases the switching loss and reduces the maximum switching frequency. Measurements of the DSM into a 30 Ω load can be seen in Fig. 3.9b. Efficiencies are not quoted with driver losses due to the difficulty in independently isolated the driver current on this board. With that said the drivers are less efficient than those of the DSM discussed in Section 3.2.2b. A photo of the supply modulation circuit can be see in Fig.3.8b.

A method for compensating the higher conduction losses in this circuit, which might motivate different design choices in a second iteration, is discussed next.

3.2.2D Current-Assist

A current-assist (CA) circuit is used in conjunction with the 4- and 8-level DSM to reduce the amount of current flowing through the DSM switches, minimizing the voltage drop across the switches and the conduction losses in the circuit. The CA uses the Analog Devices LTM8042 switching converter in a DC1511A development board. The converter uses feedback to regulate a constant current at the output and is connected in parallel with the output of the DSM through a choke. Operating the DSM as a static supply for the X-Band PA described in Section 3.1.2 the CA sources the average offset current, I_{assist} (pictured in Fig. 3.7b), that would otherwise flow through the DSM chip, lowering the voltage drop across the internal resistance in the DSM, shown in Fig. 3.10a-3.10b for a 20 V static supply. This voltage drop, which varies from 1-3 V in our area of operation, leads to a reduction in gain and degrades linearity.

During supply modulation the CA becomes the dominant factor in the efficiency of the supply modulation circuit. The effect on the current draw for different supply voltage levels is seen in Fig. 3.10c for the 8-level DSM. The CA sources all of the offset current that would otherwise flow through the supply modulator reducing conduction losses. The circuit can be extremely efficient because sourcing the constant baseline current does not require a fast modulator. The off-the-shelf solution shows 87-90 % efficiency, however a more efficient custom solution, e.g. a slow-switching buck converter that maintains a constant output current, can be designed with conventional components. For initial measurements, before the DC1511A implementation of the current assist, a voltage source and a resistor are used as a current assist.

The CA circuit works more consistently with the 8-level than the 4-level DSM due to the V_{offset}. For all drive power levels the V_{offset} average current (which is usually the dominant current draw) will be sourced by the CA as seen in Fig. 3.10c. For the 4-level DSM current flows through switches only when they are on. As the drain voltage statistics change for different drive levels the 4-level does not always benefit as clearly from the CA circuit, particularly the case when certain voltage levels are being under or un-utilized. In these cases the CA will only provide the current for these low current levels, reducing its effectiveness.

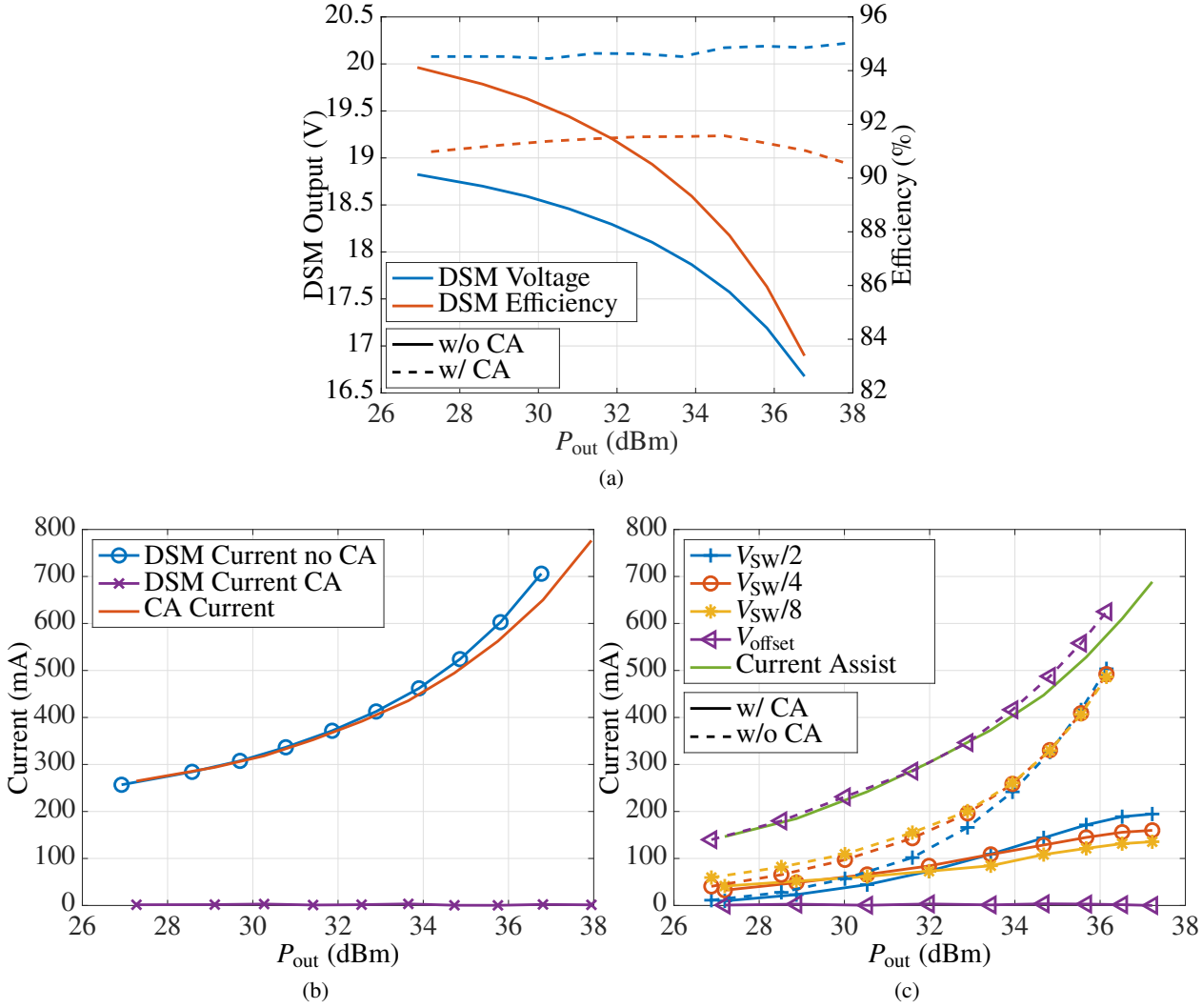


Figure 3.10: X-Band PA described in Section 3.1.2 used with 8-level DSM. Swept measurements of a 10 MHz noise-like signal using the DSM as a static 20 V supply in conjunction with the CA. (a) Output voltage and efficiency of DSM with and without the current assist. (b) Current draw from the DSM with and without the CA. Swept measurements of a 10 MHz noise-like signal using the DSM as a dynamic supply in conjunction with the CA. (c) Current sourced by different supplies with and without CA circuit for the PA under drain supply modulation. Note that the offset current is fully sourced by the CA.

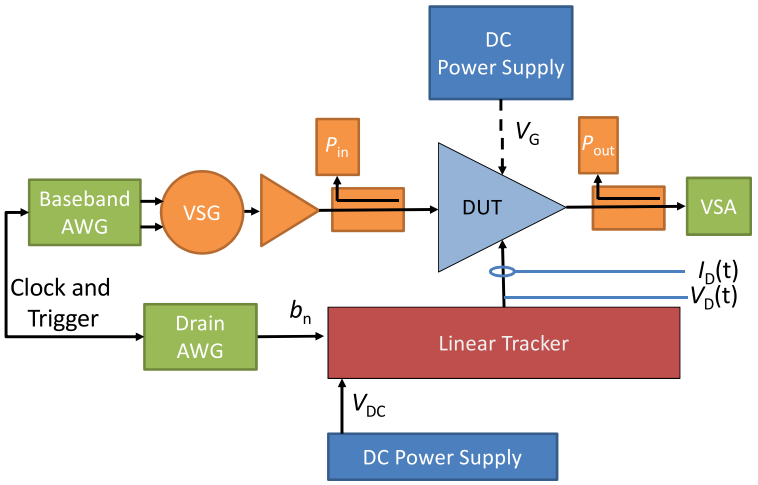
3.3 Measurement Setups

Throughout this work several measurement benches are used, all based on the same equipment with slight variations. The general test benches, Fig. 3.11, are discussed along with their calibration. Modulated signals, described in Section3.3.4, are generated by a N8241A arbitrary waveform generator (AWG), which drives a E8267D vector signal generator (VSG), and is amplified by a driver. The DUT is driven by the RF signal. A second AWG is used to provide a control signal for the linear tracker circuits, whether this is a gate or drain tracker. For discrete supply modulators the control signals are provided by a bit-pattern generator (BPG). For all of these measurements time alignment between the different signal sources is critical. To the first order this is ensured by clock synchronization of the AWG and BPG. Separate time alignment for both gate and drain signals is also necessary along with an equalization that can be applied to compensate for the frequency response of the circuit or interconnects, discussed in Section 3.3.3.

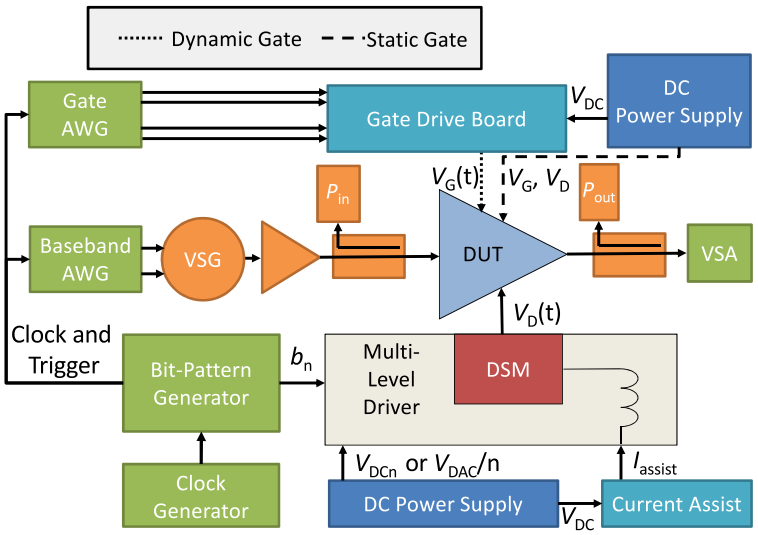
The AWGs have a maximum sampling rate of 1.25 Gs/s enabling signal generation up to a 500 MHz I and Q bandwidth and can be aligned with 800 ps resolution. The VSA has a maximum signal receiver bandwidth (for IQ data) is limited by a maximum 140 MHz IF bandwidth and a sampling rate of 170 MHz. Received data is time and phase aligned in post processing because the VSG and VSA are not phase aligned.

3.3.1 Linear Tracker Test Bench Efficiency Measurement

Accurate measurements of envelope voltage and current are required when characterizing a supply-modulated transmitter, in order to determine the non RF input power, P_{dc}, and therefore the efficiency of the device. To consider efficiency without the linear tracker P_{dc} measurements need to be taken between the tracker and the DUT. Envelope measurements are performed using a 5 Gs/s oscilloscope. The oscilloscope is set to match the sampling rate of the AWG's (1.25 Gs/s) allowing easy time alignment. A N2876A low capacitance RF probe is used for voltage measurements ($V_{\mathrm{D}}(t)$), while a N2819A high frequency differential probe is used for ac current measurements, $I_{\mathrm{D}}(t)$. The measurement is done to get the low frequency ac power and the dc power. Combining these together gives a P_{dc} that accurately reflects the output of the linear tracker.



(a)



(b)

Figure 3.11: Block diagram of test setup for (a) a linear tracker implementation and (b) a DSM implementation. The block diagrams are meant to be general and ignore the number of biases that might be present on an amplifier i.e. multiple static V_Gs. The linear tracker implementation requires current and voltage measurements at the interconnect between the tracker and the DUT. This allows measurement of P_{dc} for efficiency calculation. The DSM implementation does not require this measurement as the trackers are efficient and thus are considered in the system efficiency calculation.

3.3.1A Calibration of ac Current Measurements

Current measurements are taken across the R_s=0.2 Ω resistor at the output of the linear tracker, Fig. 3.12. A calibration needs to be performed for the probe interconnect and the frequency dependence of the differential

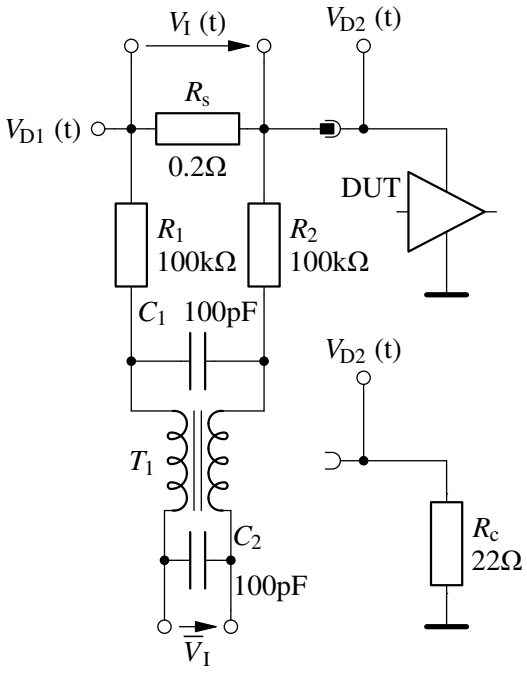
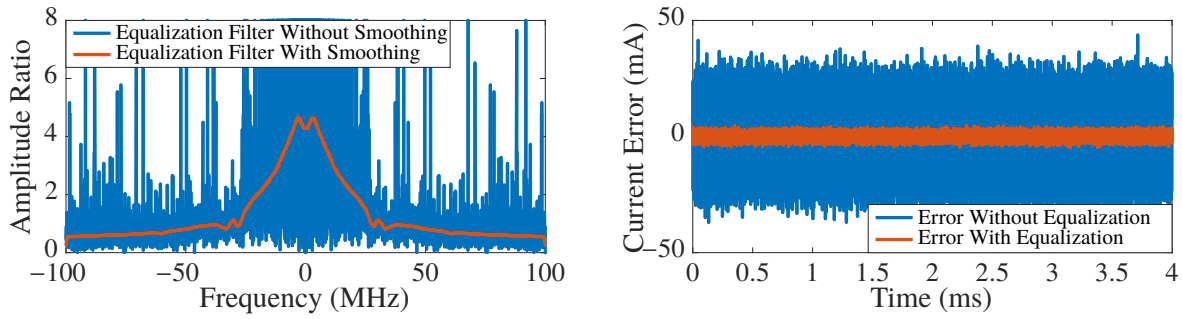


Figure 3.12: Drain current calibration and measurement. The left part of the circuit is the current sense circuitry that can be connected either to the amplifier board (top right) or the calibration board (bottom right).

probe. A "calibration board" is created with the same interconnects and shape as the amplifier board, but loaded with a R_c=22 Ω 1206 SMD resistor in place of the bias line shunt capacitor, and with the DUT removed, shown in Fig. 3.12. Measurements are then performed with a linear tracker transmitting a 100 MHz noise-like signal. With the voltage measured across the load and the value of the resistor known, the current through the load is determined.

These two signals, the ideal current and the differential voltage V_I, can then be converted into the frequency domain and divided to create an equalization function that converts the measured differential voltage to the actual current. Due to the small value of the sense resistor R_s, the resulting equalization function is noisy and a moving average smoothing function is applied to the frequency response, shown in Fig. 3.13a. The equalization function is shown with and without smoothing in the frequency domain. The smoothed version is converted into the time domain, truncated and convolved with the raw differential voltage measurements to give the corrected current. The effect of this filter function can be seen in Fig. 3.13b in the time domain current measurements.



(a) (b)

Figure 3.13: (a) Equalization filter response generated to correct the parasitics in the current measurement setup. (b) Effect of the equalization on the 4 ms noise-like signal used for calibration.

3.3.1B Calibration of dc Current Measurements

For validation of the differential probe for dc current measurements, we used a voltmeter to probe the dc component of the input current and apply this as an offset to the oscilloscope reading. This is done because we noticed that the differential probe zero reading is susceptible to variation with probe movement and thermal drift. An RC network is placed around the sense resistor which is also being used by the differential probe, Fig. 3.12. The values of $R_{1,2}$ and C_1 are set such that the time constant of the network is much greater than the signal length. A common mode choke T_1 further suppresses any interference from the envelope signal, followed by an additional capacitor C_2. This voltage V_1 is probed by a high impedance (1 GΩ) voltage meter which measures the voltage drop across resistor R_s. Loading the circuit with the "calibration board" and calculating the current through the resistor determines a factor which converts the measured voltage drop $\overline{V}_I$ to the dc component of the current.

3.3.2 DSM Test Bench Efficiency Measurement

The bench relies on a BPG which creates the clock and trigger signals for the two AWGs. All three instruments are thus capable of being temporally aligned allowing consistency between measurements. One AWG is used to generated the RF signal while another is used to generate up to two V_G control signals. The BPG creates controls signals for the DSM which generates the V_D. The MLD contains an injection point for a current assist circuit through a choke. An in depth discussion of the hardware used to power the DSM and

drivers is given in Section 3.2.2.

This configuration does not share the same complications related to efficiency measurements that the linear tracker bench does. Because the DSMs designed to be a part of a transmitter system, efficiency can be calculated from the average power $\frac{V_{\mathrm{DAC}}}{n}$ or V_{DCn}. This is as simple as a multimeter measurement for the dc from the voltage supplies. For the 8-level DSM this measurement will give the power that is directly delivered to the DUT load. For the 4-level DSM a raw measurement of the current into the DSM includes the quiescent current draw of the gate driver circuits. The losses of the gate driver circuits can be estimated analytically [39, see Section III] or measured by operating the DSM without a load. Good agreement was seen between the measured and analytically derived gate driver loss so the analytical model is used to estimate losses.

3.3.3 Bench Alignment and Calibration

Several levels of calibration and equalization are performed, and described below in the following order: RF amplitude calibration, time alignment, and AWG equilization.

3.3.3a Amplitude calibration

The RF signal path is calibrated with a CW signal by replacing the DUT in Fig. 3.11 by the P_{out} power sensor. The input and output directional couplers are then directly connected with the P_{out} power sensor at its normal location. By comparing the power levels in these two cases, the amplitude offsets for the power meters are found.

3.3.3b Time Alignment

Time alignment ensures that the RF input signal and the bias signals align at the RF PA [66, 67]. In envelope tracking, it is often done by optimizing linearity or efficiency, e.g. [68–70] and Chapter 4, as a function of path delay. This is a somewhat cumbersome technique and takes time to converge if a good starting point is not selected. Additionally, with multiple gate and drain signals there are different path delays, so alignment of several signals is required. Instead, we observe the effect of a perturbation on the drain or gate voltage as

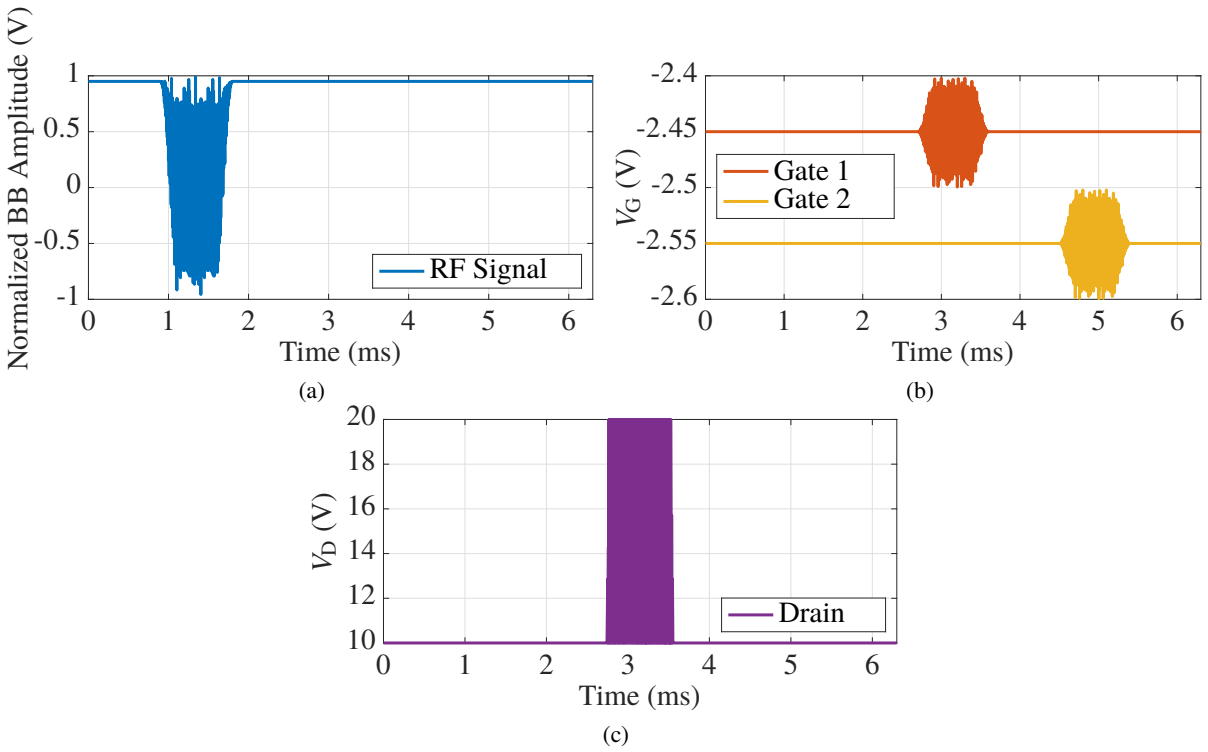


Figure 3.14: Signals used for time alignment: (a) transmitted baseband signals, (b) transmitted gate signals, and (c) transmitted drain signals. Time alignment is done in two steps, first for the gate and then for the drain.

an amplitude modulation in the PA RF output signal, and compare its temporal occurrence with a reference signal on the RF carrier. The signal bandwidths are chosen to fit within the 140 MHz bandwidth of the VSA. Therefore the gate signal amplitude modulation bandwidths may not exceed 70 MHz, since they will appear with twice the bandwidth at the RF signal. The temporally shifted pseudo-random test noise signals are shown in Fig. 3.14.

The 6.3 ms long RF signal consists of an unmodulated carrier, augmented with a 900 µ*s* long noise signal created by applying a Tukey window [71, see (6.9)] with parameter $p = 0.5$ to a concatenated signal consisting of three copies of a 300 µ*s* noise signal. The windowing creates smooth amplitude tapers at the beginning and end of the signal, reducing the bandwidth. The repetition allows cutting out a 300 µ*s* portion of the composite signal in postprocessing, resulting in a circularly shifted version of the original signal. This is beneficial for time alignment and frequency domain processing, explained below. To obtain smooth transitions between the CW and noise signal parts of the test signal, Fig. 3.14a from 0.9 ms to 1.8 ms, the CW signal is windowed by 1 minus the Tukey window, and the two signals are added.

For gate alignment the signals shown in, Fig. 3.14b consist of identical copies of a 65 MHz-wide noise signal, created in the same way as the RF signal, and unmodulated DC voltages chosen to create standard biasing conditions of the PA. The modulation on the gate signals is separated by 900 μs, and both signals are shifted by the same amount from the RF modulation pulse. The gate modulation amplitude is kept small to maintain approximately linear bias dependence of the PA transconductance, creating an amplitude modulation of the unmodulated carrier sections of the RF output signals. The received signals are time- and phase-aligned to the RF modulation pulse using crosscorrelation in post-processing. The time delay introduced by the different paths is found by crosscorrelating the received in-phase signal with the corresponding gate signal, so that the two paths are synchronized up to a single clock cycle of the ARBs (800 ps).

For drain alignment, the signal shown in Fig. 3.14c is generated from the same signal modulated onto the gates. A 15 dBm input power is assumed for the amplifier discussed in Section 3.1.2 and with the amplifier shaping function a control signal developed. The time delay is found using cross-correlation and alignment up to 800 ps is realized.

3.3.3c Voltage Mapping and Equalization

The last calibration step addresses the gate drive amplitude, enabling direct mapping between the ARB settings and the gate/drain voltages applied to the PA. The ARBs are consecutively loaded with static signals, the first one corresponding to the maximum, the second one to the minimum ARB output. The corresponding gate voltages are measured and used to compute the offset and slope of the linear relation between the ARB setting and the gate/drain voltage.

For the gate the gain and phase response of the gate drive boards are well behaved up to 10 MHz, Fig. 3.6a-3.6b, however the theoretical bandwidth of the gate tracking signal, as derived from the RF signal envelope, is infinite. Additionally, the interconnect between the gate drive PCB and the MMIC PA affects the frequency response of the tracking signal. To mitigate this, we apply a zero forcing equalizer [72, p.220] to the gate signal prior to loading it to the ARB. The equalizer is found from the same measurement used for time alignment. The original 300 μs long center piece of the noise signal is cut out of the in-phase received signal, and processed in the frequency domain. Since the signal was transmitted repeatedly, applying the

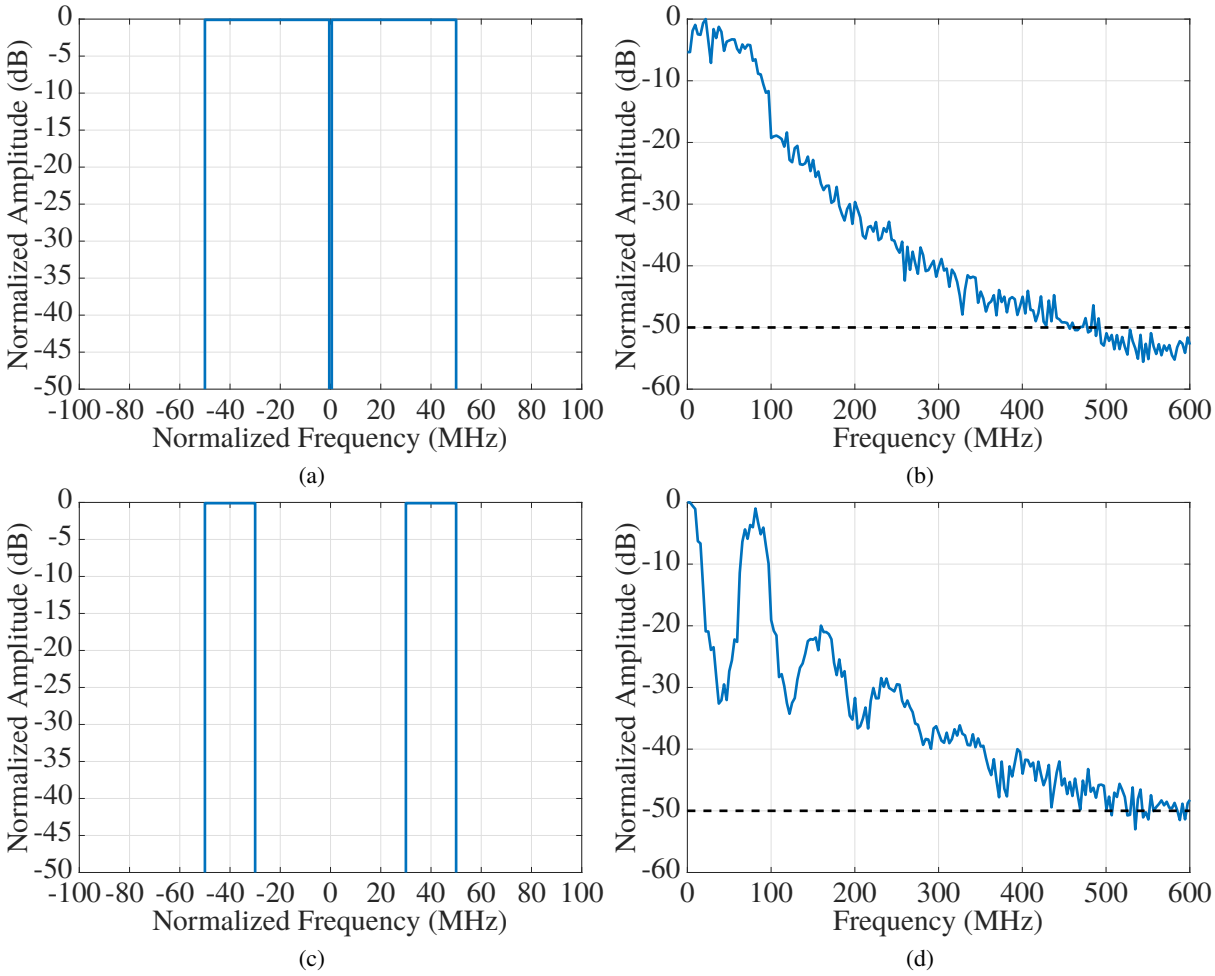


Figure 3.15: (a) One 100 MHz NPR signal and (b) envelope of the signal.(c) Two 20 MHz LTE signals spaced 80 MHz in bandwidth and (d) envelope of the signal.

cyclic Fourier transform does not introduce any extra distortions, and the equalizer is directly found in the frequency domain by comparing to the original noise signal applied on the gate. This results in a flat frequency response at the PA transistor gate from DC to 65 MHz.

3.3.4 Signals

The two signal cases examined in this work are: broad instantaneous bandwidth signals, such as the ones used in the characterization of satellite communications systems, and multiple broadly spaced signals being transmitted through an amplifier simultaneously, as in carrier aggregation.

A noise like signal is used for testing noise power ratio (NPR). The test signal is generated by creating

30,001 carriers in the frequency domain and ascribing them a random, uniformly distributed phase from 0 to 2π. At the center frequency of the signal 1 % of the carriers are removed. In the time domain, this signal generation results in in-phase/quadrature signals with uncorrelated Gaussian amplitude distributions and a composite signal with a Rayleigh distributed amplitude. The PAPR of the signal is greater than 10 dB [73]. This type of signal is used for testing in satellite communication applications. The metric of linearity checks for regrowth within the signal bandwidth. For these applications broadband communication channels are used (up to 2 GHz) making efficient signal transmission challenging. A 100 MHz version of this signal is shown in Fig. 3.15a as it's the envelope which does not drop below -50 dBc until 500 MHz Fig. 3.15b.

The other case is more commonly used in cellular communication systems. This is a carrier aggregation situation in which two signals are concurrently amplifier by the same amplifier. In Fig. 3.15c two 20 MHz LTE signals are shown for an intra-band case. More broadband signal spacing are also possible for the inter-band cases. As the signal spacings increase, the baseband envelope will increase to even larger bandwidths as seen in Fig. 3.15d where the envelope does not drop below -50 dBc until 600 MHz.

3.4 Summary

In this section the general equipment, hardware, and test procedures used throughout this work are discussed. Several common linear tracker circuits are used and the test methods developed in this work, a general overview of their design and performance along with pictures are shown. General test benches are then discussed in context of the supply modulator circuits used. The signal types of interest in this work are then discussed.

The details presented in this chapter are contained in publication [22, 55, 70, 74–80].

Chapter 4

Multiple Signal Supply Modulation for Carrier Aggregation

Contents

Carrier aggregation, seen visually in Fig. 4.1 from [81] is a method in which a single user is assigned multiple carrier frequencies simultaneously. Traditionally this can be done using a different amplifier for each of the transmit and receive bands. However to reduce the number of amplifiers in the system multiple frequencies are transmitted through a single amplifier. Currently intra-band carrier aggregation [1, 2], when multiple unique signals are transmitted simultaneously in the same band, can be used up to a 100 MHz bandwidth posing difficulties for both efficient and linear amplification. As transmitters move to inter-band

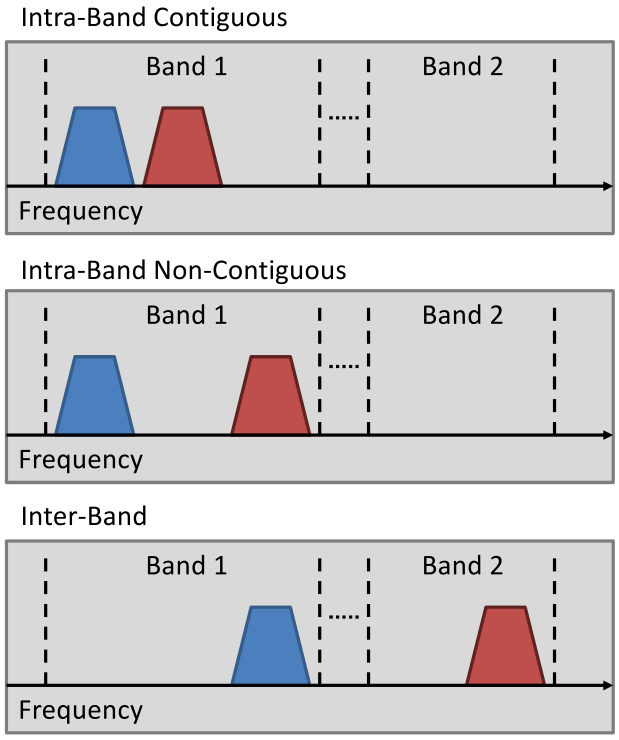


Figure 4.1: Simplified block diagram showing the three cases of carrier aggregation used.

carrier aggregation, when multiple unique signals are transmitted simultaneously in different bands, the instantaneous bandwidth being amplified will increase beyond 100 MHz posing still greater challenges for both efficient amplification and supply modulation.

The large instantaneous bandwidths required for inter-band carrier aggregation make continuous envelope tracking impractical. When multiple simultaneous signals are amplified, the resulting overall signal bandwidth increases as a function of signal spacing, making efficient tracking difficult. A possible solution is to track the sum of envelopes (SoE), rather than the envelope of the composite signal, as presented in [74, 82–84]. This results in a trajectory that can be tracked with a slower and more efficient supply modulator. The goal of the work presented here is to demonstrate that an increase in average efficiency is possible while maintaining linearity.

A method for overcoming the limitations of past slew rate reduction techniques is proposed in [85–88]. The method, referred to as power envelope tracking, or just power tracking (PT), only uses the even terms of a power series of the signal envelope, see Fig. 4.2. Neither early trajectory designs, reviewed in e.g. [89],

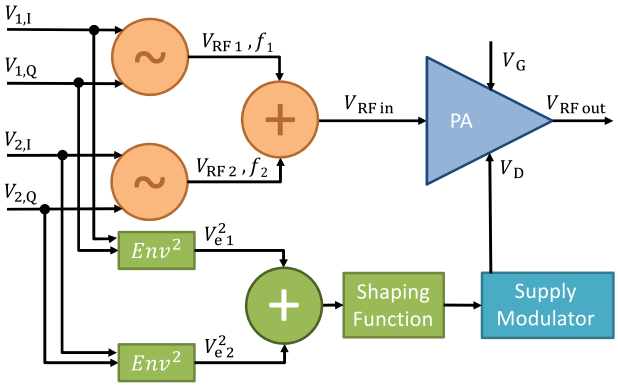


Figure 4.2: Block diagram of a concurrent dual-signal transmitter with supply modulation. The shaping functions, or trajectories, are expressed in terms of the square of the envelope, or more generally a power series with even powers of the envelope. The two signals V_{RF1} and V_{RF2} are at frequencies f_1 and f_2 that are arbitrarily spaced within the PA RF operating band.

or more recent ones, e.g. [90, 91] aim to reduce envelope bandwidth. In this chapter, the PT approach is investigated by optimizing different metrics, such as peak power-added efficiency (PAE), flat gain and a trade between linearity and efficiency. First we present results for a single signal, followed by an extension to two widely separated signals. We show that the PT method used in conjunction with average SoE tracking [92] results in a band-limited trajectory for multi-signal envelope tracking.

Then to demonstrate the new approach, a high-efficiency octave bandwidth (2-4 GHz) GaN power amplifier, based on the design originally presented in [55] with two widely-spaced signals, is expanded to a supply modulated transmitter. The PA is first characterized statically for amplitude and phase variation over input drive for trajectory design. Several different trajectories for PT are designed and discussed in terms of bandwidth-reduction and linearity. The octave bandwidth amplifier is tested using a 10-MHz LTE signal with supply modulation, and results with and without digital pre-distortion (DPD) are compared. Multi-signal efficient amplification is next shown using two 10-MHz LTE signals 800 MHz apart, using a new supply modulation trajectory, and efficiency improvement is demonstrated for a linearized PA. Then results for an X-band PA are shown with Peak SoE tracking with three signals is shown motivating a discussion of the limitations of these methods for an increaseing number of signals.

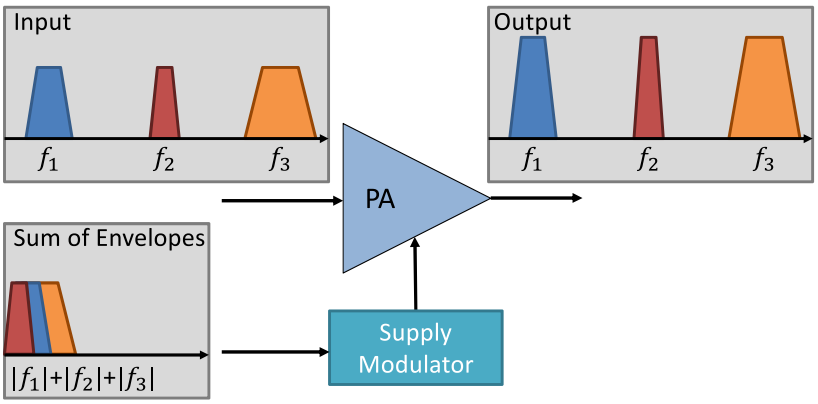


Figure 4.3: Block diagram of amplifier transmitting three signals, (f_1, f_2, f_3), using a supply modulation shaping function based on the sum of the three signals.

4.1 Sum of Envelopes Tracking

Three signals f_1, f_2, and f_3 spaced in frequency are amplified by a PA with supply modulator, Fig. 4.3. The total bandwidth of the input signal is approximately $(f_3 - f_1)$, assuming the modulation bandwidth is substantially smaller than the signal separation. Using a conventional ET approach, the bandwidth expansion of the nonlinear envelope computation means that a bandwidth of at least $5 \times (f_3 - f_1)$ is required for the tracker. For our example signals separated by up to 200 MHz, an efficient 1 GHz tracker would be needed, which has not been demonstrated to date.

To reduce the tracker bandwidth requirements, we investigate tracking based on the peak sum of the envelopes [74, 93, 94]. In peak SoE tracking, the peaks of the signals are tracked:

$$V_{\hat{\text{S}}\text{in}} = \Sigma_i^N V_{\text{in}_i} \tag{4.1}$$

where V_{in_i} is the envelope of one of the N multiple signals. Conceptually, this approach treats the multiple signals as time-varying vectors, and tracks the amplitude of the worst-case envelope, i.e. the condition when all vectors add constructively. In this way, the composite signal is never clipped by the tracker. Qualitatively, the sum of envelopes has dynamics dominated by that of the fastest-varying signal. Note that it is only the modulation bandwidth, not the separation of the carrier frequencies, that affects the tracking signal as this computation is performed on the baseband signals.

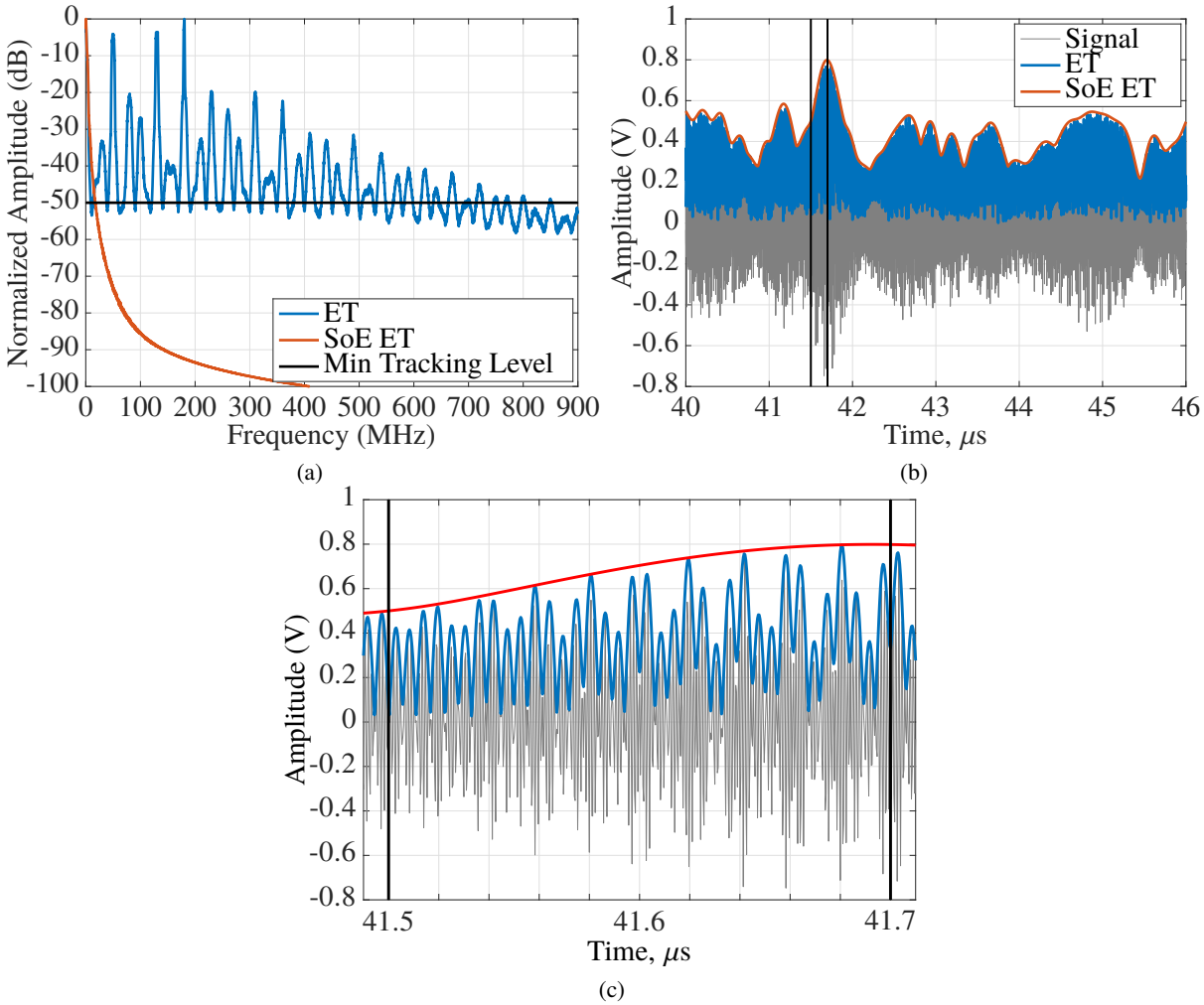


Figure 4.4: (a) Spectra of combined envelope (blue) and summed envelopes (red). (b) Time domain waveforms of the same and (c) Zoomed in time domain waveform showing the carrier, combined envelope and summed envelope.

The frequency-domain analysis is shown in Fig. 4.4a(a) and confirms the bandwidth benefits of this approach. The envelopes of three 16QAM signals centered around 9.8 GHz with bandwidths of 1, 3, and 5 MHz and with various spacings (as detailed in Table I), are combined. Conventional ET requires 800 MHz tracking, while tracking the sum of envelopes requires only 17 MHz, a reduction by approximately a factor of 50 in bandwidth. Fig. 4.4b(b) compares the combined RF signal (grey), its envelope (blue), and the sum of envelopes signal (red). In the zoomed in section of Fig. 4.4c(c), it can be seen that the sum of envelopes tracks the peak of the conventional envelope signal at much lower bandwidth, but does not deviate into the troughs of the signal. When an ideal class-B PA is assumed, the simulated efficiency when the sum of the

envelopes is tracked is 52%, whereas linear class-B operation at peak output power results in only 23% efficiency.

4.2 Trajectory Design for the Octave Bandwidth PA

To achieve high efficiency in an envelope tracking power amplifier, a specific trajectory $V_D(V_{in})$ is selected, and will be different from, e.g., a flat gain trajectory. Because switching power supply modulators degrade in efficiency as switching frequency increases, a trajectory that minimizes envelope bandwidth is used to improve composite transmitter efficiency. Traditional methods of trajectory design aim to create an accurate tracking function but do not minimize the envelope bandwidth of the signal [90, 91]. Other methods of trajectory design aim to reduce the required slew rate (or envelope bandwidth) while sacrificing the accuracy of the tracking function and eliminating the clear $V_D(V_{in})$ function [25–27].

4.2.1 Signal Power Tracking

A method for overcoming the limitations of previous slew-rate reduction techniques is proposed in [85–88]. The method, referred to as power tracking (PT), fits the desired $V_D(V_{in})$ trajectory by approximating it as a first or second order power series of the envelope. This method uses only even exponents of the series, resulting in a supply voltage that is proportional to the power, square of the power, etc. of the signal. This in turn results in a tracking bandwidth limited to integer multiples of the signal bandwidth. For example, for a quadratic series it reduces to the signal bandwidth, while for a 4-th power of V_{in}, or second-order PT (PT2), the required tracking bandwidth is twice that of the signal.

The envelope, V_{in}, of the RF signal can be used to generate a tracking trajectory as:

$$\begin{aligned} V_{in} &= \sqrt{V_I^2 + V_Q^2} \\ B_e &= \infty \end{aligned} \tag{4.2}$$

Due to the presence of the square root function, the resulting envelope bandwidth, B_e, in general is infinite, although there are some cases such as an AM signal where the bandwidth is finite. The increased bandwidth is explained mathematically by looking at the infinite series expansions of a square root function

in (1.9). Raising a signal to the n-th power increases the signal bandwidth by a factor of n, and taking the square root of that function results in an infinite sum and therefore an infinite bandwidth. The coefficients a_n drop with higher values of n due to the $\frac{1}{n!}$ term. The higher frequency components can be truncated when developing a trajectory, as their low values do not have an effect on the performance.

Now it is perhaps clearer why PT, based on even powers of V_{in} reduces the required tracking bandwidth by removing the square root function, thus creating a band-limited trajectory with a bandwidth matching that of the RF signal, B_{RF}:

$$\begin{aligned} V_{\text{in}}^2 &= V_{\text{I}}^2 + V_{\text{Q}}^2 \\ V_{\text{PT}} &= a_0 + a_2 \cdot V_{\text{in}}^2 \\ B_{\text{e}} &= B_{\text{RF}} \end{aligned} \tag{4.3}$$

This function can be extended to higher orders for more accurate tracking. Second order PT is given by:

$$\begin{aligned} V_{\text{PT2}} &= a_0 + a_2 \cdot V_{\text{in}}^2 + a_4 \cdot V_{\text{in}}^4 \\ B_{\text{e}} &= 2 \cdot B_{\text{RF}}, \end{aligned} \tag{4.4}$$

where the coefficients (a_0, a_2, and a_4) can be selected to fit a trajectory that optimizes a given metric.

4.2.2 Single Signal Trajectory Design

The octave bandwidth amplifier used is discussed in Section 3.1.1. Two trajectories are developed to compare the performance of PT to a "traditional" trajectory, one for flat gain and one for maximum PAE. The former sets the PA gain to a constant value as the input voltage varies, while the latter follows the peak PAE points for each of the drain supply voltage level PAE(P_{in}) curves. The results from this analysis at 2.1 GHz are shown in Fig. 4.5. Measurements are performed using a power calibrated VNA with an external test set; this extracts static AM/AM and AM/PM data in a fully calibrated environment. Drain voltage is swept in 1 V steps from 6 to 28 V.

Fig. 4.5 shows the response of the PA with the seven trajectories calculated from the static measurements. The traditional trajectories better track the $V_{\text{D}}(V_{\text{in}})$ characteristic they are selected to follow. The maximum PAE (max-PAE) tracking function is able to hit the peaks of the PAE(P_{in}) for each voltage level, while the

flat gain function results in a perfectly flat gain. The PT cases approximate these ideal trajectories. It should be noted that all of these trajectories increase phase distortion from 3 deg with a constant 28 V to 10 deg with a varying supply.

The seven trajectories and their corresponding spectra are shown in Fig. 4.6. The spectral benefit of PT can be seen in Fig. 4.6a: the 28-37 MHz bandwidth required for standard envelope tracking of a 10 MHz LTE signal (including two 0.5 MHz guard bands) is reduced to 9 MHz, where bandwidth is defined at frequencies where the spectrum amplitude drops by 50 dB (excluding the dc offset). Fig. 4.6b shows that the max-PAE PT trajectory is a shallower version of the traditional max-PAE trajectory. A higher order function better approximates the shape, as seen with the PT2 case. The traditional flat-gain trajectory is a kinked line which also cannot be approximated by a first order PT. The PT2 case offers a closer approximation but still does not perfectly track the original case, which implies that the AM-AM distortion is increased.

The performance of the octave bandwidth amplifier is analyzed, as a first-order approximation, by assuming a memoryless model and applying the gain and phase trajectories developed from the static measurements to a 10 MHz LTE signal. The results of this analysis are given in Table 4.1. Note that for all supply modulated cases the PAE is approximately the same at 40 %. For the max-PAE tracking cases the gain of the transmitted signal is reduced compared to the static case, and there is a 3-7 dB decrease in normalized mean square error (NMSE), described in (1.2).

Table 4.1: Comparison of Different Trajectories

Trajectory	Pout	Gain	η_D	PAE	NMSE	ACPR
Static V_D	33.6	13	24.7	23.4	-16.8	-31.9
max-PAE	30.8	6.7	51.6	40.5	-9.08	-26.5
max-PAE PT	32.3	8.1	49.9	42.2	-13.4	-31.5
max-PAE PT2	31.4	7.2	50.6	41	-9.2	-31.5
flat-gain 10dB	34.2	10	44	39.6	-31.8	-38.3
flat-gain PT	33.7	9.5	45.4	40.3	-24.4	-36.6
flat-gain PT2	33.9	9.7	45.2	40.4	-27.4	-35.3
Optimized PT2	33.7	9.5	45.2	40.2	-24.3	-36.9

PT: Power Tracking, PT2: 2^{nd} order PT
Pout(dBm), Gain(dB), PAE(%), η_D(%), NMSE(dB), ACPR(dBc)

The flat-gain cases offer a better compromise than the max-PAE case, since the PAE remains the same

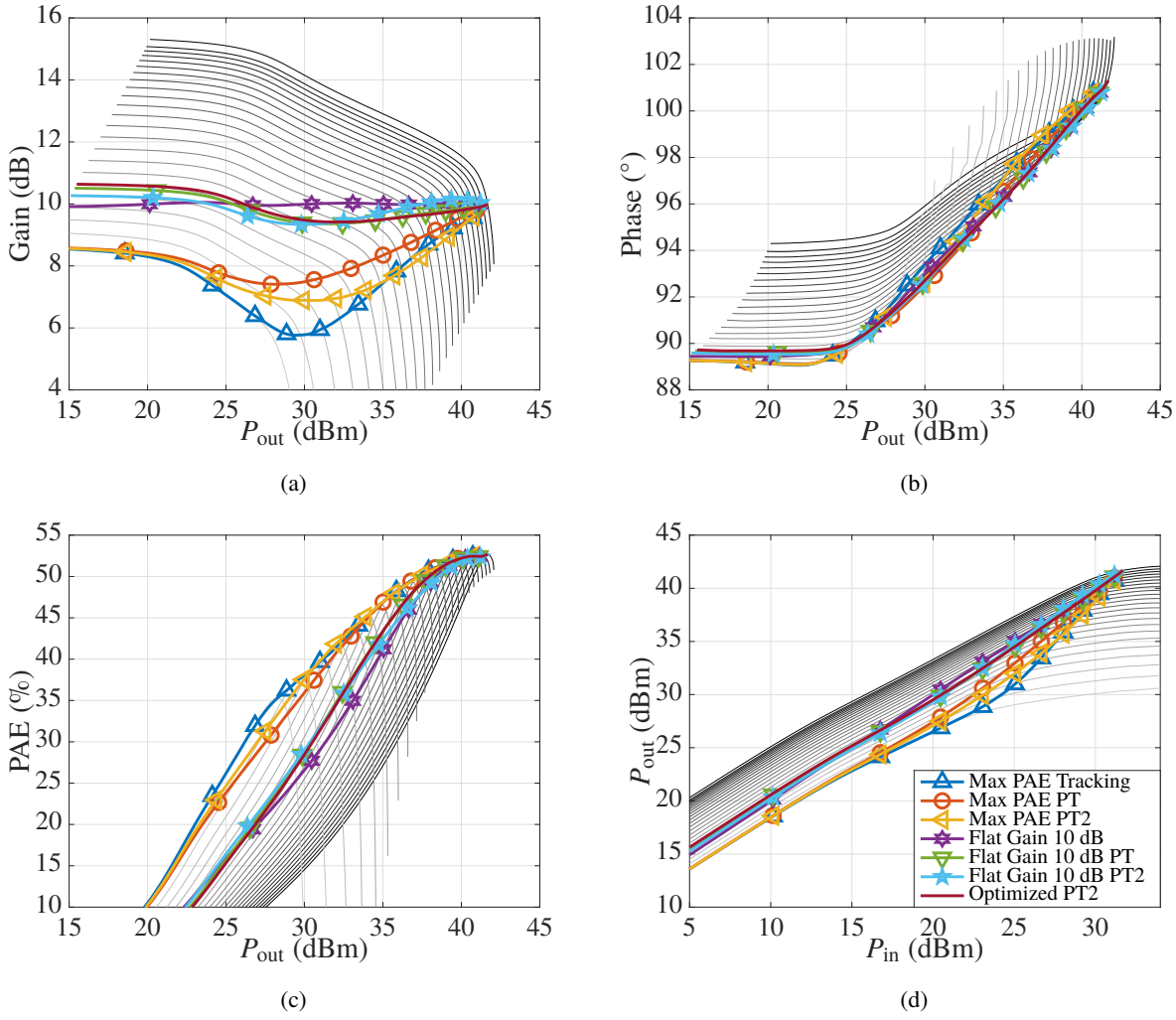
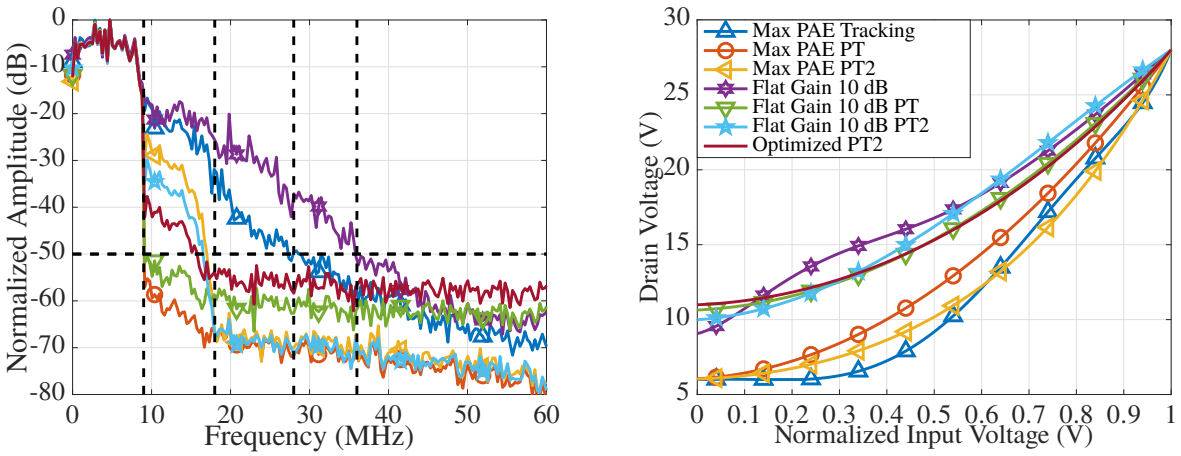


Figure 4.5: Measured (a) gain amplitude, (b) phase and (c) PAE vs. output power, as well as (d) compression curves of the octave bandwidth PA from Fig. 3.1c shown in gray lines as a function of drain voltage (6-28 V in 1 V steps). Seven trajectories are superimposed onto static measurements. Darker lines indicate higher drain voltages.



(a) (b)

Figure 4.6: (a) Simulated normalized amplitude vs. frequency for the four synthesized trajectories. Note that the PT trajectory results in a 9-MHz bandwidth, while PT2 gives 18 MHz. In contrast, the traditional envelope trajectories extend to 28-37 MHz. (b) Drain supply voltage vs. normalized input voltage for the seven trajectories. The PT and PT2 trajectories are smoother, as they use fewer terms.

while the linearity is improved. An "optimized PT2" trajectory was created by maximizing PAE and the linearity metric STDR (signal to total distortion ratio), presented [95]. The goal of STDR is to describe spectral and time domain based nonlinearities with a single metric as opposed to using a different metric to access spectral and time domain linearity. The optimization is done in simulation using the methods described in Section2.2.1 and consists of identifying coefficients that improve both STDR and PAE simultaneously, equal weighting was ascribed to both metrics.

If the amplifier is operated at another frequency, a look-up table of PT coefficients can be created for each operating point. The effect of using the ideal (non PT) trajectories developed for a signal at 2 GHz and applied to different frequencies is examined in Fig. 4.7a for the max-PAE case and Fig. 4.7b for the flat-gain 10 dB case. Seen in Fig. 4.7a, using the max-PAE trajectory developed at 2 GHz at different frequencies will have a small (less than 1 percentage point) effect on PAE as a function of output power. Applying the flat-gain trajectory developed for 2 GHz to other frequencies results in an output with flat gain (± .5 dB) as a function of P_{out} but does not result in the target gain, shown in Fig. 4.7b.

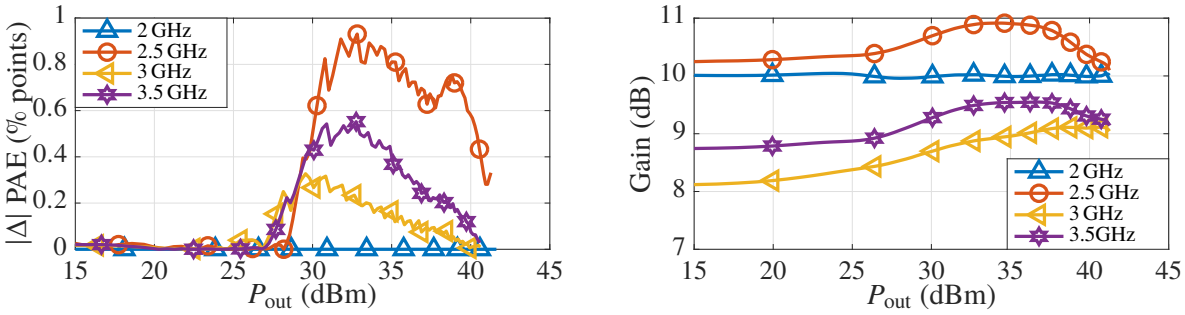


Figure 4.7: (a) Variation in PAE at several (2.5,3,3.5 GHz) frequencies for the Max-PAE trajectory created at the each respective frequency point versus the one created at 2 GHz and applied at the other frequency points. Applying the trajectory designed at 2 GHz to the other frequencies will result in a less than 1 percentage point variation in PAE. (b) Variation in Gain at several (2.5,3,3.5 GHz) frequencies applying the flat gain 10 dB trajectory made for 2 GHz. Note that even though the gains do not stay constant at 10 dB, gain variation for the power sweeps is ± .5 dB.

4.2.3 Two-Signal Trajectory Design

In carrier aggregation, an amplifier is driven by multiple signals across its operational bandwidth. Supply modulation for efficiency enhancement will differ in this case compared to a single signal, since the total signal bandwidth and PAPR are increased. Generating a trajectory for two signals can be done as in (4.2), where the I and Q components of the composite signal are considered. However, doing this would result in a tracking bandwidth of at least $5 \cdot (f_2 - f_1)$ for a two-signal case. Due to the inverse relationship between switching supply speed and efficiency, as signal spacing increases this technique becomes less practical.

A method for overcoming this is called sum of envelopes (SoE) tracking. Performing SoE tracking reduces the bandwidth requirements for the supply modulator to that of the largest individual signal bandwidth. There are two main SoE approaches: peak SoE (shown in (4.1) and discussed in Section 4.1) and average SoE [92]. Average SoE tracking, is defined as:

$$V_{\overline{\text{Sin}}} = \sqrt{\Sigma_i^N V_{\text{in}_i}^2} \tag{4.5}$$

Both methods provide an improvement in efficiency though average SoE is shown in [92] to provide a larger improvement.

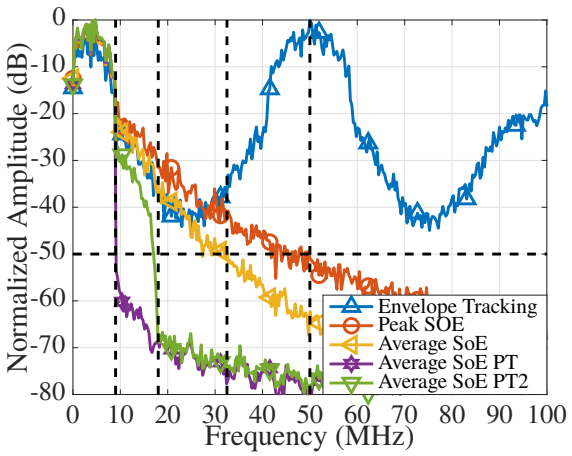


Figure 4.8: Normalized spectra of 5 trajectories for multi-signal envelope tracking. Two 10 MHz LTE signals are used with a 50 MHz spacing.

The techniques discussed earlier for PT are easily applicable to (4.5). Expanding this equation for two signals gives:

$$V_{\overline{\text{Sin}}} = \sqrt{\left(\sqrt{V_{1,\text{I}}^2 + V_{1,\text{Q}}^2}\right)^2 + \left(\sqrt{V_{2,\text{I}}^2 + V_{2,\text{Q}}^2}\right)^2} \tag{4.6}$$

This is simplified to :

$$V_{\overline{\text{Sin}}} = \sqrt{V_{1,\text{I}}^2 + V_{1,\text{Q}}^2 + V_{2,\text{I}}^2 + V_{2,\text{Q}}^2} \tag{4.7}$$

The function in (4.7) can then be used with (4.3) to produce a PT trajectory that is band-limited to the signal bandwidth, or with (4.4) to twice the signal bandwidth. This method can be used with average SoE tracking since squaring the absolute value function eliminates the square-root function from the envelope. If this method were used with peak SoE tracking, the square root of the calculation of the V_{in_i} would not be removed, and the resulting function would not be band-limited.

Trajectories are designed for five cases of two 10-MHz signals separated by 50 MHz: envelope tracking, peak SoE tracking, average SoE tracking, average SoE PT and average SoE PT2. A 50 MHz spacing is used for this simulation to allow easier visualization of the concepts discussed in this chapter, later testing is done with an 800 MHz spacing. The resulting spectra are given in Fig. 4.8. The PT trajectories band limit the

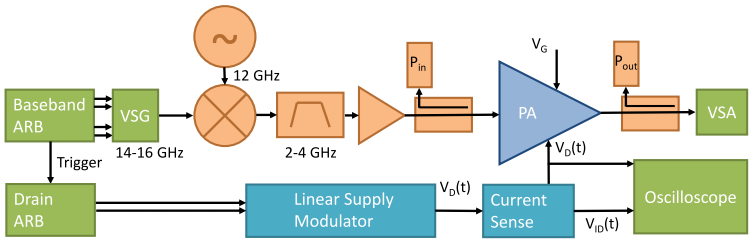


Figure 4.9: Block diagram of measurement setup for validating trajectory design applied to the octabe bandwidth GaN PA from Fig. 3.1c.

required tracking spectrum to the signal bandwidth for PT, and twice the signal bandwidth for PT2. The average SoE and peak SoE trajectories have tracking bandwidths of 32 MHz and 50 MHz, respectively. Note that for a 50 MHz signal spacing, traditional envelope tracking would require a tracking bandwidth exceeding 500 MHz.

4.3 Measurement Methods and Results

A test bench developed to validate the tracking theory described above is shown in Fig. 4.9 and makes use of the calibration procedure described in Section 3.3.1. This configuration enables the generation signals with up to 1 GHz bandwidth, however at lower carrier frequencies (<3.2GHz), the bandwidth that the VSG can generate without distortion is reduced to 130 MHz. To overcome this, the VSG operates in X-band, and a mixer is used to downconvert the signal to the band of interest (2-4 GHz). The signal is then received at both the input and output of the DUT using a (VSA) which has a maximum receive bandwidth of 160 MHz. Measurements at the input of the DUT evaluate the linearity of the test bench itself. Testing uses the linear tracker described Section 3.2.1a.

4.3.1 Single Signal Results

Linearity testing of the PA is performed using a 10-MHz LTE down-link signal with PAPR=8.5 dB generated in MATLAB. Measurements are first done with the original signal, and subsequently with DPD applied. The PA is linearized using the model shown in [96] with a 7^{th} order polynomial and 7 memory taps; the long term stability of the DPD coefficients was not investigated. The DPD is first applied to the signal and then

Table 4.2: Comparison of Different Trajectories at 30 and 33 dBm Output Power

Trajectory	Pout (dBm)	Gain (dB)	PAE (%)	η_D(%)	NMSE (dB)	$ACPR_L$ (dBc)	$ACPR_U$ (dBc)
Static V_D	30	13.4	14.1	14.7	-20	-35.6	-35.4
w/ DPD	29.8	**13.4**	13.7	14.4	**-33.5**	**-49.2**	**-50.4**
max-PAE PT	30.1	6.19	**34.9**	46	-12.4	-30	-30.9
w/ DPD	30.1	6.27	34.3	44.9	**-31.3**	**-45.6**	-43.2
max-PAE PT2	29.9	5.16	33.4	**48.1**	-11.1	-32.9	-36.2
w/ DPD	30	5.43	34.1	47.7	**-33.5**	**-47.4**	**-49.2**
flat-gain PT	29.9	8.47	28.8	33.5	-24.5	-36.9	-37.3
w/ DPD	29.7	8.5	27.7	32.3	**-33**	**-47**	**-49**
flat-gain PT2	29.9	8.38	29.1	34	-18.1	-32.7	-33.6
w/ DPD	30.2	8.47	29.5	34.4	**-33.1**	**-47.5**	**-49.5**
Optimized PT2	30	8.48	28.4	33.1	-27	-38.3	-38.8
w/ DPD	30.3	8.51	29	33.8	**-33.9**	**-50.8**	**-49.8**
Static V_D	32.9	**12.8**	20.8	22	-19.3	-37	-37.2
w/ DPD	33	12.6	21.4	22.6	**-33.5**	**-49.7**	**-51.1**
max-PAE PT	32.9	6.45	40.8	52.8	-11.7	-28.1	-28.5
w/ DPD	33.1	6.62	**41**	52.4	-27.7	-42.5	-40.6
max-PAE PT2	32.5	5.22	38.3	54.7	-9.3	-27.9	-29.3
w/ DPD	33.4	5.52	39.8	**55.3**	-26.9	-43.6	-41.6
flat-gain PT	32.8	8.5	37.4	43.5	-20.6	-33.6	-34.5
w/ DPD	32.9	8.51	37.1	43.2	**-34.5**	**-50.3**	**-49.7**
flat-gain PT2	33	8.67	37.8	43.7	-19	-30.6	-31.1
w/ DPD	33.1	8.67	37.4	43.2	**-32**	-41.2	-42.1
Optimized PT2	32.9	8.42	37	43.2	-22.2	-34.5	-36.3
w/ DPD	32.9	8.48	36.9	43	**-33**	**-50.1**	**-49.6**

PT: Power Tracking, PT2: 2^{nd} ord. PT

the pre-distorted signal is used to generate an updated trajectory for the supply modulator, this maintains the same $V_D(V_{in})$ characteristic with or without DPD.

The PA output power is stepped in 0.5 dB increments from 27-35 dBm. At each power level the DPD algorithm generates a new signal. The DPD algorithm linearizes to the same peak output power level achieved in the characterization. It does not additionally adapt the average input power to match the average characterization output power. The trajectories are designed from Fig. 4.6b for the output powers shown in Table I. If the PA is over-driven and the voltage expected to swing above 28 V, we clip the trajectory which expands the bandwidth, although it is possible to redesign the trajectory with clipping in mind. If on the other hand the PA is under-driven and the peak voltage does not reach 28 V, the trajectory remains the same but the peak voltage is reduced. Measured results at 2.1 GHz are shown in Fig. 4.10, where the drain efficiency, gain and NMSE are presented for 12 different cases (6 without DPD). The DPD provides improvement,

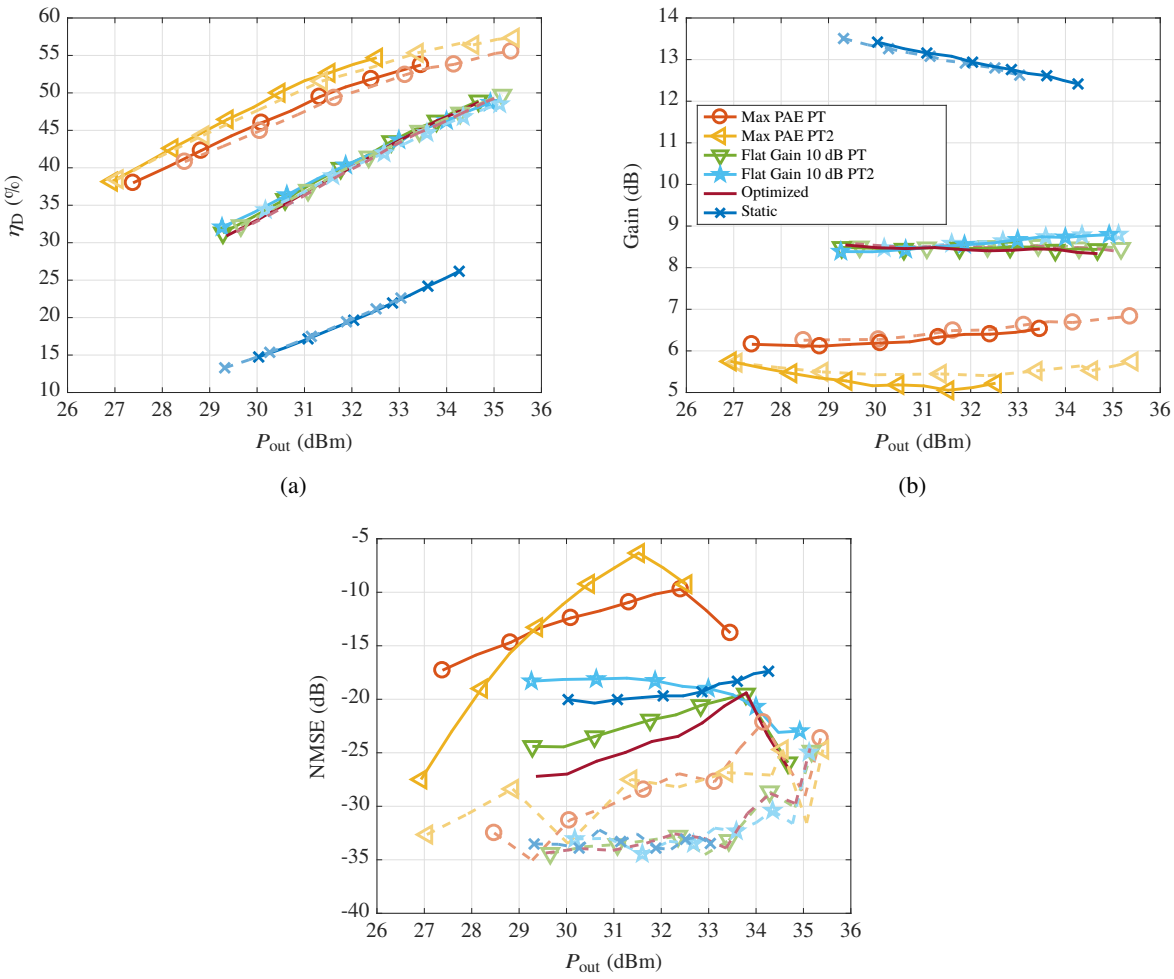


Figure 4.10: Measured (a) η_D, (b) gain and (c) NMSE vs. output power for 6 different cases, with (dashed faded lines) and without (solid lines) DPD for a single 10-MHz signal at 2.1 GHz.

particularly at lower power levels and for trajectories that flatten gain. It is interesting to observe that with the addition of DPD, the average output power of the max-PAE case increases. This can be attributed to the expansive gain characteristic of the octave bandwidth amplifier, seen in Fig. 4.5a, when tracked for the max-PAE PT/PT2 cases. Linearizing the amplifier in these cases requires an input signal that has a higher average power than the signal without DPD, resulting in a higher output power.

Selected results of these measurements are displayed in Table 4.2 for 30 dBm average output power (top) and 33 dBm average output power when the PA is compressed (bottom). The following conclusions can be made:

Table 4.3: Comparison of Different Trajectories for Two Signal Operation

Trajectory	Pout (dBm)	Gain (dB)	PAE (%)	η_D (%)	$NMSE_1$ (dB)	$ACPR_1$ (dBc)	$NMSE_2$ (dB)	$ACPR_2$ (dBc)
Static V_D	29.9	13.3	13.3	13.9	-22.1	-34	-24.2	-33.7
w/ DPD	30	13.3	13.7	14.4	**-31.9**	-44.8	**-30.7**	**-45.9**
max-PAE PT	30.1	7.98	30.9	36.8	-8.05	-26.3	-7.91	-27.3
w/ DPD	30.2	7.78	29.4	35.3	**-31**	**-47**	**-31.7**	**-48**
max-PAE PT2	29.8	7.14	**31.3**	**38.8**	-5.57	-26	-6.91	-27.1
w/ DPD	30.4	7.25	31.2	38.4	**-30.9**	-41.4	**-31.7**	-41.5
flat-gain PT	29.7	8.99	25.1	28.8	-14.8	-32.7	-13.6	-33.1
w/ DPD	30.1	8.98	25.4	29.1	**-32.5**	**-45.4**	**-32.1**	**-45.7**
flat-gain PT2	29.8	9.13	25.3	28.8	-13.5	-31.1	-12	-31.8
w/ DPD	29.7	9.15	24.6	28	**-32.9**	**-46.3**	**-31.9**	**-46.6**
Optimized PT2	29.8	9	25	28.6	-16.3	-33.4	-14.2	-33.4
w/ DPD	30	9.05	25.2	28.8	**-32.5**	**-46.2**	**-32.8**	**-46.7**
Static V_D	32.5	12.9	19.7	20.8	-21.8	-34.6	-23.8	-32
w/ DPD	33	12.4	20.9	22.2	-29.4	-40	-28.7	-42.6
max-PAE PT	32.9	9.29	35.3	40	-10.8	-24.7	-6.14	-25.2
w/ DPD	33.1	8.77	34.9	40.2	**-32.8**	**-47.5**	**-32.9**	**-46.9**
max-PAE PT2	32.8	9.15	35.8	40.8	-10	-23.2	-5.53	-23.7
w/ DPD	33.2	8.09	35.9	42.5	**-30.8**	-38.7	-29.3	-38.5
flat-gain PT	32.6	9.49	32.5	36.7	-12.7	-29.8	-10.2	-30
w/ DPD	33.1	9.45	32.8	37	**-32.8**	**-46**	**-32**	**-45.6**
flat-gain PT2	32.7	9.63	31.6	35.5	-12.5	-28.5	-10.7	-29.6
w/ DPD	33.1	9.6	31.8	35.7	**-32.6**	**-46.8**	**-30.1**	**-47.3**
Optimized PT2	32.6	9.21	31.9	36.2	-11.4	-29.6	-10.7	-31.1
w/ DPD	33	9.24	32.3	36.6	**-30.3**	**-46.7**	**-31.3**	**-48.4**

PT: Power Tracking, PT2: 2^{nd} ord. PT

- Using a static supply provides the highest gain with the lowest efficiency and a competitive linearity.
- The PT and PT2 max-PAE cases provide the highest PAE and η_D but these trajectories also have the lowest gain and worse raw linearity.
- The flat-gain cases and the optimized PT2 case for minimized NSME and maximized PAE provide very similar performance in terms of gain and efficiency. Though the gain is designed to be 10 dB from the static measurements, this is reduced by 1-1.5 dB in the dynamic results. This reduction is a well-known phenomenon in GaN related to trapping effect [34] and was previously reported on in [35, 97]. Dual-pulse characterization of GaN devices and PAs has shown the same effect [98]. This is also observed in the gain performance of the other trajectories.
- The optimized PT2 trajectory does improve linearity over the two flat-gain cases and is seen to have better performance even than the static bias case for some measures of linearity.
- The trends we see are similar to those calculated in Table 4.1. The differences between these results

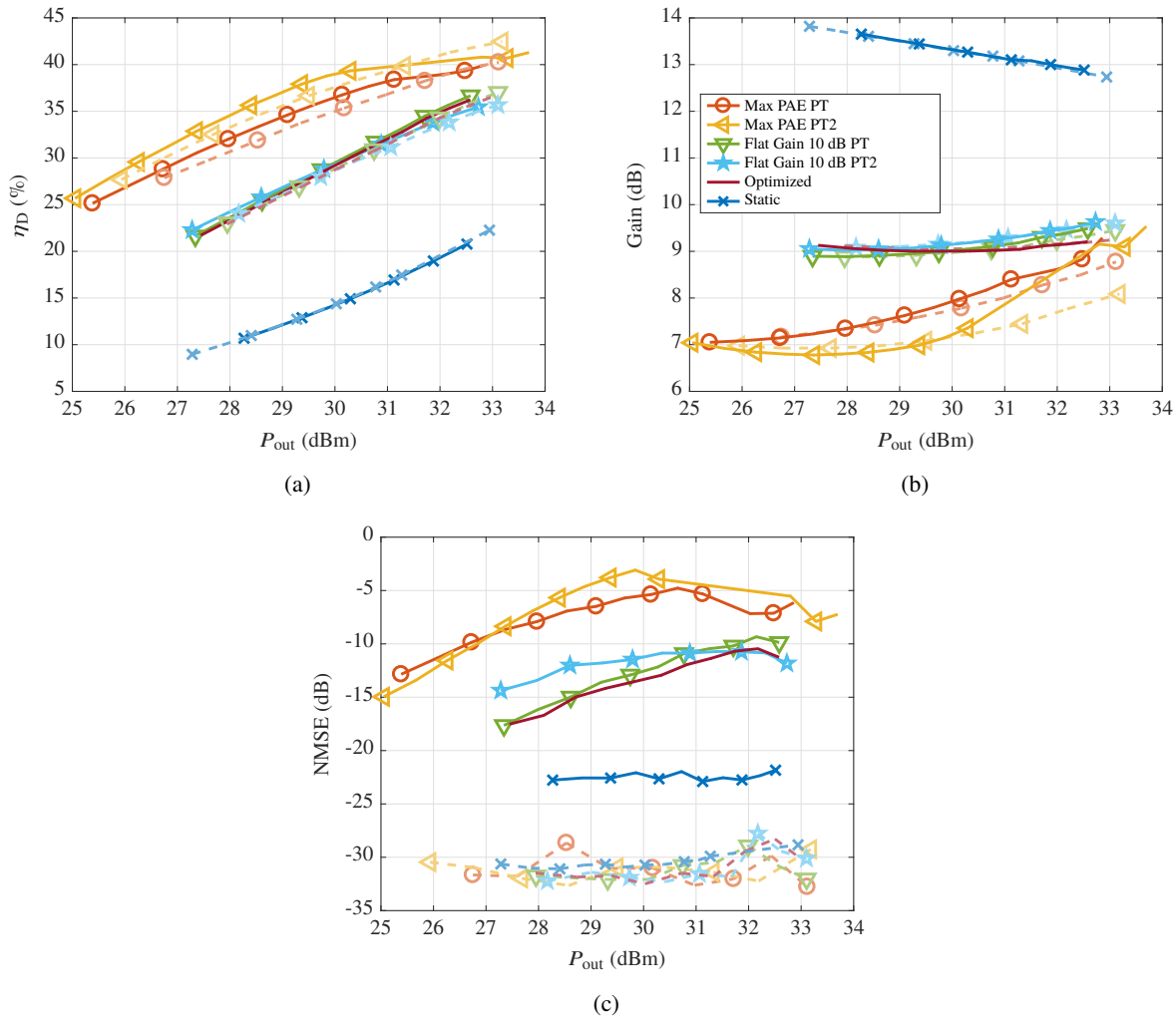


Figure 4.11: Measured (a) η_D, (b) gain and (c) NMSE vs. output power for 6 different cases, with (dashed faded lines) and without (solid lines) DPD for two 10-MHz signals centered at 2.15 and 2.95 GHz (800 MHz apart).

are related to the simplicity of the memoryless model and the use of static measurements to model an amplifier operating in a dynamic fashion.

- Supply modulation increases the drain efficiency by more than 30 percentage points with a greater than 20 percentage point improvement in PAE. At the lower drive level, $P_{out} = 30$ dBm, in conjunction with DPD, and for all but one trajectory, max-PAE PT, achieve less than -45 dB ACPR for both upper and lower channels. For all but the max-PAE PT case, a NMSE< -30 dB is realized.

- At the higher output power level, $P_{out} = 33$ dBm, a reduction in linearity can be observed for all but

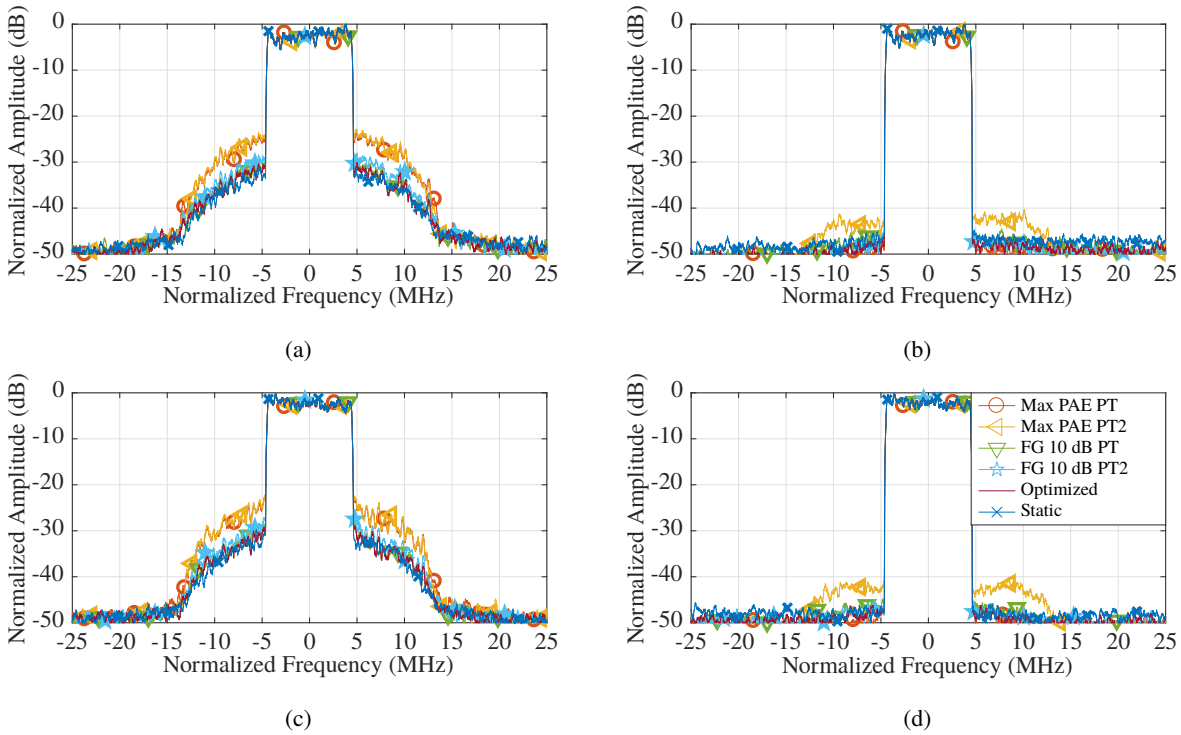


Figure 4.12: Measured spectra for $P_{\text{out}} = 30\,\text{dBm}$ with two signals: (a) lower band; (b) lower band with DPD; (c) upper band; and (d) upper band with DPD.

two cases. The flat-gain and optimized PT2 cases both still show less than -45 dBc ACPR for both the upper and lower channel and a NMSE of less than -30 dB. A higher order memory polynomial might benefit the other cases at a higher power level for achieving ACPR$< -45\,\text{dBc}$.

4.3.2 Dual Signal Results

The octave bandwidth amplifier is tested with two concurrent 10 MHz LTE signals at 2.15 and 2.95 GHz for an 800 MHz total signal spacing. DPD is performed using the algorithm presented in [99], using 7 memory taps and 7th order polynomial for each cross term. As the tracking trajectory changes (and if the signal spacing changes), the DPD coefficients need to be updated. A power sweep is performed for the same trajectories as in the single signal case. The power sweep results are shown in Fig. 4.11.

Selected results of these measurements are summarized in Table 4.3. The two ACPR columns show the worse of the two channels. Supply modulation offers a 14-23 percentage point improvement in drain

Table 4.4: Summary of performance for several signal scenarios

f_1,f_2,f_3 (GHz)	P_1,P_2,P_3	Supply	PAE (%)	EVM (%)		
				1	2	3
9.7, 9.83,9.88	0.33, 0.33,0.33	Track	42.4	13.8	16.7	18.8
		Fixed	29.7	8.7	11.3	14.4
9.7, 9.83,9.9	0.2, 0.5,0.3	Track	41.6	17.2	20.2	24.8
		Fixed	29.4	10.9	6.8	15.3
9.73, 9.85, 9.9	0.33, 0.33, 0.33	Track	41.1	12.3	16.4	19.1
		Fixed	29.8	9.4	10.8	13.9
9.73, 9.85, 9.9	0.2, 0.5, 0.3	Track	40.1	14.1	18.5	19
		Fixed	28.8	9.2	10.6	12.1

efficiency and 12-16 percentage points in PAE, compared to the static supply case. The trends in gain are similar to those seen with one signal, though there is a 0.5 dB higher gain for the flat-gain and optimized PT2 trajectories, and a gain expansion with increasing drive level for the two max-PAE cases. At the lower drive level ($P_{\text{out}} = 30$ dBm) in conjunction with DPD, all but one trajectory, max-PAE PT2, achieve ACPR< -45 dBc for both upper and lower channels. For all but the max-PAE PT2 case, a NMSE< -30 dB is realized. Spectra measurements for the lower drive level case are shown in Fig. 4.12. Similar conclusions can be drawn at the higher output power level ($P_{\text{out}} = 33$ dBm).

4.4 Testing with X-Band PA

Testing is done using the PA discussed in Section 3.1.2. For a 9.8 GHz center frequency, the PA is measured with several different signal scenarios, in which the relative spacing and average power levels are varied. Testing is done using the linear tracker described Section 3.2.1a without the gain stage. A summary of these measurements is given in Table 4.4. For each signal scenario, the PA is measured with and without reduced-bandwidth supply modulation. The PAE values in Table I do not include the efficiency of the linear tracker. Supply modulation improves the PAE by approximately 11 percentage points in each case.

Fig. 4.13a shows the full measured spectrum at the PA with and without supply modulation for the first

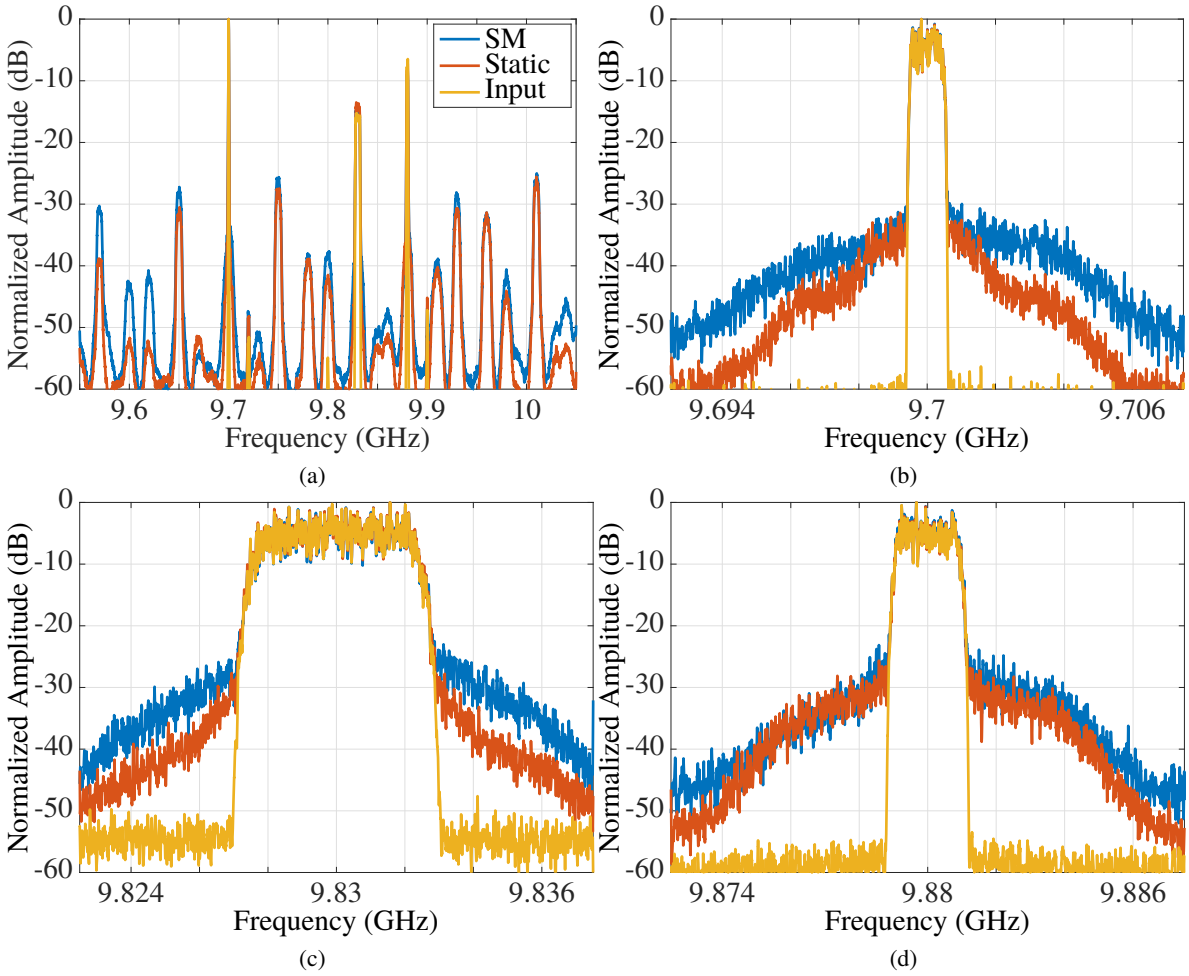


Figure 4.13: (a) Measured spectrum of signals at the PA output with and without reduced-bandwidth supply modulation. Measured normalized individual signal spectra at the input of the PA (green), output of PA with no supply modulation (blue) and output of PA with reduced bandwidth supply modulation (red).

scenario in Table 4.4. Significant mixing products can be seen due to the nonlinearities of the PA, even with a fixed supply. Supply modulation exacerbates this nonlinearity, as is expected from the supply-dependent gain seen in Fig. 3.2b. The normalized individual signal spectra are shown in Fig. 4.13. It is expected that the nonlinearities can be corrected using predistortion techniques such as those described in [82, 94]. Experimental validation shows that this approach results in 12.7 pp higher PAE in an X-band PA operating on three equal-power 16QAM signals within a 200 MHz bandwidth centered around 9.8 GHz. The methods previously discussed for two signals are extended to this three signal case.

4.5 SoE for an Increasing Number of Signals

This Chapter shows two demonstrations, one with two signals spaced in frequency and one with three signals. For a broad instantaneous bandwidth signal rather than tracking the entire signal it might make sense to cut the signal into pieces and use SoE tracking to reduce the modulation bandwidth to a level where a continuous supply can be used. To see the limitations of this method simulations are performed using up to 30 unique LTE test signals with a 5 MHz bandwidth. Signals are placed at 5 MHz increments and then the methods discussed in Section 4.1 are used to analyze the performance of peak sum of envelopes tracking. This analysis, performed for an ideal class-B amplifier, shows the benefits of SoE diminish with an increasing number of signals.

As the number of signals increases the efficiency of sum of envelopes tracking shrinks, seen in Fig 4.14, dropping from a 40 pp improvement for two signals to a <10 pp improvement for 30 signals. As the number of signals increases the envelope bandwidth of the composite signal continues to increase whereas the SoE envelope stays constant, seen in Fig 4.15b.The composite signal PAPR increases, rising by 6 dB as the number of signals increases, seen in Fig. 4.15a. Meanwhile the PAPR of the SoE envelope begins to asymptotically approach 3 dB. Because the signals are effectively independent random variables added on top of one another, this can be explained by the central limit theorem.

For the case of 20 signals, which is effectively a 100 MHz signal, the benefit over the ideal class-B is <10 pp and will be lower in a real implementation. In this case a different approach, such as discrete supply modulation (discussed in Chapter 5 and 7), which can track the composite signal is more effective.

4.6 Summary

This chapter demonstrates an efficient method of amplifying multiple concurrent signals over a large bandwidth using a supply modulation approach. The octave bandwidth amplifier is first tested using a single 10-MHz signal with several reduced-bandwidth supply modulation trajectories that are constructed as an even-termed power series of a 10-MHz LTE signal envelope. With this power tracking (PT) approach, a

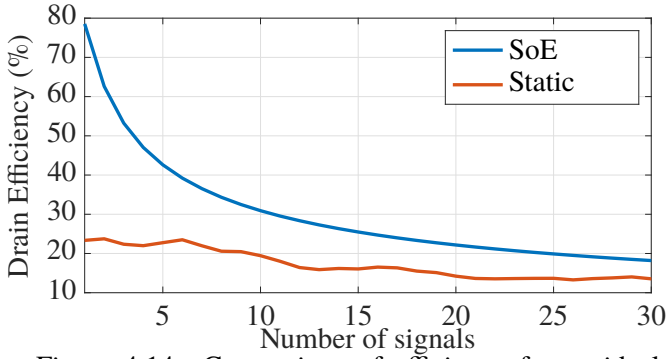


Figure 4.14: Comparison of efficiency for an ideal class-B using a static supply and SoE tracking with an increasing number of signals.

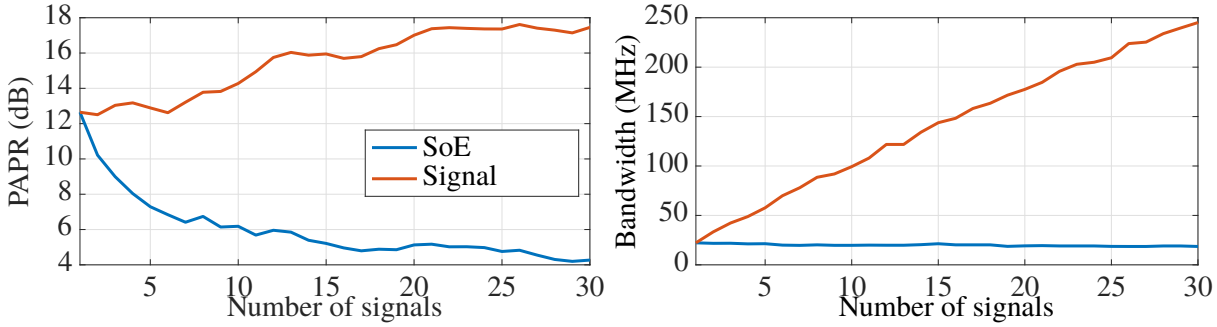


Figure 4.15: (a) PAPR of the signal and the envelope using SoE tracking as the number of signals increases. (b) Bandwidth of the signal envelope and SoE envelope for increasing number of signals.

greater than 30 percentage point increase in η_D is achieved while maintaining less than -45 dB ACPR with digital predistortion. Two 10 MHz LTE signals with 800 MHz spacing are then amplified using a similar bandwidth-reduction technique. A greater than 20 percentage point increase in η_D is seen with an improvement in linearity through the use of multidimensional digital pre-distortion, and several orders of magnitude tracking bandwidth reduction. The method presented here can be extended to more than two concurrent signals of arbitrary spacing for a PA with large RF bandwidth.

The chapter shows that sum-of-envelope power tracking significantly improves PA efficiency for two widely-spaced signals with potentially dynamic and arbitrary spacing, and with a tracking bandwidth that is approximately that of a single signal.

The X-band PA is then tested and PAE improvements of 12.7 pp are observed for three signals with a 200 MHz spacing. In this case digital predistortion is not used so there is a degradation in linearity. To

analyze the effects of an increasing number of signals, a model of an ideal class-B amplifier is used to analyze the effectiveness of SoE tracking with an increasing number of signals.

The details presented in this chapter are contained in publications [55, 70, 74].

Chapter 5

Simultaneous Gate and Drain Modulation

Contents

In this chapter, a method to improve linearity and gain of a drain supply-modulated PA is shown. A GaN X-band PA, described in Section 3.1.2 is tested at 9.7 GHz using a single dynamic supply modulator for both stages. Simultaneously, the gate biases of the transistors in the two stages are varied independently, as shown in Fig. 5.1. An efficient discrete supply modulator, Section 3.2.2c, is used to generate the drain supply voltage, while two high-speed instrumentation amplifiers are used to drive the gates of the amplifier, Section 3.2.1b. Performing gate and drain bias modulation provides the efficiency improvement of drain supply modulation with improved linearity performance by dynamically adjusting the gain and compensating for the phase variation in saturation. This method can be implemented entirely in the analog domain, without the knowledge of digital baseband signals, useful for, e.g. satellite repeaters.

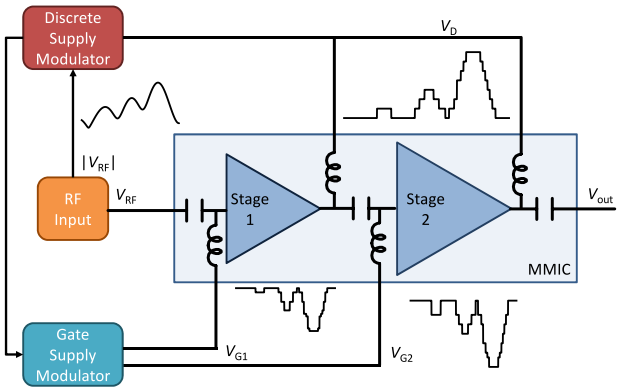


Figure 5.1: Block diagram of a transmitter in which a two-stage PA is supply-modulated with a single dynamic drain voltage V_D and two independently-controlled gate bias voltages, V_{G1} and V_{G2}.

In previous work drain supply modulation with discrete supply modulators effectively improves efficiency for broadband signals, but generally degrades linearity because the power amplifier is in saturation over a larger dynamic power range and the discrete voltage levels add distortions. Gate modulation is shown to improve the linearity of amplifiers under static drain bias conditions in [79, 100], while simultaneous gate and drain modulation are applied to improve supply modulator efficiency in [54], and to improve linearity and efficiency of a single transistor in [101]. Gate modulation is previously investigated for a two-level class-G modulated amplifier [102], but did not show an improvement in linearity with the addition of gate modulation.

Here initial testing is done with only drain modulation. This improves efficiency but not linearity. Next gate modulation using statically determined gate shaping functions improves linearity and efficiency for some cases. Then developing gate shaping functions dynamically rather than statically, results in unique shaping functions at each power level with improvements in both efficiency and linearity. An optimization routine is developed to determine the dynamic V_G shaping functions which improve the linearity of the amplifier under supply modulation beyond performance with a static supply. This method compensates for variations in the dynamic performance of the amplifier not seen during static characterization. Results using the dynamically-determined gate biases, demonstrate an improvement in both efficiency and linearity.

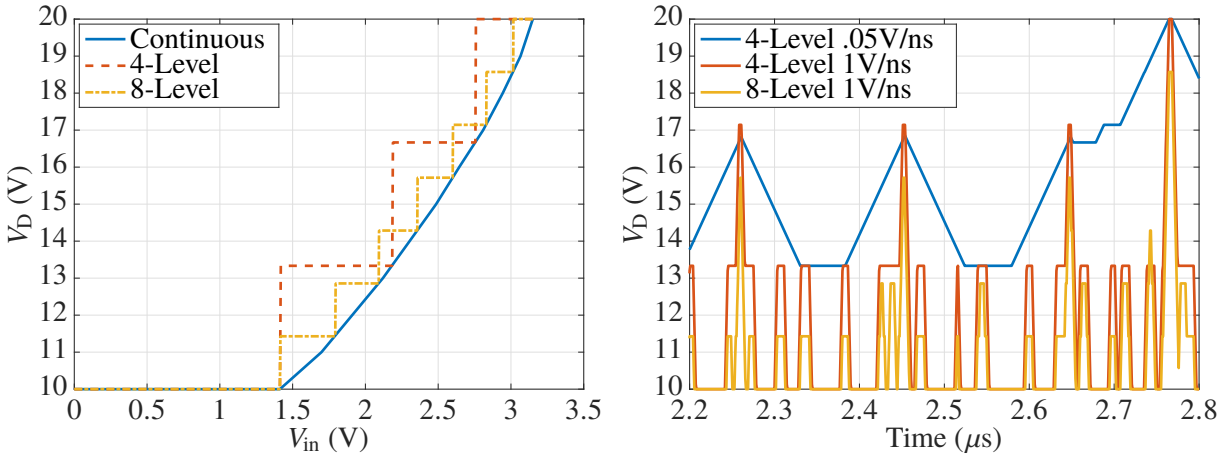


Figure 5.2: (a) Shaping function for X-Band PA with continuous and discrete (4- and 8-level) supply modulation. (b) Ideal time domain drain voltage waveforms for three shaping functions with different slew rates and numbers of levels.

5.1 Initial Testing

5.1.1 Linear Tracker Testing

The linear tracker used is the one described in Section 3.2.1a without the driver stage. In this configuration the power stage of the linear tracker had higher gain, higher output impedance, and lower bandwidth. Noise-like signals typical in satellite communications, discussed in Section 3.3.4, have a high (> 10 dB) PAPR making efficient transmission difficult. For a 250 MHz signal an over 1 GHz supply modulator bandwidth would be required to track down to 50 dBc below the signals main lobe. This high bandwidth requirement can be overcome by using discrete supply modulation.

A shaping function for testing is designed to allow for a flat gain of approximately 20 dB. This is determined by static measurements of the amplifiers performance which are then used to create a input voltage to drain voltage relationship. This continuous relationship is then discretized to be used with the linear tracker. The discretized shaping function is shown in Fig. 5.2a. Testing is done for a variety of slew rates which assume a certain, V_D, rise and fall time during the transitions between levels. Seen in Fig. 5.2b faster slew rates mean better tracking of the continuous supply modulation case.

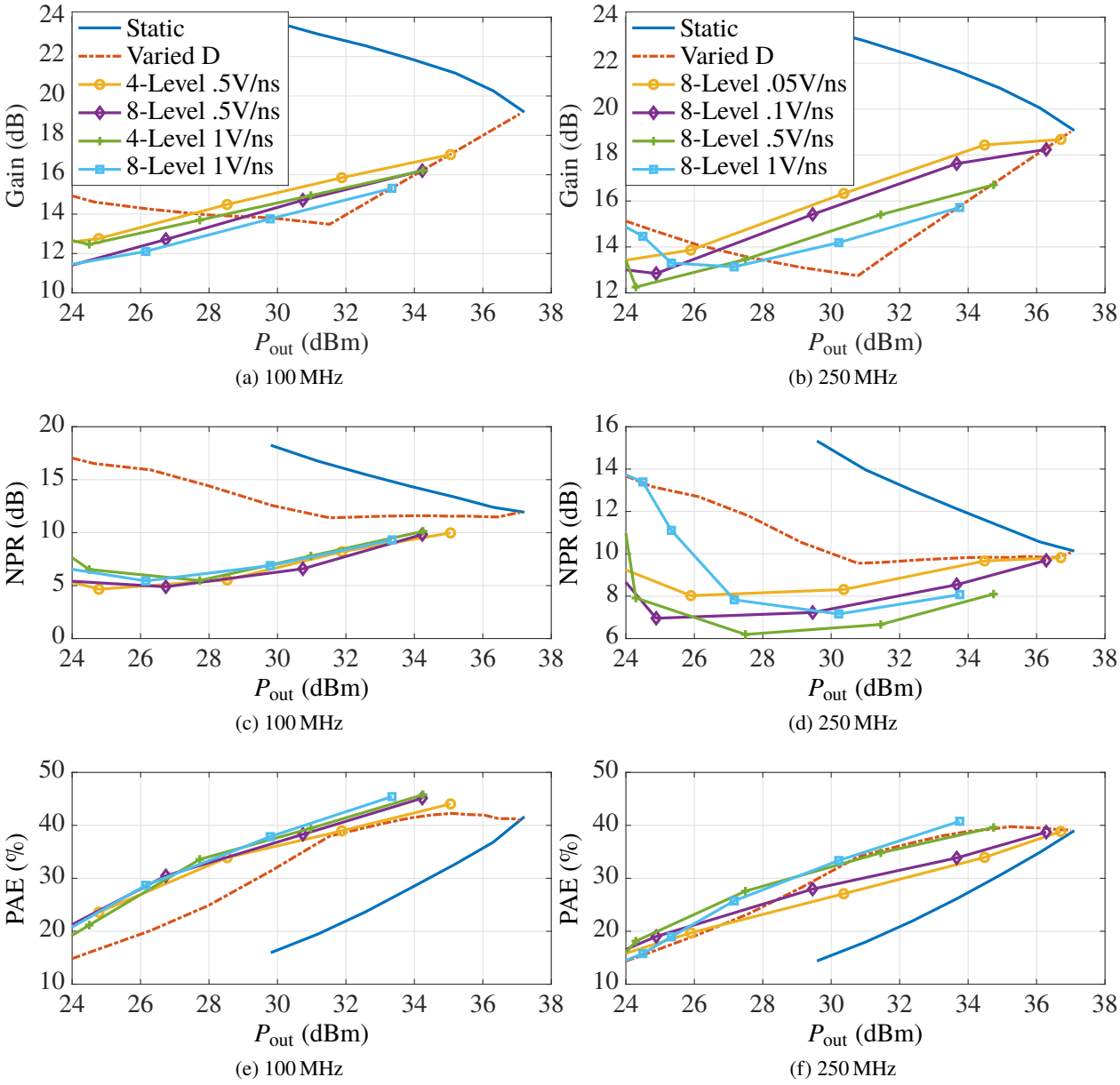


Figure 5.3: Results for a 100 MHz signal showing (a) gain, (c) NPR, and (e) PAE. Results for a 250 MHz signal showing (b) gain, (d) NPR, and (f) PAE.

Table 5.1: Measurement Results B_N=100 MHz

V_D	SR	P_{out} (dBm)	NPR (dB)	PAE (%)	Gain (dB)
20 V	0 V/s	35.2	13.3	32.7	21.2
15 V	0 V/s	35.1	11.6	42.3	17.1
4 Lev.	0.05 V/ns	34.5	11.1	36.3	18.7
8 Lev.	0.05 V/ns	33.6	10.1	35.4	18.4
4 Lev.	0.5 V/ns	35.1	10.0	44.0	17.0
8 Lev.	0.5 V/ns	34.2	9.8	45.1	16.2
4 Lev.	1 V/ns	34.3	10.1	45.8	16.2
8 Lev.	1 V/ns	33.4	9.3	45.4	15.3

Table 5.2: Measurement Results B_N=250 MHz

V_D	SR	P_{out} (dBm)	NPR (dB)	PAE (%)	Gain (dB)
20 V	0 V/s	33.7	12.1	26.2	21.7
14 V	0 V/s	34.0	9.8	38.9	16.0
4 Lev.	0.05 V/ns	35.1	10.0	34.5	18.9
8 Lev.	0.05 V/ns	34.5	9.7	34.0	18.7
4 Lev.	0.5 V/ns	35.4	9.3	39.9	17.3
8 Lev.	0.5 V/ns	34.7	8.1	39.6	16.7
4 Lev.	1 V/ns	34.6	8.2	40.6	16.5
8 Lev.	1 V/ns	33.8	8.1	40.8	15.7

Results for the amplifier and linear tracker can be seen in Fig. 5.3. Efficiency is improved greatly as a results of supply modulation. All supply modulation cases improve efficiency by 15-20 pp over the static supply case. Another test is done in which the envelope of the efficiency for multiple static supplies is looked at. This "Varied D" case shows highest efficiency at a given P_{out} for supply voltages statically swept from 10-20 V. Even in this case, supply modulation exceeds or equals the results all for higher slew rates (>=.5 V/ns).

While these results are good from an efficiency perspective there is a degradation in performance from a linearity perspective. For all cases, supply modulation is worse than both the static supply NPR and the efficiency envelope NPR. Initially the results from Fig. 5.2b led to speculation that the output impedance of the supply modulator circuit, which is on the order of 10 Ω, might be causing some added bias modulation to the amplifier, degrading linearity. The only way to effectively rule the linear tracker out as a distortion

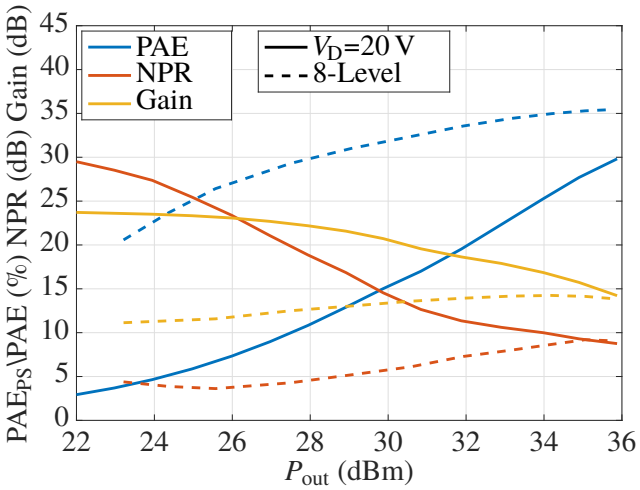


Figure 5.4: 100 MHz results with MMIC discrete supply modulator.

cause is to do testing with an actual DSM which has a lower output impedance, on the order of 1 Ω for the 8-Level DSM.

5.1.2 8-Level DSM Testing

With this in mind further testing is performed using the 8-level discrete supply modulator described in Section 3.2.2c, which should behave in a similar way to the highest slew rate 8-level case for the linear tracker with a lower output impedance (the output impedance of the 8-level tracker will just be be the resistance of the three switches on the MMIC in series). The results in Fig. 5.4 confirm that the testing shown with the linear tracker is accurate. Up until now this method has been aimed at supply modulation of broadband signals. As a result measurements are always performed with signals whose bandwidths exceeded the capture bandwidth of the VSA. To get more insight into what is actually happening in the amplifier testing is done with a more narrowband signal (10 MHz).

The AM/AM and AM/PM results for a 10-20 V drain voltage swing is shown in Fig. 5.5. As can be seen the gain collapses for lower input powers at the lowest drain voltage. This effect is not seen during static (CW) characterization and is only present during dynamic measurements.

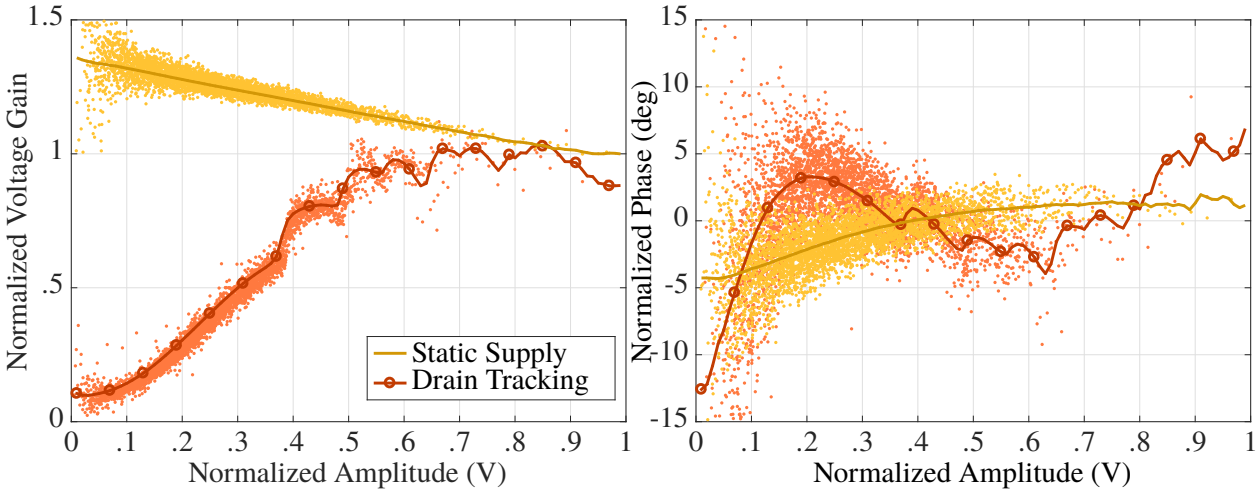


Figure 5.5: Measured results at 9.7 GHz and 28 dBm output power showing (a) AM/AM and (b) AM/PM for a 10-MHz NPR signal with a PAPR=10 dB. yellow shows performance for just a static supply, blue shows gate and drain modulation, and red shows drain modulation. The discrete points are faded and a darker trend line is superimposed for clarity.

5.2 Constant Quiescent Current Mode

To further analyze this problem the amplifier is re-characterized on the VNA test bench described in Section 2.1. The results in Fig. 5.6a show that the amplifier has parametric oscillations that occur for lower drain voltages and drive powers. From this two possible reasons for the variation in performance are surmised one being dynamic "trapping" affects [35] in the amplifier and another being a parametric oscillation. Using static characterization it is also observed that there is large variation in quiescent current as a function of drain voltage .

The quiescent current of an ideal amplifier would remain the same over a range of V_D, provided the transistors are biased in the saturation region In a practical amplifier, the quiescent current can vary greatly over V_D. In drain supply-modulated amplifiers, this effect can lead to an increase in gain variation and a resulting degradation of linearity. Fig. 5.6 shows measured results for the amplifier tested in this work for constant gate voltages, V_{G1} and V_{G2}, and a constant quiescent current, while varying statically the common drain voltage.

For the constant V_G case of Fig. 5.6a, the measured gain varies over 6 dB from 10-20 V. Additionally, there

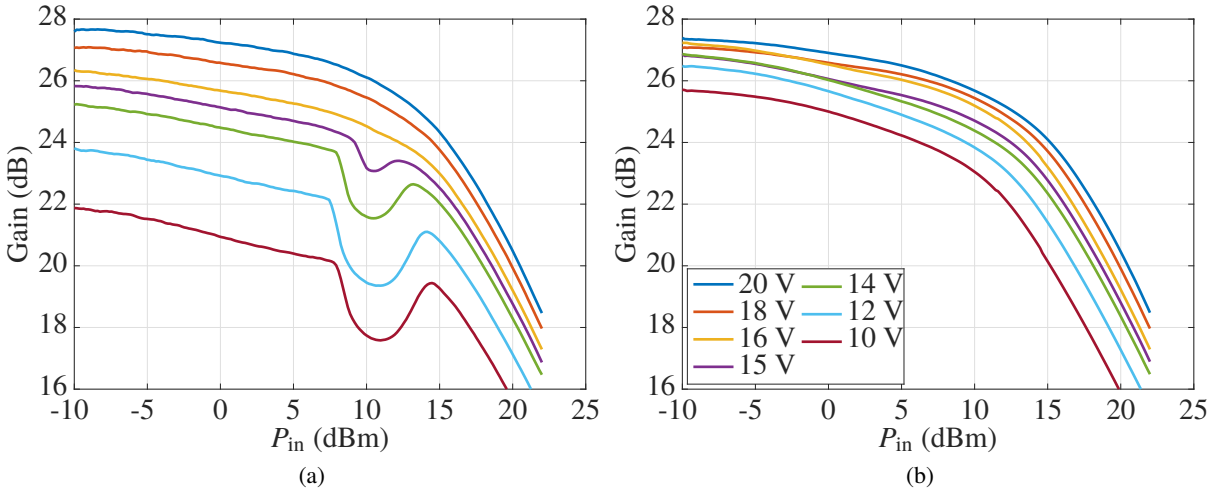


Figure 5.6: Measured gain at 9.7 GHz of the X-Band MMIC PA as a function of input power P_{in} for (a) V_{G1} and V_{G2} static for the quiescent bias at V_D=20 and (b) constant quiescent current, when the single drain supply V_D is varied from 10 to 20 V. Dips in gain during the static gate bias case are indicative of parametric oscillations. These are present for P_{in}={8 − 14}

are gain dips around P_{in}=10 dBm that are indicative of parametric oscillations, which practically limit the amplifier drain modulation range to 16-20 V for linearity. Efficiency measurements show that this limitation in supply voltage range results in a >10 percentage point (pp) impact on efficiency relative to the full range. If the quiescent current of the amplifier is held constant over drain bias by adjusting the gate bias accordingly, seen in Fig. 5.6b, the gain variation are reduced to <2 dB and the parametric oscillations are eliminated.

A static amplifier characterization is performed to define the dependence of drain voltage on input voltage. This drain shaping function is seen in Fig. 5.7a and is designed to maintain a flat gain over drive power. The shaping function is discretized assuming for an 8-level DSM. To compensate for the drain current variation due to the discrete nature of the drain voltage, the gate shaping functions are also discontinuous and shown in Fig. 5.7b. They are designed from static measurements by selecting gate voltages that keep the quiescent current constant. Because the gates of the transistors draw virtually no dc current, this can be done without reducing efficiency. For higher modulation bandwidths there will be some ac current draw on the gates, effecting efficiency.

The application of the shaping functions from Fig. 5.7a-5.7b to a 10 MHz noise-like signal in the time domain can be seen in Fig. 5.7c-5.7d. As the supply voltage reduces on the drain, the gate supply provides

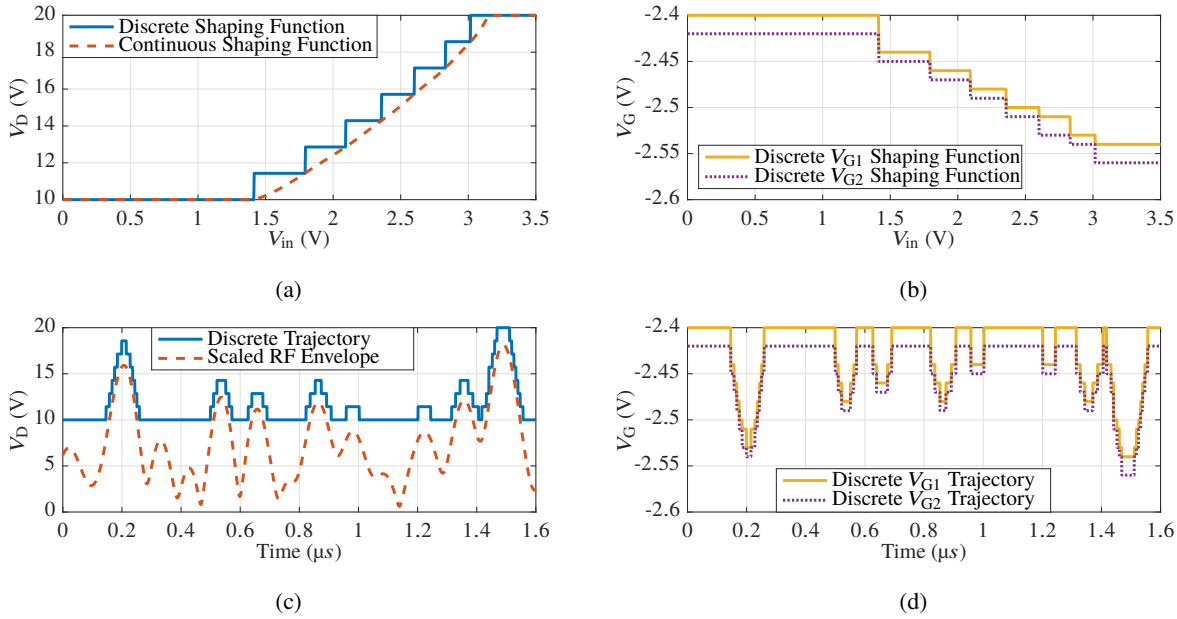


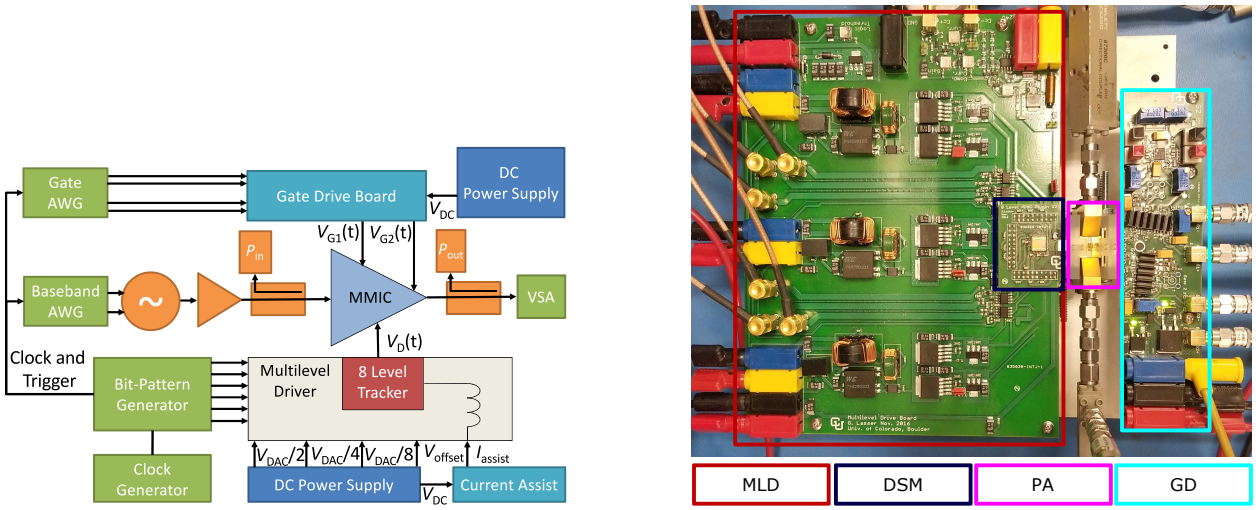
Figure 5.7: (a) Drain shaping function maps the input envelope to the dynamic drain supply voltage, and (b) gate shaping functions for the two stages. V_{in} is calculated from the input power assuming a 50-Ω impedance. Time domain voltage waveforms for a 10 MHz noise-like signal at P_{in}=14 dBm, for (c) the drain voltage and continuous envelope (d) gates 1 and 2.

a more positive voltage, compensating for the quiescent current drop seen for a static supply. The two gate voltages vary synchronously, but to different values due to the different bias voltages needed to maintain a constant quiescent current for the two stages.

5.2.1 Measurement Method and Results

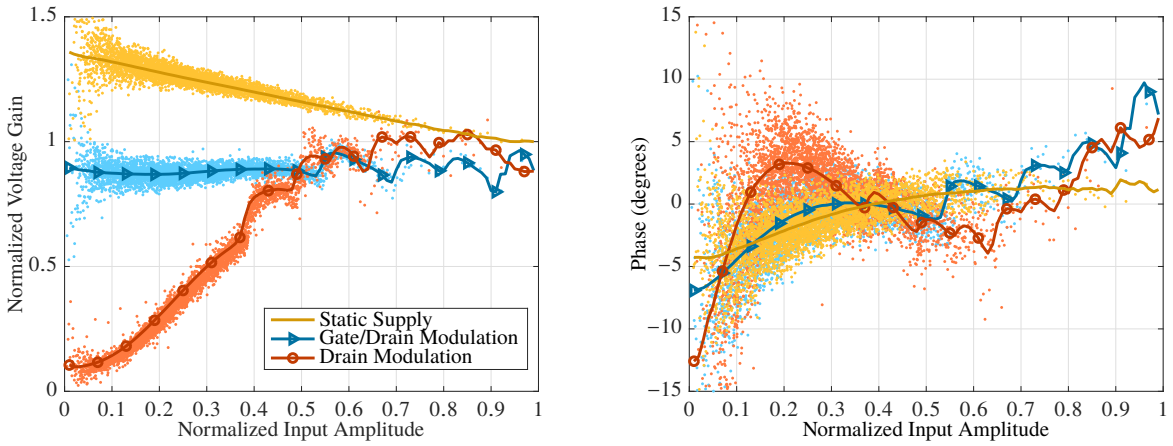
The PA with dynamic drain and gate biasing is characterized with a test setup illustrated in Fig. 5.8. The bench is variant of the one discussed in Section 3.3.2 and is calibrated per the description in Section 3.3. The 8-level DSM described in Section 3.2.2c. An inefficient current assist is used and it's efficiency is not considered in measurements. Testing is done with a 10 MHz noise-like signal. The amplified signal is captured in the frequency and time domains. For time domain data, the signal is received by the VSA, upsampled from the received sampling rate to the generation sampling rate, and then time and phase aligned to the original signal.

Fig. 5.10a shows results for a power sweep for three cases: static supply, drain modulation (DM), and



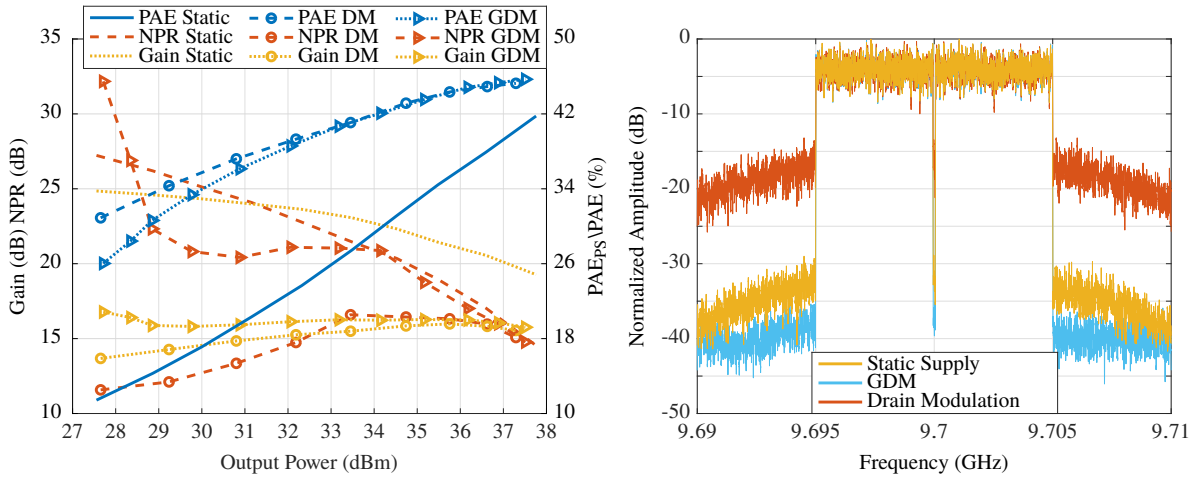
(a) (b)

Figure 5.8: (a) Block diagram of test setup. Gates 1 and 2 are varied independently. The dynamic drain voltage is provided by an 8-level tracker controlled by a BPG that commutates three external voltages, $\frac{V_{SW}}{2}$, $\frac{V_{SW}}{4}$, $\frac{V_{SW}}{8}$, while the dynamic gate signals are provided synchronously by the AWG. An external current assist circuit sources current for the 8-level tracker. (b) Photo of test setup, left hand side shows multilevel drive board, right hand side show gate drive board. Between the two is the CuMo mounted MMIC.



(a) (b)

Figure 5.9: Measured results at 9.7 GHz and 28 dBm output power showing (a) AM/AM and (b) AM/PM for a 10-MHz NPR signal with a PAPR=10 dB. yellow shows performance for just a static supply, blue shows gate and drain modulation, and red shows drain modulation. The discrete points are faded and a darker trend line is superimposed for clarity.



(a) (b)

Figure 5.10: (a) Measured results for the transmitter under static bias, with drain modulation (DM), and with both gate and drain modulation (GDM). PAE values include power stage losses of the supply modulator. (b) Measured spectrum of a 10 MHz noise-like signal at 28 dBm output power for static supply (yellow), gate and drain modulation (blue) and drain modulation (red).

gate and drain modulation (GDM). While GM and GDM show similar PAE improvements over the static supply case, the NPR penalty is very different. The GDM consistently outperforms DM in NPR by over 20 dB at P_{out}=28 dBm and over 10 dB up to P_{out}=34 dBm. For output powers exceeding 34 dBm, GDM is equal to or outperforms the static supply in terms of NPR, while improving PAE between 5 pp and 12 pp. Using GDM reduces efficiency in back-off by <5 pp compared to DM, as a higher gate voltage will increase current draw at lower power levels, however the efficiency degradation disappears at higher drive levels.

AM/AM and AM/PM data for the three cases of the static supply, DM, and GDM can be seen in Fig. 5.9. The steep drop in gain at lower drive levels is a is discussed in Section 2.2, and it is seen that GDM prevents this gain decrease which is pronounced with DM. Additionally, there is a tighter spread on the AM/PM at lower input amplitudes for the GDM case compared to DM. Compared to the static supply case, the GDM AM/AM is more linear. Measured spectra for the static supply, DM, and GDM cases are given in Fig. 5.10b. At P_{out}=28 dBm GDM provides the best linearity, even exceeding that of the static supply case, with a substantial, 20 dB, improvement over DM alone.

While drain modulation improves efficiency, as expected for supply modulated PAs, the linearity characterized by NPR is degraded. If an NPR >16dB is desired, the distortion for drain modulation only renders the

Table 5.3: Bias parameters at $V_D = 20\,V$

Values	V_{G1}, V	V_{G2}, V	I_{D1}, mA	I_{D2}, mA
min	-3	-3.05	1.1	2.3
max	-2.4	-2.45	101	454.9
nom	-2.64	-2.67	60	250

PA practically useless, since backing-off the power degrades performance further. Adding gate modulation improves the NPR to levels of over 20 dB for output power levels up to 34 dB with a marginal PAE penalty. This is enabled by modulating the gate biases of the driver and output stage of the PA independently. In this case, the PAE is improved by 15 percentage points from 18 to 33% at P_{out}=30 dBm and by 5 percentage points as peak power is approached, while maintaining linearity.

5.3 Gate Modulation Characterization

A static characterization of the amplifier, similar to the one done in Section 2.1, is performed to see trends important for linearization during gate modulation [77, 78]. The static bias parameters are given in Table 5.3 and the measured data at 9.8 GHz plotted in Fig. 5.11a and Fig. 5.11b, respectively. The "Static Bias" trace shows the behavior of the PA for nominal, static bias. The initial gain at P_{out}=20 dBm is 28.0 dB, and gradually drops to 23.7 dB as the PA is driven into compression at P_{out}=40 dBm. In the same range, the transfer phase of the PA has an S-shape, starting at -186 deg, peaking at P_{out}=37.8 dBm with -174 deg and finally reaching -177 deg at 10 W output, with a total span of 10 deg.

The gray shaded area corresponds to the observed range in terms of PA transfer gain and phase, when independently varying the gate voltages. We see that at an output power of 20 dBm the gain of the PA varies between 13.6 dB to 29.4 dB, and the phase can be varied in a 85 deg range. At P_{out}=40 dBm, the gain range reduces to 20.5 dB to 25.2 dB, and the phase range drops to 35 deg. However, not all combinations of gain and phase settings are possible. To illustrate this, the bounds of the phase range corresponding to gate settings producing 24 dB of gain are plotted A dashed lines in Fig. 5.11b. The phase range that allows for flat gain and phase over the full measured amplitude range is examined for three cases shown by colored

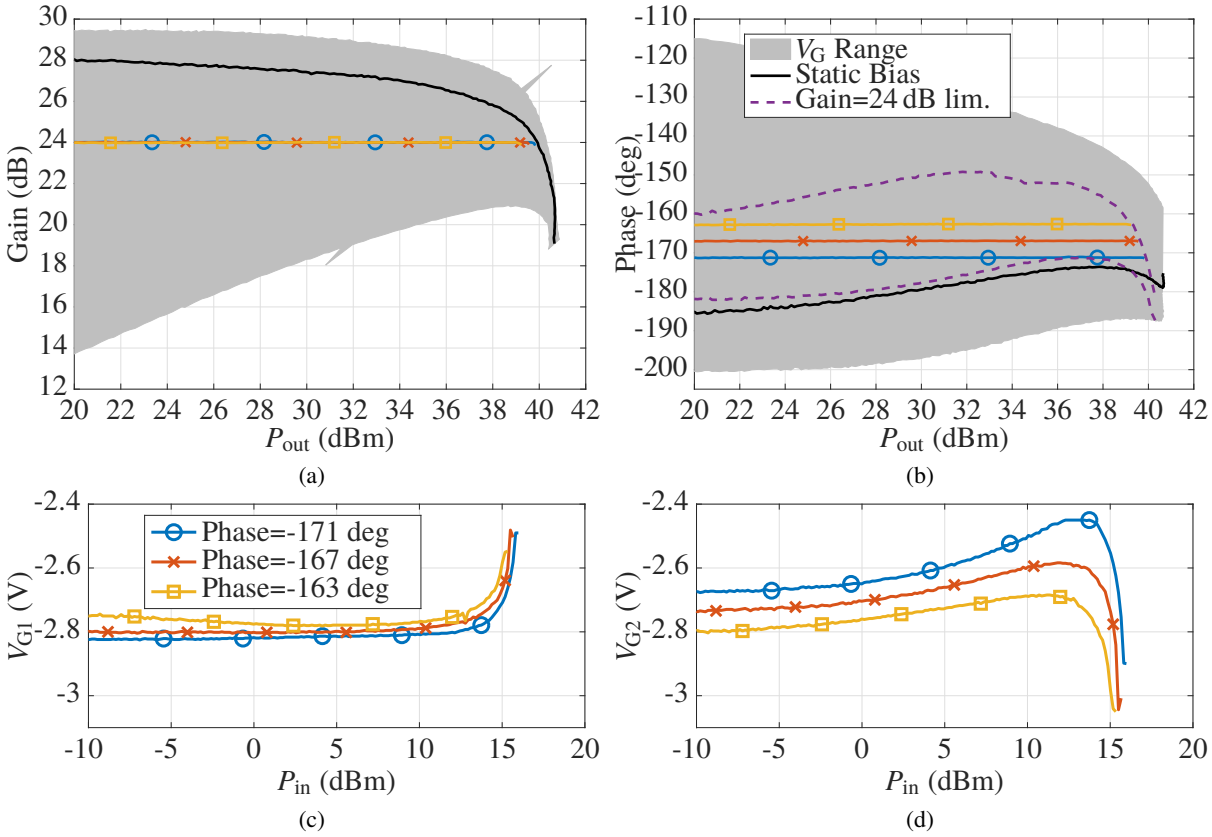


Figure 5.11: Static gain (a) and transfer phase (b) characterization of a 2-stage GaN MMIC PA. The grey area shows the obtainable gain (a) and phase (b) range when the gates are swept according to Table 5.3. The dark solid line corresponds to the conventional static bias, the colored lines show the resulting gain and phase for three dynamic bias cases with 24 dB of gain. Gate 1 (c) and gate 2 (c) tracking functions for the three flat amplitude and phase trajectories providing 24 dB of gain and the indicated phase value.

traces in Fig. 5.11a and Fig. 5.11b, with nominal phases of -163 deg, -167 deg, and -171 deg. The required gate tracking functions for these cases are plotted in Fig. 5.11c-5.11d. From this example, we observe:

- Two independently controllable gate voltages provide two degrees of freedom and enable linearization of amplitude and phase;
- The output power range for complete linearization is limited;
- For the same gain, different phase settings result in slightly different output power ranges and efficiencies.

To explain the last point, inspecting Fig. 5.11d shows that for different phase settings, similar but shifted

gate 2 trajectories are required. This is true for gate 1 (Fig. 5.11c), but to a lesser degree. Since stage 2 uses larger transistors (3. mm for stage 2 vs. 0.8 mm in stage 1), and the gate voltage difference is larger, the voltage shift in the gate 2 tracking functions dominates the total current consumption and thus efficiency. The -163 deg case therefore provides the best efficiency of the three investigated 24 dB cases, but a slightly smaller peak output power.

This static analysis is used in [79] to determine a shaping function for linearization of the X-Band PA with a static drain supply. It is found that the statically determined shaping function did not effectively predict the performance of the amplifier under dynamic operation. To overcome this an optimization routine based on dynamic measurements is used. By this technique an improvement in linearity and efficiency is realized over a static supply.

5.4 Optimized Gate Shaping Function

Static determination of the amplifiers V_{G1} and V_{G2} levels resulted in a shaping function that improves linearity without reducing efficiency [76]. The statically determined shaping function, though better than a static gate supply, only improved linearity for select values of P_{out}. The analysis in Section 5.3 indicates the possibility of improving linearity over all power levels through a power-dependent shaping function.

5.4.1 Gate Shaping Function Optimization

The discrete gate levels are determined by dynamic measurements, necessary to compensate for the different thermal and trapping states of the PA due to different supply regimes (static vs. dynamic). On average, the temperature of the MMIC PA with a static supply is higher because of the lower average efficiency in this regime. With a dynamic supply, the variation in gain caused by supply voltage variation is compensated by the gate biases.

A shortened test signal, with a probability density function (PDF) and PAPR similar to a noise-like signal, is used for the optimization routine. During the measurement sequence, the signal is repeated for each optimizer variation while a windowing is applied at the beginning and end of the signal to make it cyclic

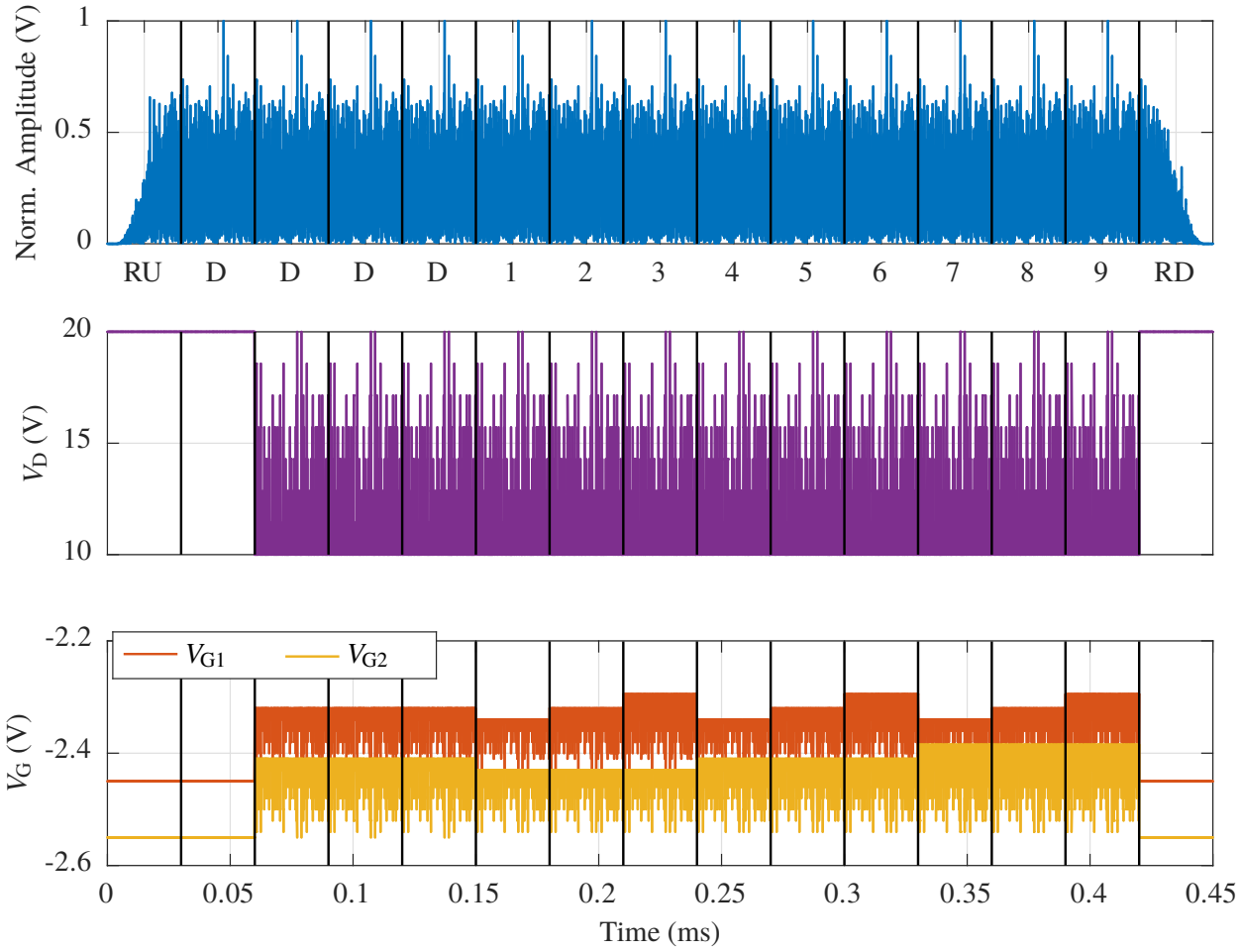


Figure 5.12: Example optimization signal for a 20 MHz signal at P_{in}=15 dBm optimizing the level 1 gate voltages. In this case the same signal is repeated fifteen times. A ramp up (RU) and ramp down (RD) are used to align the received data in post processing. Four dummy sequences (D) are used, one under static operation and three under dynamic operation to set the thermal state of the amplifier. Nine combinations (1 – 9) of gate 1 and gate 2 voltages are tested and then analyzed in post processing.

and easy to align, seen in Fig. 5.12.

The optimization begins with statically determined gate voltages for each drain voltage (V_D) level and optimizes the gate voltages ($V_{G1,2}$) for a new shaping function at every input power (P_{in}), as illustrated with the flowchart in Fig. 5.13. The optimizer steps through each V_D level and varies V_{G1} and V_{G2} simultaneously and independently. Ten voltages for each gate (V_{G1} and V_{G2}) are simultaneously varied resulting in 100

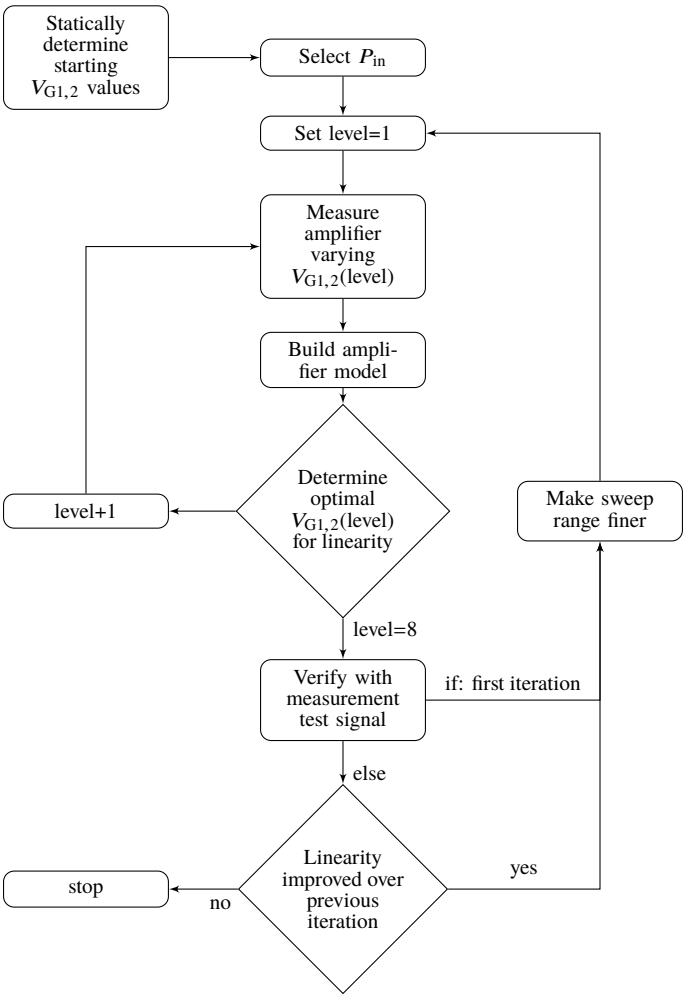


Figure 5.13: Optimization routine used to find the ideal gate voltages ($V_{G1,2}$) for each drain voltage (V_D) level. The optimization is performed for each input power level (P_{in}).

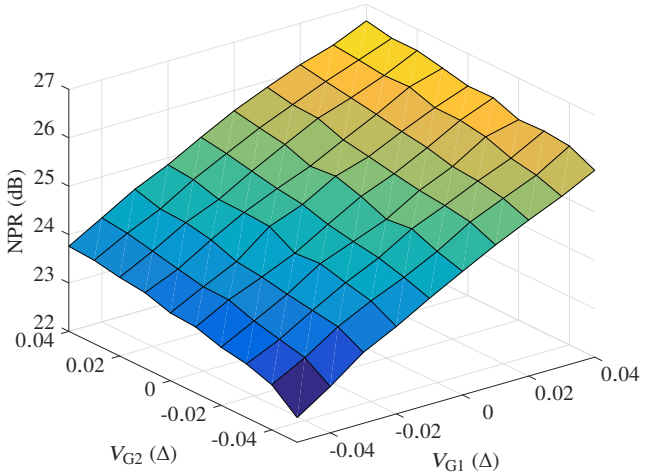


Figure 5.14: Optimization results varying gate voltages for the level 2 drain voltage level at P_{in}=13 dBm.

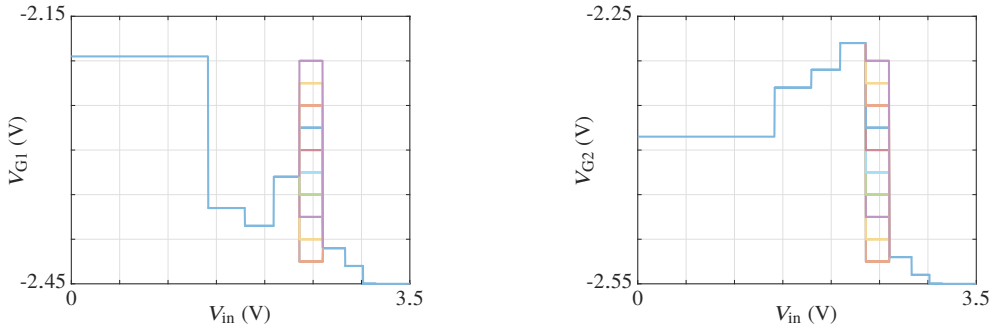


Figure 5.15: (a) V_{G1} and (b) V_{G2} shaping function during optimization for level 5 of V_D. Levels 1-4 have already been optimized in this example

total combinations per measurement. This data is measured using the VSA and the signal is time and phase aligned and then cut into 100 individual sections, one for each combination. A trendline is then produced for the AM/AM and AM/PM variation of each section, and used to create a memory-less look-up table model of the amplifier's performance. A 20 MHz notched noise-like signal is then interpolated with the trendline gain and phase variation for each of the 100 gate voltage variations gathered in the single measurement. The linearity metric of interest in this work is the Noise Power Ratio (NPR), which is estimated for each V_G. The gate voltages ($V_{G1,2}$) providing the maximum modelled NPR are then selected for this level, as seen in Fig. 5.14.

After this is completed, the algorithm iterates to the next drain voltage level and the gate voltages are varied to find the optimum NPR point. This process, seen in Fig. 5.15 for the level = 5 optimization step, is repeated for all V_D levels and then the optimized $V_{G1,2}$ shaping function is used for testing with the full measurement test signal. If the shaping function results in improved linearity as compared to a static supply, then the optimization is complete. If the shaping function is insufficient, the sweep range of the $V_{G1,2}$ is made finer (step size reduced from 0.025 V to .01 V) and the optimization continues, as seen visually in Fig. 5.13.

5.4.2 Optimization Model Validation

The model performance is first confirmed by varying the whole shaping function for V_{G1} and V_{G2}, rather than changing the levels individually, as shown in Fig. 5.16. To validate the approach used, the amplifier is modeled

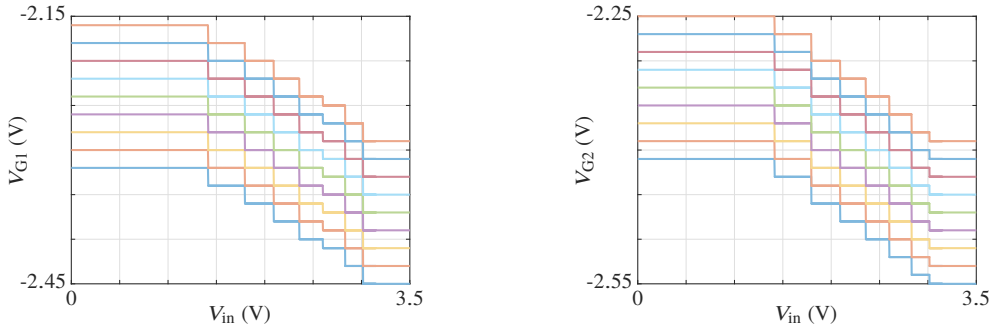


Figure 5.16: (a) V_{G1} and (b) V_{G2} shaping function variations for testing NPR model used in optimization.

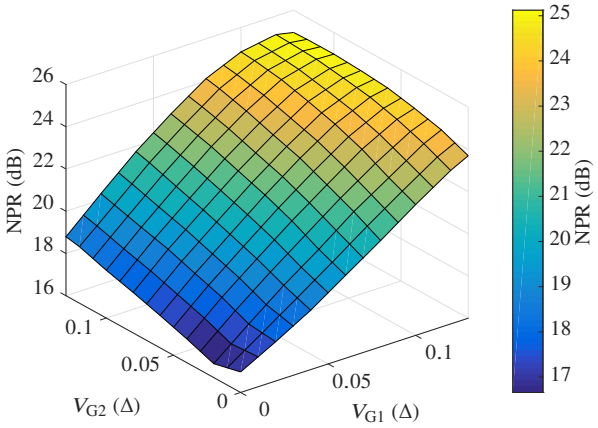


Figure 5.17: Modelled NPR for 196 variations of V_{G1} and V_{G2} gathered from a single measurement.

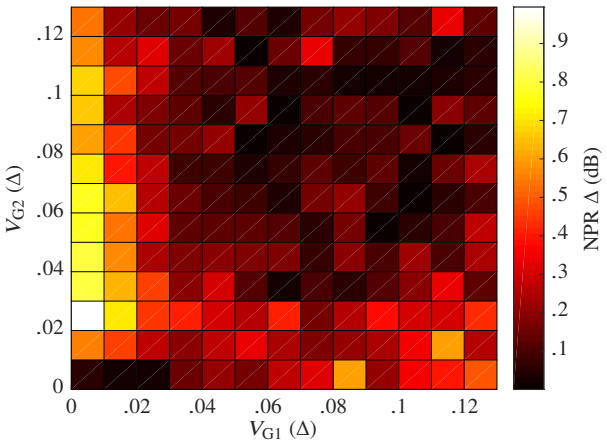
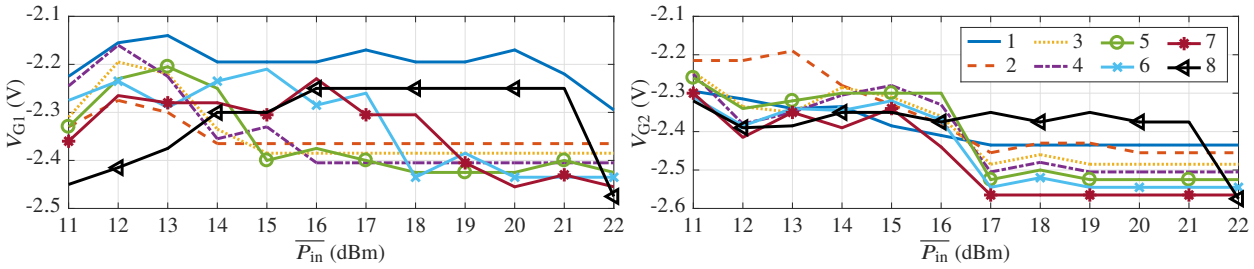


Figure 5.18: Comparison between modelled result from a single measurement and results from 196 individual measurements. Absolute variation between the two is less than 1 dB.

using the optimization test signal (results seen in Fig. 5.17), and then longer individual measurements are performed at each data point with the 10 MHz measurement test signal transmitted through the amplifier. The difference between the measured NPR with the measurement test signal and modelled NPR with the optimization test signal can be seen Fig. 5.18, where the color represents the absolute difference in dB between the two. The model differs by less than 1 dB across the measured values indicating good agreement. This approach allows quick measurements enabling efficient on-the-fly optimization of the individual gate voltage values.



(a) (b)

Figure 5.19: (a) V_{G1} and (b) V_{G2} final shaping functions for each P_{in} level. 1 corresponds to the lowest V_D level and 8 to the highest. As input power increases the $V_{G1,2}$ tend to become more negative. The exceptions to this are levels 1 and 8 for V_{G1} and level 8 for V_{G2}.

5.4.3 Results

Measurements are done with and without the 87 % efficient CA circuit. Efficiency is shown assuming a perfect (100 % efficient) and the real CA circuit. The dynamic V_G shaping functions are developed with the CA active, and performs better with the CA than without it. The current assist circuit as well as its effect on current draw are discussed in depth in Section 3.2.2d

The measurement test signal has a similar PAPR and PDF as the optimization test signal used for modeling the amplifier in the optimization procedure. For the 10 MHz signal noise-like signals, with NPR as the linearity metric are looked at. For the 20 MHz case both LTE and noise-like signals are looked at with ACPR and NPR as the respective linearity metrics.

For dynamic measurements the input power to the amplifier is varied from P_{in}=11-22 dBm. The gate shaping functions, unique for each drive power level, are shown for one case in Fig. 5.19, where 1 corresponds to the lowest V_D level and 8 to the highest. The same drain shaping function is used for the different P_{in} levels but the shaping function is updated to reflected the change in V_{in} at higher drive power levels. For drain-modulated measurements with static gate, the PA is biased at the quiescent point for a 20 V supply. Characterization with a static supply is performed over P_{out} for comparison with the dynamic case.

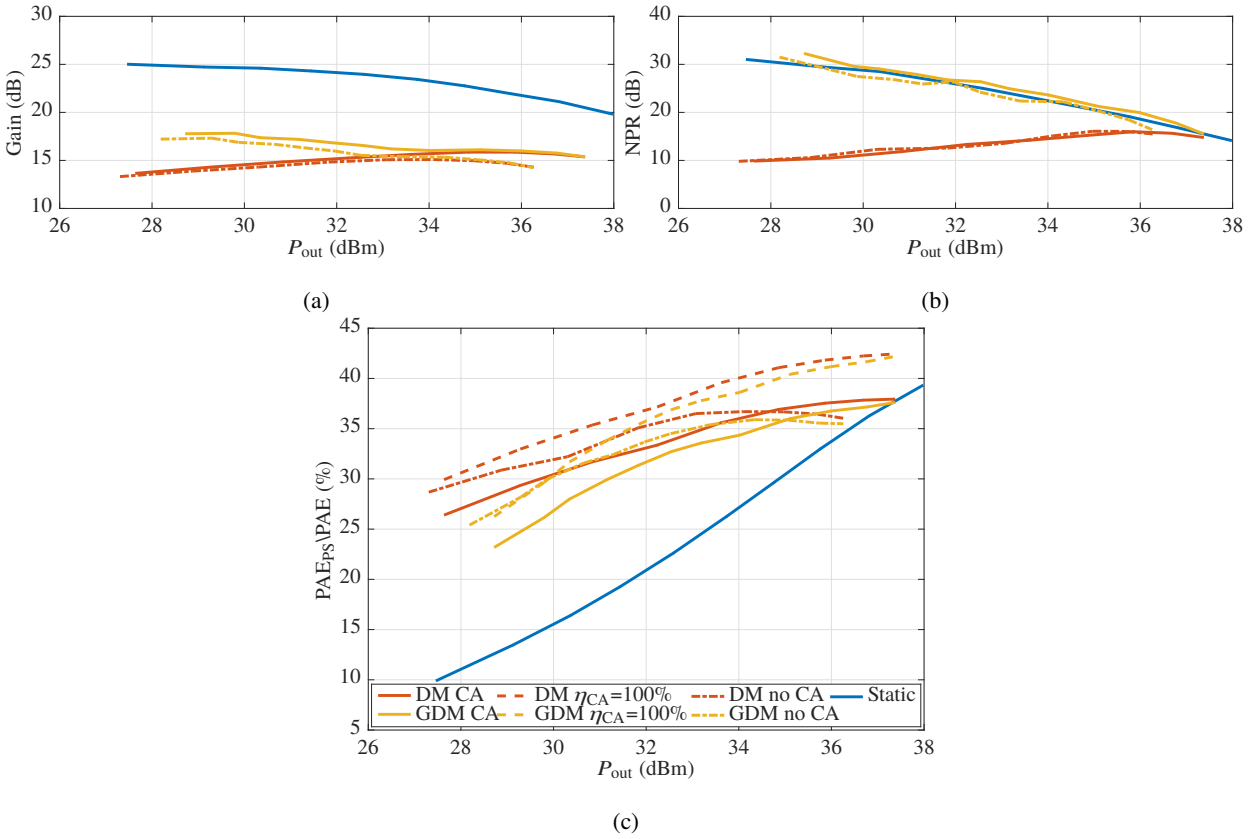


Figure 5.20: Power sweep measurement results for X-Band PA with a static supply, gate and drain modulation (GDM), and drain modulation (DM). Results are shown at 9.7 GHz for a 10 MHz noise-like signal. For the dynamic supply cases, results with and without the current assist circuit are shown. (a) Gain (b) NPR (c) PAE.

5.4.3A 10 MHz Results

Fig. 5.20 shows results of a power sweep for three cases: static supply, drain modulation (DM), and gate and drain modulation (GDM). DM and GDM modulation show similar improvements over the static supply case with PAE. The gain difference between the two is as much as 4 dB in backoff, with GDM outperforming DM, but the two converge at higher drive levels. Using the optimization routine developed in this work, GDM outperforms a static supply in all cases for linearity. At $P_{out} = 28$ dBm there is an over 20 dB improvement in NPR for GDM versus DM. GDM always outperforms DM with the difference between the two decreased as P_{out} increases. The PAE improvements seen with GDM and DM can be further increased at higher drive levels $P_{out} > 35$ dBm with the CA circuit. Improving the CA efficiency would result in a 3-5 pp improvement

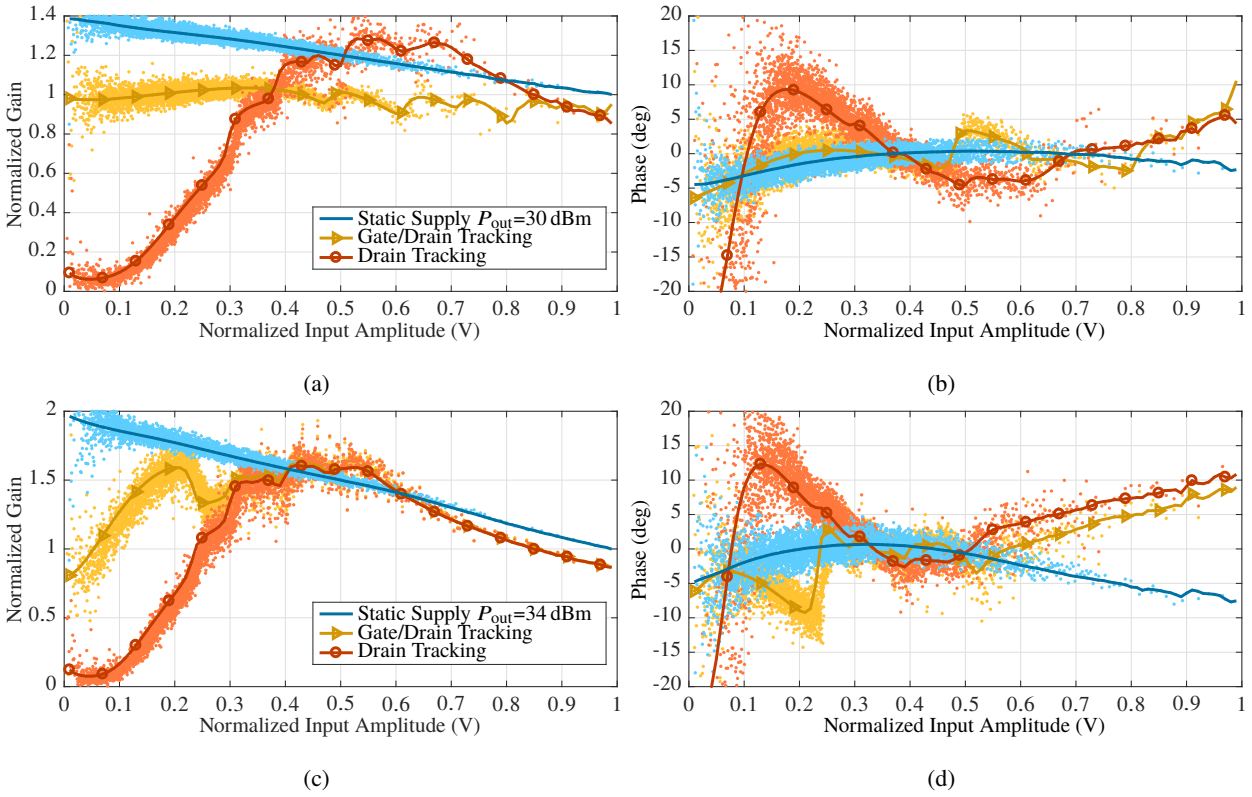


Figure 5.21: Measured results at 9.7 GHz for a 10 MHz noise-like signal with a PAPR=10 dB: P_{out}=30 dBm (a) AM/AM and (b) AM/PM, P_{out}=34 dBm (c) AM/AM and (d) AM/PM. Blue shows performance for just a static supply, yellow shows gate and drain modulation, and red shows drain modulation. The measured data points are faded and a darker trend line is superimposed for clarity.

over the current CA performance, while also affording GDM and DM an efficiency improvement for higher P_{out} levels.

AM/AM and AM/PM data for the three cases of the static supply, DM, and GDM can be seen in Fig. 5.21. The steep drop in gain at lower drive levels is a known phenomenon in GaN [35], pronounced with DM, but it is seen that GDM prevents this gain decrease. Additionally, the AM/PM at lower input amplitudes for the GDM case varies less compared to DM. Compared to the static supply case, the GDM AM/AM is more linear. At higher compression, the AM/AM is not corrected, however the phase (AM/PM) becomes more linear, as seen in Fig. 5.21 for $P_{out} = 34$ dBm. Measured spectra for the static supply, DM, and GDM cases are given in Fig. 5.22. At $P_{out} = 30$ dBm GDM provides the best linearity, even exceeding that of the static supply case, with a substantial 20 dB improvement over DM alone.

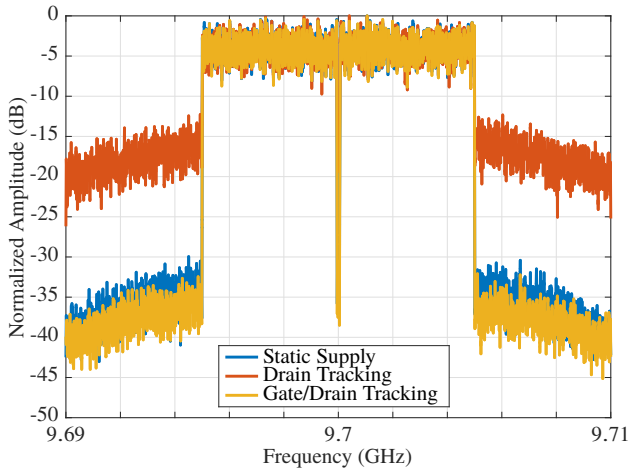


Figure 5.22: Measured spectra of a 10 MHz noise-like signal at $P_{\text{out}} = 30$ dBm for static supply (blue), drain modulation (red), and gate and drain modulation (yellow).

5.4.3B 20 MHz Results

Fig. 5.23 shows results of a power sweep for three cases: static supply, drain modulation (DM), and gate and drain modulation (GDM). DM and GDM modulation show similar PAE improvements over the static supply case. The gain difference between the two is as much as 4 dB in backoff, with GDM outperforming DM, but the two converge at higher drive levels. Using the optimization routine developed in this work, GDM outperforms a static supply in all cases for linearity. At $P_{\text{out}} = 28$ dBm there is an over 20 dB improvement in NPR for GDM versus DM. GDM always outperforms DM but less so as the amplifier saturates.. The PAE improvements seen with GDM and DM can be further increased at higher drive levels $P_{\text{out}} > 35$ dBm with the CA circuit. A higher CA efficiency would result in a 3-5 pp improvement in composite efficiency.

AM/AM and AM/PM data for the three cases can be seen in Fig. 5.24. The steep drop in gain at lower drive levels is a known phenomenon in GaN [35], pronounced with DM, but it is seen that GDM prevents this gain decrease. Additionally, the AM/PM at lower input amplitudes for the GDM case varies less compared to DM. When compared to the static supply case, the GDM AM/AM is more linear. Some spurious points can be seen for the normalized amplitude between 0.3 and 0.4 on the AM/AM curve. This spreading is caused by ambiguity of the voltage states for high switching speeds. To prevent waveform clipping while accounting for switching speed, a higher supply voltage might overlap with an area of operation that lower

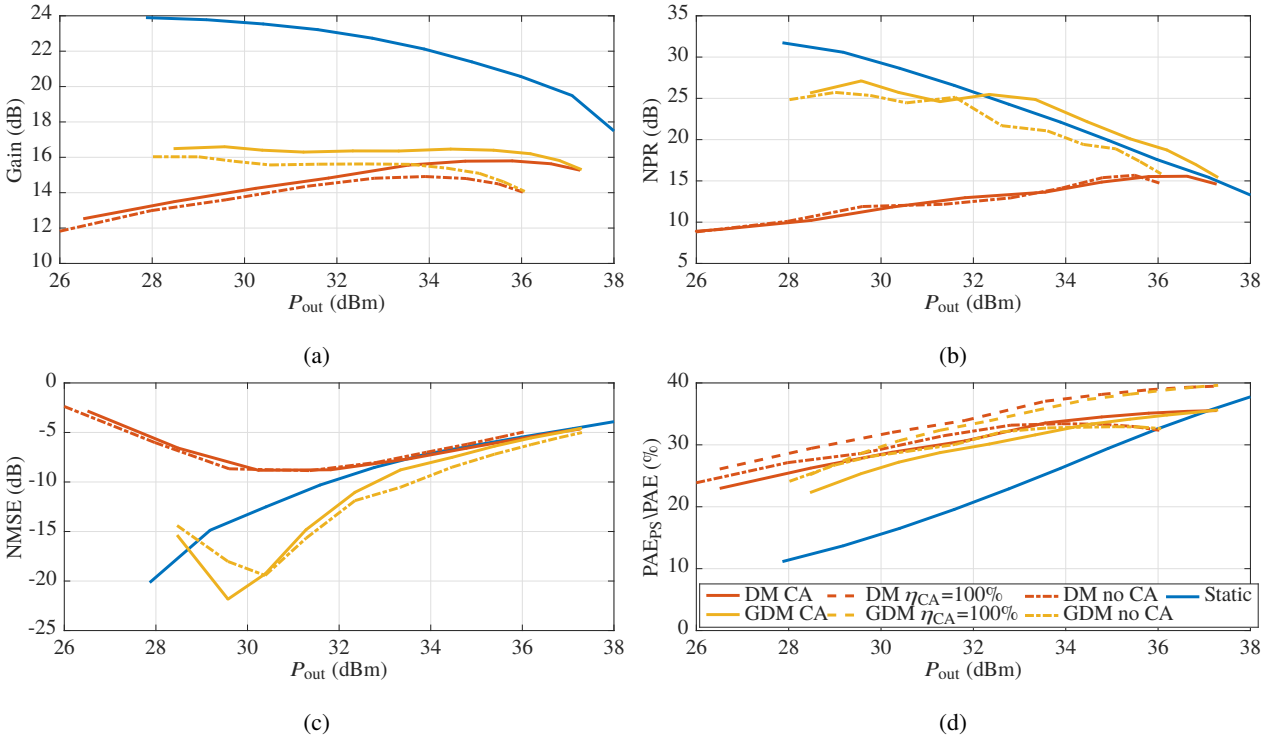


Figure 5.23: Power sweep measurement results for X-Band PA with a static supply, gate and drain modulation (GDM), and drain modulation (DM). Results shown for a 20 MHz noise-like signal. For the dynamic supply cases, results with and without the current assist circuit are shown. (a) Gain (b) NPR (c) NMSE (d) PAE.

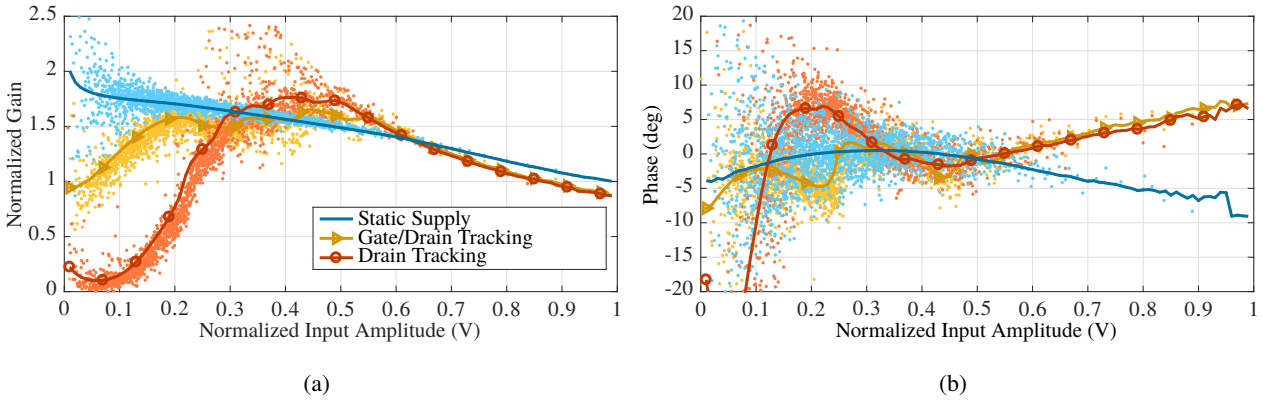


Figure 5.24: Measured results at 9.7 GHz for a 20 MHz noise-like signal signal with a PAPR=10 dB: P_{out}=33 dBm (a) AM/AM and (b) AM/PM. Blue shows performance for just a static supply, yellow shows gate and drain modulation, and red shows drain modulation. The measured data points are faded and a darker trend line is superimposed for clarity.

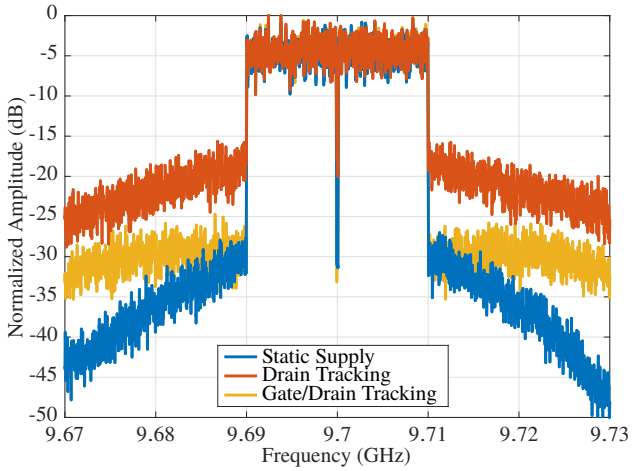


Figure 5.25: Measured spectra of a 20 MHz noise-like signal at $P_{\text{out}} = 33$ dBm for static supply (blue), drain modulation (red), and gate and drain modulation (yellow).

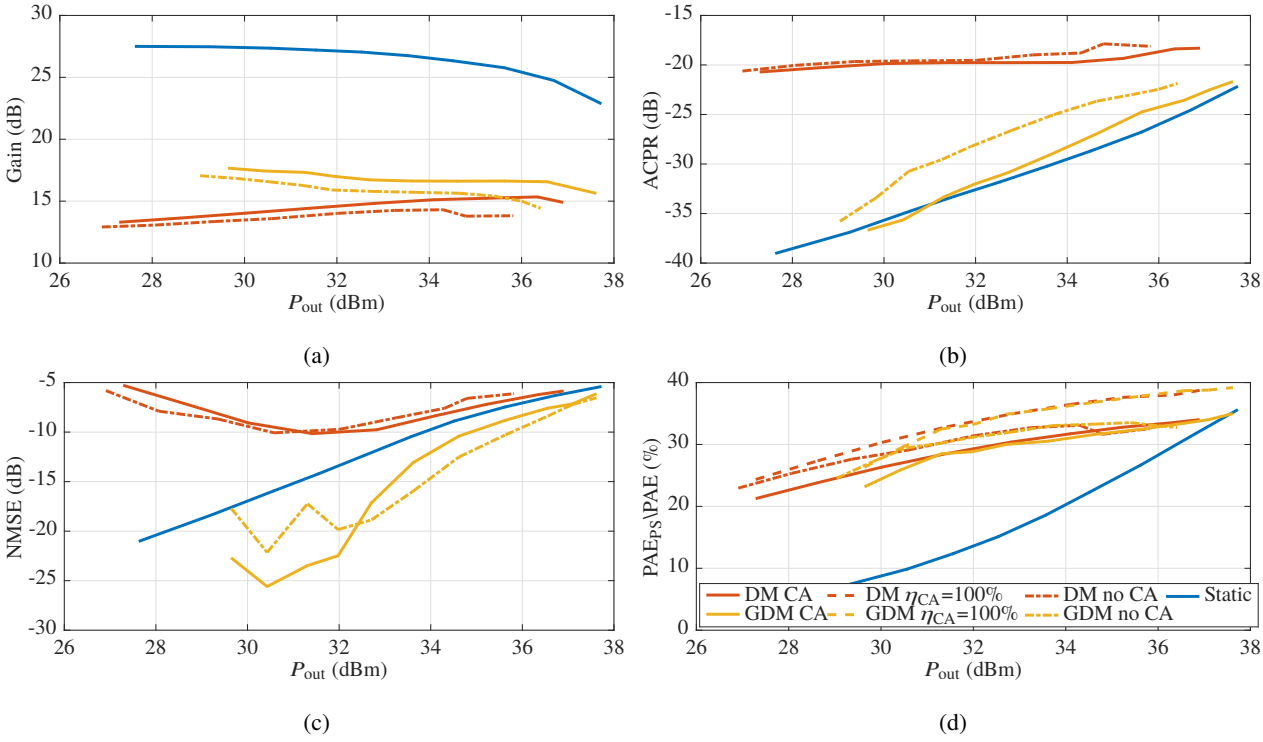


Figure 5.26: Power sweep measurement results for X-Band PA with a static supply, gate and drain modulation (GDM), and drain modulation (DM). Results shown for 20 MHz LTE Signal. For the dynamic supply cases, results with and without the current assist circuit are shown. (a) Gain (b) ACPR (c) NMSE (d) PAE.

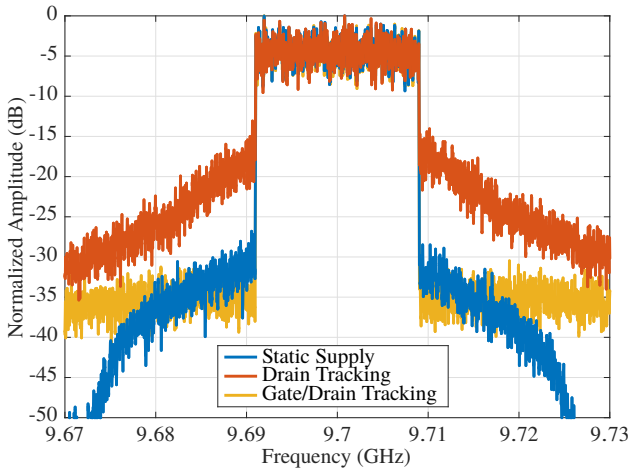


Figure 5.27: Measured spectra of a 20 MHz LTE at $P_{out} = 30$ dBm for static supply (blue), drain modulation (red), and gate and drain modulation (yellow).

voltage would normally cover. Measured spectra for the static supply, DM, and GDM cases are given in Fig. 5.25.

Using the same methods described in Section 5.4.1 testing is also performed for a 20 MHz LTE Signal. A new optimization test signal, with a PDF and PAPR similar to that of an LTE signal is used, with a lower PAPR than the noise-like signal by 1.5 dB. The DM and GDM modulation show similar improvements over the static supply case with PAE. The repeated optimization test signal now has a 20 MHz bandwidth as well to reflect the bandwidth of the LTE signal. During the modeling stage of the optimization routine, ACPR is used as the optimization metric in this case. As seen in Fig. 5.26 the same improvement in normalized mean square error (NMSE), PAE, and gain is realized for the LTE signal. ACPR is improved to near the level of a static supply for the GDM case while DM does not results in good ACPR performance. The spectrum of the LTE signal for the three cases can be seen in Fig. 5.27.

5.5 Conclusion

In this chapter, an efficient two-stage 10 W X-band GaN MMIC amplifier is characterized under both drain and gate modulation, with demonstrated improvement in efficiency and linearity. While drain modulation improves efficiency, as expected for supply modulated PAs, the linearity characterized by NPR is degraded.

If an NPR >16dB is desired, the distortion for drain modulation only renders the PA practically useless, since backing-off the power degrades performance further. Adding gate modulation improves the NPR to levels of over 20 dB for output power levels up to 34 dB with a marginal PAE penalty. This is enabled by modulating the gate biases of the driver and output stage of the PA independently.

The initial gate shaping functions are designed from static conditions, and showed an improvement in PAE by 15 percentage points from 18 to 33 % at $P_{\text{out}} = 30$ dBm, however linearity improvements are limited [76]. Here we show that power-dependent shaping function design for the two-stage gate bias voltages results in both efficiency and linearity improvements, as compared to a static supply. The efficiency improves by 10-15 pp while the NPR is improved for all instances. In addition to applying dynamic gate shaping functions, a current-assist circuit is introduced and tested, showing a path to improved efficiency enhancement of a supply modulator, here demonstrated with an 8-level efficient discrete supply.

The details presented in this chapter are contained in publication [22, 76–79, 103].

Chapter 6

A Three Stage 18.5 24 GHz GaN on SiC 4 W 40 % Efficient MMIC PA

Contents

Here we demonstrate a three-stage reactively matched K-band GaN MMIC amplifier fabricated in the Qorvo 150-nm 28 V process. The design maximizes efficiency, with PAE exceeding 40 %, while reaching a target peak output power of 4 W and peak saturated gain of 25 dB. The output power exceeds 3.2 W with over 20 dB gain for the 18.5-24 GHz frequency range. Performance and design criteria are evaluated for a drain supply voltage range of 10-28 V, with a nominal bias point of 100 mA/mm for a drain voltage of 20 V.

The chapter presents the design flow, starting with transistor sizing and network design, and a statistical analysis of 230 on-wafer probed amplifier chips. Discussed are process considerations focusing on the

performance of the final stage transistor over supply voltage and frequency, matching network synthesis for a non-isolated reactive combiner and details the design approach for the amplifier, including stabilization, and probed performance of the amplifier and shows a statistical analysis of measured large signal data over 5 wafers. Finally connectorized measured PA performance is presented.

Table 6.1: Comparison of K-Band GaN Amplifiers

Freq. (GHz)	Frac. BW (%)	P_{out} (dBm)	PAE (%)	Gain (dB)	Year Ref.
26	-	33.5	42	8	2017 [104]
17-20	16	29.7	36	4	2017 [105]
21-23	9.1	37	48	16.7	2012 [106]
18-20	10.5	31	22	16	2014 [107]
18-19	5.4	40	30	20	2016 [108]
20.8-22.4	7.4	39.5	35	22	2016 [109]
17.2-20.2	16	40	38	18	2017 [110]
18-19	5.7	40	30	14	2017 [108]
18.5-24	**26**	**36.5**	**40**	**25**	**This work**

Peak values at saturation are shown for all table entries.

6.1 Power Stage Transistor Analysis

The amplifier presented in this work is designed in a Qorvo 150-nm GaN on 100 μm SiC process with slot vias. An 8×100 μm transistor, with pairs of 15 µm spaced gates with internal source vias within the 52 µm spacing between pairs, is chosen for the output network. A nonlinear model (EEHEMT in NI/AWR Microwave Office), validated up to 18 GHz for a 25 C backside temperature, is extrapolated through K-band.

Load pull is simulated at 21 GHz, the center frequency of the design band (18-24 GHz). The output stage transistor is simulated for drain voltages from 10-28 V (28 V being the highest recommended bias point for the process) with a 100 mA/mm quiescent current. For each load pull point an optimum source impedance is also found, to ensure a good input match. This is done to evaluate the output stage transistor performance for possible supply modulation operation.

The load pull data is gathered for a range of bias voltages and assessed for two cases: a maximum PAE match and a maximum P_{out} match. For each of these cases, at each voltage level, the output reflection

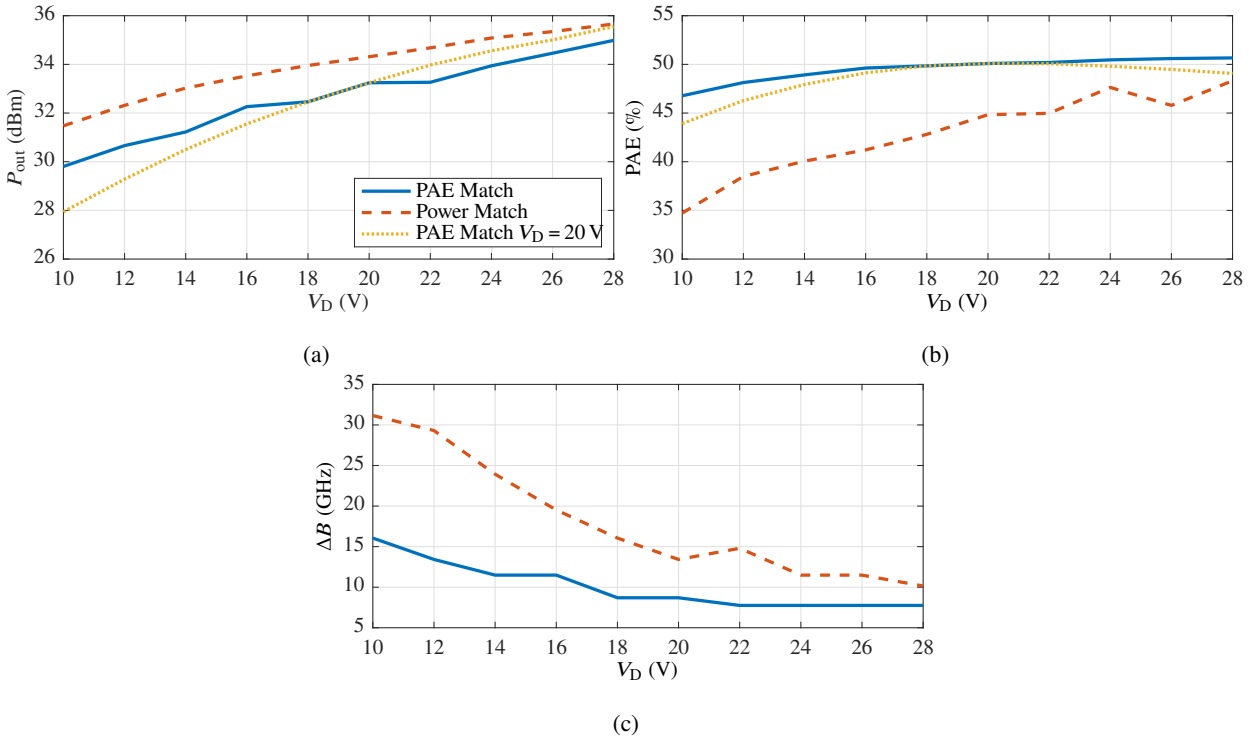


Figure 6.1: Simulated (a) P_{out} and (b) PAE performance of the 8×100 μm transistor at 21 GHz over drain voltage, and (c) drain bandwidth assessed using the Bode-Fano criterion.

coefficient, Γ_L, is converted into an equivalent parallel RC network that models the output impedance at the drain. A similar process is performed to model the gate as an equivalent series RC circuit [111]. From the results shown in Fig. 6.1a there is a less than 0.5 dB variation in P_{out} when using either an optimized PAE or P_{out} match for the range of voltages. Fig. 6.1b shows that this is accompanied by a 1-5 percentage point (pp) variation in PAE. Some of the ripple in PAE is likely due to the settings of the load pull sweep and the drain voltage extrapolation of the model.

Using the RC models of the transistor drains, the achievable bandwidth of a matching network can be estimated using the Bode-Fano criterion [112]. It can be shown that the bandwidth, ΔB, is related to the return loss of the reflection coefficient, $\mathrm{RL}(|\Gamma|)$, by:

$$\Delta B \leq \frac{10}{RC \cdot \ln(10) \cdot \mathrm{RL}(|\Gamma|)} \tag{6.1}$$

Using a 20 dB return loss as the match criterion, a plot as a function of drain voltage is obtained in

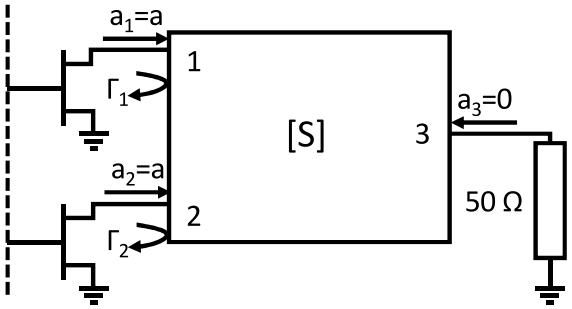


Figure 6.2: Circuit diagram of 3-port non-isolated power combiner with output-stage devices at ports 1 and 2 replaced by their equivalent *RC* network impedances.

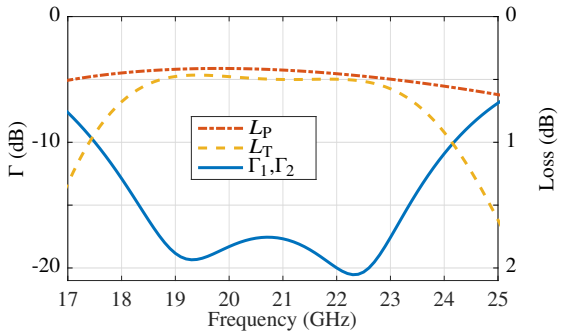


Figure 6.3: Simulated power loss, transducer loss and reflection coefficients for the power combiner network in the final stage of the PA.

Fig. 6.1c. As the transistor is biased at a higher voltage, the optimal reflection coefficient for P_{out} and PAE moves towards the edge of the Smith chart. This increases the Q factor of the *RC* network and reduces the achievable bandwidth of a matching network.

Based on this analysis, a transistor load impedance, Z_{T}, corresponding to the maximum PAE point at 20 V is chosen for the design. The corresponding PAE and P_{out} performance is shown in Fig. 6.1a and Fig. 6.1b.

6.2 Amplifier Design

6.2.1 Matching Network Synthesis

Based on the load-pull data for the transistors and the target output power of 4 W, two 8×100 µm transistors are selected for the final stage of the amplifier. The transistors are combined through a reactive three port network as seen in Fig. 6.2. The *S*-parameters are defined for Z_1=Z_2=Z_{T} at ports 1 and 2 and with Z_3=50 Ω, using complex port parameters [113]. Referring to Fig. 6.2, the *S*-parameter representation of this network is:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a \\ a \\ 0 \end{bmatrix} \tag{6.2}$$

and the reflection coefficient at port 1 becomes:

$$\Gamma_1 = \frac{b_1}{a} = S_{11} + S_{12} \tag{6.3}$$

In equation (6.3) the reflection seen at port 1 is not simply S_{11} but includes the coupling from port 2, S_{12}, therefore taking into account the non-isolated combiner effects.

A common loss definition [114] used in amplifier design is the power loss of the circuit, L_P, which removes the effects of the mismatch. This will be defined in terms of the power delivered to the load, P_{LD}, and the power delivered to the combiner, P_{CD}:

$$L_P = \frac{P_{LD}}{P_{CD}} \tag{6.4}$$

Using the assumptions made in (6.2), the power delivered to the load becomes:

$$\begin{aligned} P_{LD} &= (|b_3|^2 - |a_3|^2) = |b_3|^2 \\ &= |S_{31} + S_{32}|^2 \cdot |a|^2 \end{aligned} \tag{6.5}$$

The power delivered to the combiner is then found to be:

$$\begin{aligned} P_{CD} =& P_{CD,1} + P_{CD,2} \\ =& (|a_1|^2 - |b_1|^2) + (|a_2|^2 - |b_2|^2) \\ =& (|a_1|^2 - |S_{11} + S_{12}|^2 \cdot |a_1|^2) + \\ & (|a_2|^2 - |S_{21} + S_{22}|^2 \cdot |a_2|^2) \\ =& \big((1 - |S_{11} + S_{12}|^2) + (1 - |S_{21} + S_{22}|^2)\big) \cdot |a|^2 \end{aligned} \tag{6.6}$$

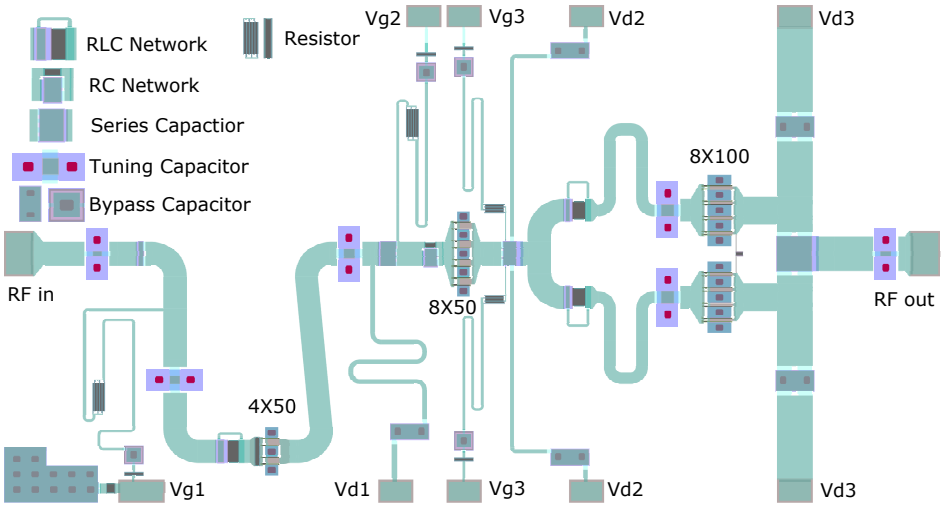


Figure 6.4: Final MMIC layout in a 4 mm *times* 2 mm footprint. A legend for sub-circuits discussed in the text of the chapter is included in the top left. The drain bias lines of the 2nd and 3rd stage and the gate bias lines of the 2nd stage are designed with vertical symmetry to ensure equal impedances are presented to the output-stage devices.

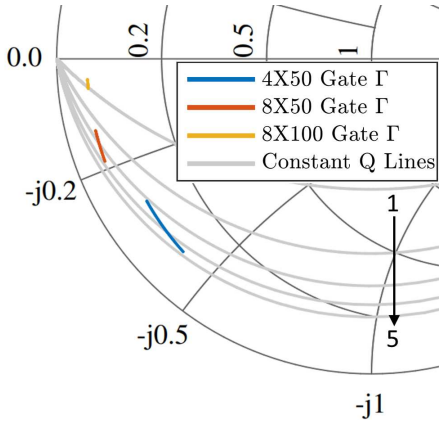


Figure 6.5: Impedances of the transistor gates modelled as series *RC* circuits from 16 to 25 GHz, with constant Q-factor arcs shown for Q=1-5. Smaller transistors are modelled by higher-Q resonators, making broadband matching more difficult.

Combining the above, the power loss can be expressed as:

$$L_P = \frac{|S_{31} + S_{32}|^2}{(1 - |S_{11} + S_{12}|^2) + (1 - |S_{21} + S_{22}|^2)} \tag{6.7}$$

Simulation results for this loss metric for the output combiner are seen in Fig. 6.3. This metric gives a conservative estimate of loss as the match of the network degrades. For the efficiency of the final stage of an

amplifier, it is important to maximize the match of the network to the optimal transistor load and a different loss metric, transducer loss L_T, is more appropriate for the design of the output matching network. This is defined in terms of the power delivered to the load, P_{LD}, and the power available to the combiner, P_A:

$$L_T = \frac{P_{LD}}{P_A} \tag{6.8}$$

The power available at the input ports of the combiner is:

$$P_A = (|a_1|^2 + |a_2|^2) = 2 \cdot |a|^2 \tag{6.9}$$

and combined with equations (6.5) and (6.8) results in the transducer loss:

$$L_T = \frac{|S_{31} + S_{32}|^2}{2} \tag{6.10}$$

This loss metric more accurately reflects the frequency response of the combiner without masking the effects of deviation from the large signal impedance match at the transistor ports or coupling between transistors.

The loss metrics along with the derived Γ for the output matching network are illustrated in Fig. 6.3. Because the design is symmetric (S_{11}=S_{22}) the two transistors see the same reflection coefficient. The same method is valid for the input network of this stage.

6.2.2 Amplifier Design and Stability Analysis

To achieve 30 dB of small-signal gain, a three stage design is selected. The chosen staging ratio for the transistor peripheries is 1:2:8. This ensures that the current draw of the two driver stages has a minimum impact on the total efficiency of the amplifier. The first and second driver stages use 4×50 μm and 8×50 μm transistors, respectively. The transistor models are validated for 18-35 GHz operation.

Once the topology is determined, small and large signal models are used for a final optimization of the matching networks. Concurrent small and large signal optimization was performed to ensure maximum large signal performance while maintaining stability, gain flatness (small-signal gain >30 dB with ±1.5 dB

flatness), and match ($|S_{11}|$ and $|S_{22}|$ <-10 dB). It should be noted that all bypass capacitors at the gates and drains are minimized to allow supply modulation in the future, while maintaining low-frequency stability. The gate bypass capacitances are 1, 2, and 2 pF while the drain bypass capacitances are 3, 6, and 8 pF for the 1st, 2nd, and 3rd stage, respectively. The smaller capacitor values do not negatively affect RF performance.

The final layout of the circuit can be seen in Fig. 6.4. The 4×50 µm transistor used for the first stage has the highest Q factor gate equivalent circuit requiring a higher order matching network. Two capacitors to ground create an easily tunable low-loss matching network. A small series capacitor along with a RLC and R network are used to decrease the out-of-band gain and eliminate in-band oscillations. The first interstage network uses a simple LCL matching network; the microstrip lines act as inductors, combined with an RC stability circuit to suppress low frequency gain. The second interstage match follows the same topology as the first, but a RLC stability network is used. This network suppresses higher and lower frequency gain while allowing the in-band gain to be shaped by appropriate choice of the resonant frequency. The output matching network makes use of low impedance lines to minimize loss. Bias circuits are absorbed into the matching networks, and all gate bias lines have resistors that dampen any resonances. Both input and output matching networks account for a 10-mil alumina to 100 μm SiC bondwire transition modelled in a full-wave electromagnetic simulator (HFSS).

K factor is not sufficient for stability analysis of multi-stage power-combining amplifiers [115], therefore a Nyquist loop-gain analysis is performed [116] under large and small signal operation at various bias points. Odd mode stability is evaluated for the the final stage and a resistor added [117].

6.3 Probed Amplifier Performance

6.3.1 Small-Signal Performance

The amplifier was fabricated as part of a shared wafer run, and 230 chips were made on 5 wafers, W={1, 2, 3, 4, 5} in 7 positions along the axis normal to the gate fingers, Y={10, 15, 20, 25, 30, 35, 40}, and 9 positions parallel to the gate fingers, X={5, 7, 9, 11, 13, 15, 17, 19, 21}. Pulsed large and small signal measurements were performed on the chips at 9 frequency points, f={19.5, 20, 20.5, 21, 21.5, 22, 22.5, 23,

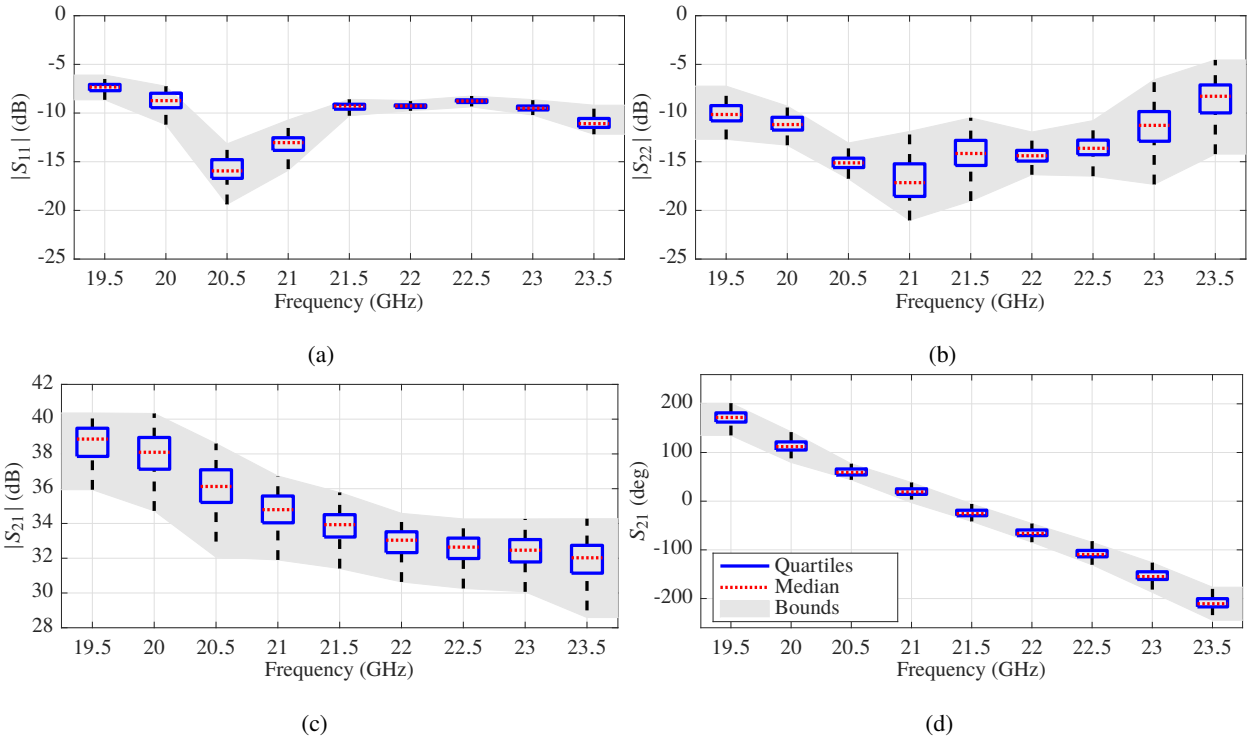


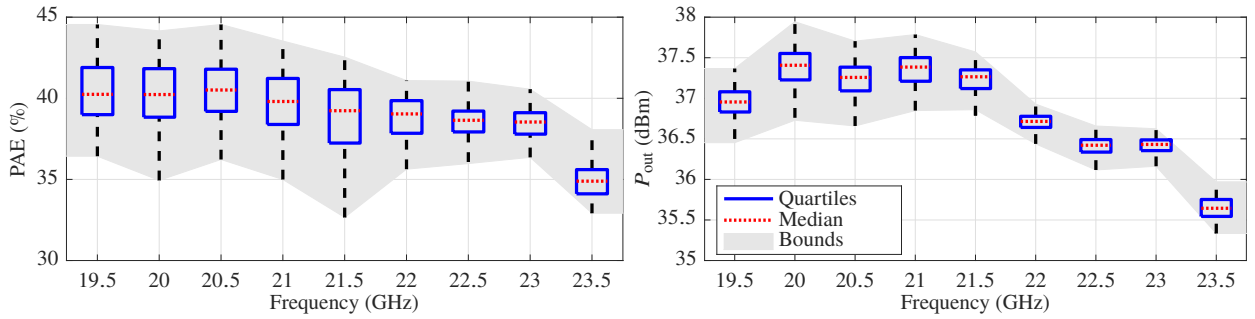
Figure 6.6: Small-signal $|S_{11}|$, $|S_{22}|$, $|S_{21}|$ and $\angle S_{21}|$ measured across 5 wafers. The graph shows the performance of 202 of 230 measured chips. 230 chips were probed of which 28 of the chips performed as outliers and are not shown. An outlier is defined as performing below Q_1-1.5×IQR or above Q_3+1.5×IQR where IQR is the interquartile range and Q_1 and Q_3 are the lower and upper quartiles respectively. The boxes include 50% of the measured chips, and the range shows performance of all 202 die.

23.5} GHz. Large signal on-wafer pulsing was performed with a 100 µs pulse using a 10 % duty cycle at three drive levels P_{in}={8, 10, 12} dBm.

The probed data performance is expected to differ from the mounted amplifier performance, as the amplifier was designed to have a transition to alumina on the input and output, but can still be used to see trends in the performance of the amplifier across wafer and X/Y position.

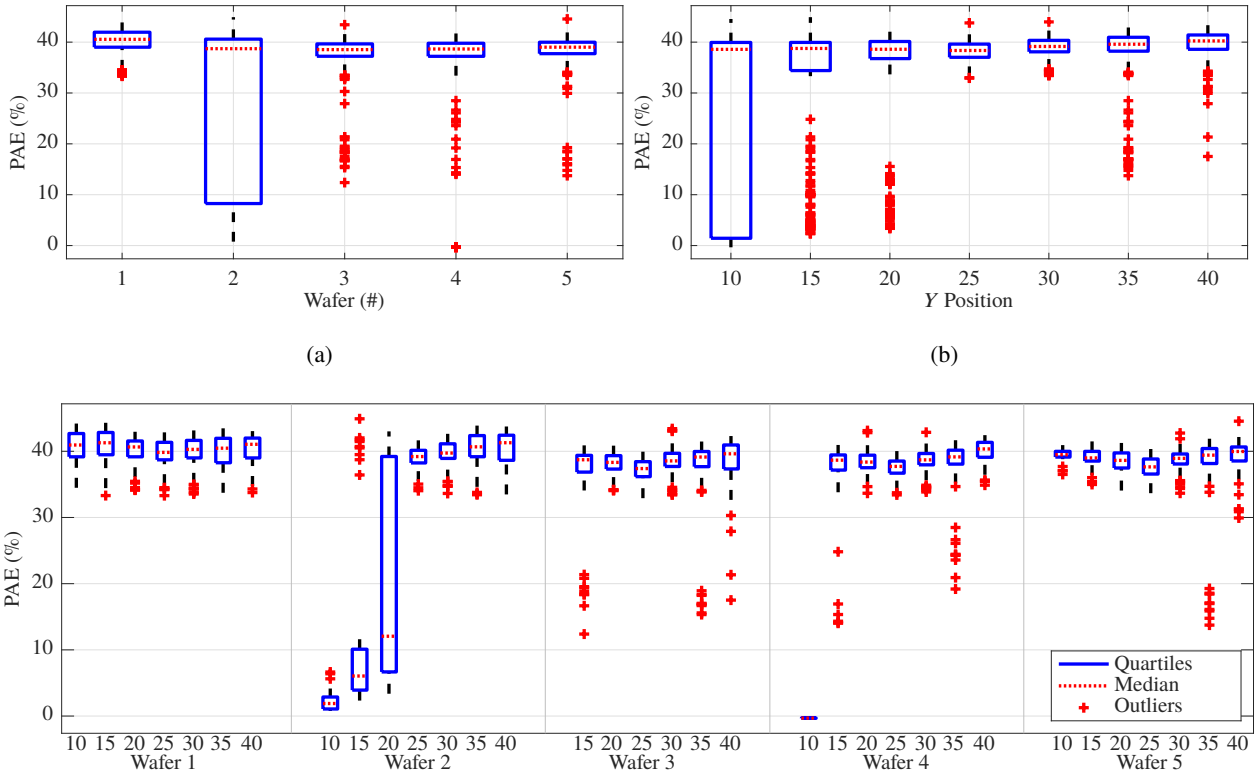
Probed small signal performance of the amplifier chips is shown in Fig. 6.6. A small percentage of chips, deemed outliers, are excluded from these plots in order to improve readability, but are included in the final analysis of performance. Boxplots are used to show the quartiles and means of the dataset because they make no assumptions about the distribution of the amplifiers dependent variable.

Return loss, $|S_{11}|$, varies from -7 to -20 dB across the frequency band. The lower frequency performance (≤21 GHz) shows a greater variation than the higher frequency data. The $|S_{22}|$ similarly varies from -4 to



(a) (b)

Figure 6.7: Measured PAE (a) and output power (b) for wafer-probed amplifier die at 11 dBm input drive. The graph shows the performance of 202 of 230 measured chips. 230 chips were probed of which 28 of the chips performed as outliers and are not shown. An outlier is defined as performing below Q_1-1.5×IQR or above Q_3+1.5×IQR where IQR is the interquartile range and Q_1 and Q_3 are the lower and upper quartiles respectively. The boxes include 50% of the measured chips, and the range shows performance of all 202 die.



(a) (b) (c)

Figure 6.8: PAE statistics as a function of wafer number W (a), position Y (b), and number vs. position W:Y (c) for 230 probed die.

-22 dB across the frequency band. The mid band of the performance (20-22.5 GHz) shows the best match with a $|S_{22}| \leq$ -10 dB. $|S_{21}|$ shows an approximately 4 dB variation at each frequency point. The mean gain varies from 39 dB at the lowest frequency to 32 dB at the highest frequency. The higher than expected gain variation across the band is likely due to the lack of bondwire interconnect and is not observed for mounted chip measurements. It should be noted that, based on the frequency dependence of the gain, we expect that measurements would show high gain performance below 19.5 GHz. Note also that the transmission phase response, Fig. 6.6d, varies linearly over frequency, as expected.

6.3.2 Large-Signal Performance

Large signal performance at P_{in}=12 dBm is shown in Fig. 6.7. Data from 28 of the 230 measured chips are considered outliers and removed for readability. Average PAE stays around 40 % excluding the 23.5 GHz point. The mean of P_{out} varies in the range of 37 dBm±0.5 dB excluding the 23.5 GHz point which drops down to below 36 dBm.

A statistical analysis is performed in which the PAE data at a 12 dBm drive level is the dependent variable. The analysis aims to see how the W, X, Y, and f affect the efficiency of the chips. From this we can derive the main manufacturing factors that affect the variation in the amplifiers performance. All statistical analysis is performed using SPSS [118]. An Analysis of Variance (ANOVA), which allows multiple group means to be compared for statistical significance, is performed. Outlying chips were not manually remeasured, so any error in the probing cannot be thoroughly ruled out while examining the performance of the chips.

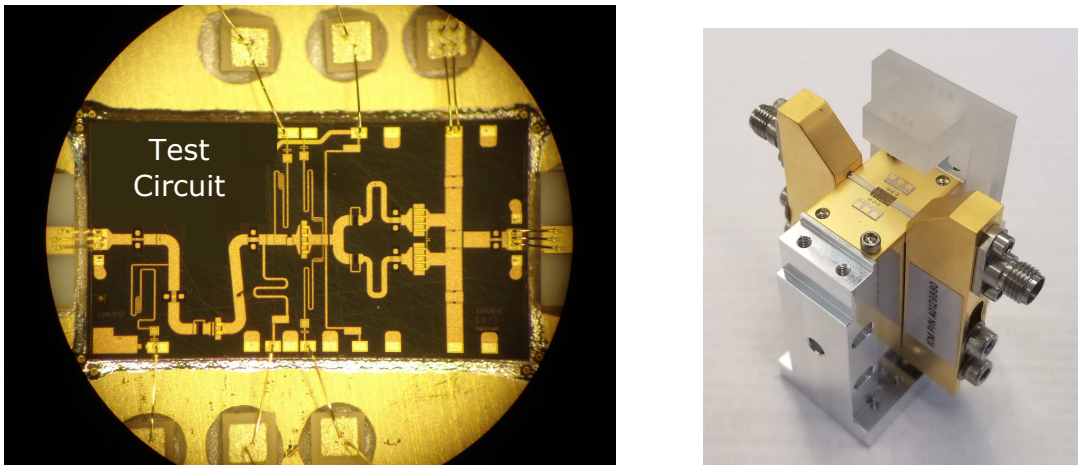
A four-way ANOVA analysis is performed on the main effects and all possible two-way interactions of W, X, Y, and f. The analysis results are shown in Table 6.2 with an additional column added for the "importance", ω_{i}^2, of each parameter calculated as:

$$\omega_{\text{i}}^2 = \frac{SS_{\text{i}} + (df_{\text{i}})MS_{\text{residual}}}{SS_{\text{total}} + MS_{\text{i}}} \tag{6.11}$$

where SS is the sum of squares, MS is the mean square, df is the degrees of freedom , and i is the grouping of variables. A type-III SS is used due to unequal variances between the groups [119]. The results for f are not shown due to a lack of statistical significance.

Table 6.2: ANOVA of Means

Source	df	SS	MS	ω^2 (%)
X	8	3202.7	400.3	1.7
Y	6	35942.3	5990.4	18.3
W	4	27089.3	6772.3	13.8
X:Y	33	11312.6	342.8	6
X:W	32	10659.1	333.1	5.6
Y:W	23	71246.3	3097.7	36.4
Error	1811	24953.4	12.7	
Total	2069	196511.4		81.8

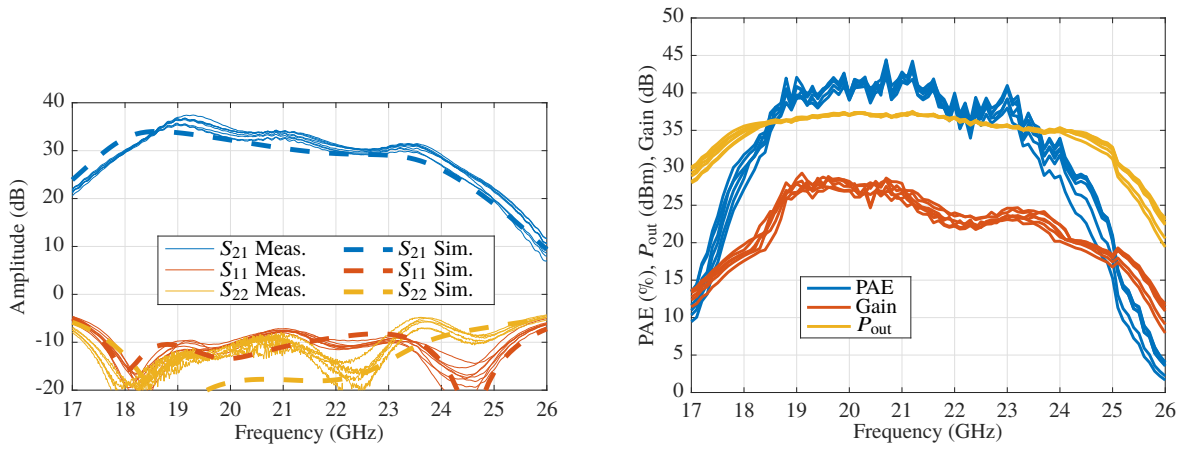


(a) (b)

Figure 6.9: (a) Photograph of the 3-stage K-band MMIC mounted on a CuMo carrier and bonded to 10-mil alumina microstrip lines at input and output. 100 pf bypass capacitors are bonded to the 6 bias pads. Three bondwires connect the amplifier RF bond pads to the alumina input and output lines. A single bondwire is used for all DC bias lines excluding the final stage where DC current draw is the highest.(b) Photograph of a MMIC in a fixture. The CuMo carrier is attached to an aluminum heat sink. The 3-D printed plastic mount and spring-loaded pins supply DC bias to amplifier. 100 pf off-chip bypass capacitors are bonded to the 6 bias pads.

The ANOVA is able to explain 81.8 % of the variation in the means. The dominant causes of the variation are related to the wafer-to-wafer performance and the Y position on the wafer which account for 68.5 % of the variations in means. Boxplots analyzing these variations are shown in Fig. 6.8. It can be seen that wafer W=2 has the worst performance while the Y=10 position performs the worst of the Y positions.

A Games-Howell test [120] is used for the post-hoc analysis of the ANOVA results. The results of this



(a) (b)

Figure 6.10: Simulated (dashed) and measured (solid) small-signal parameters for 8 mounted chips from 17 to 26 GHz.

analysis are discussed for the three independent variables, W, X and Y, without interactions and the following conclusions can be made:

- PAE performance is the lowest for W=2, with the mean performance being 8 pp lower than for W=4, the second lower performing wafer;
- Amplifiers with higher Y values perform better with a 17 pp variation from Y=10 to Y=40;
- There is no clear performance trend in the X values, but PAE varies by over 5pp depending on X (from 34-39 %).

6.4 Packaged IC Performance

Ten MMICs are evaluated in the fixture shown in Fig. 6.9b. The MMIC is mounted on a CuMo carrier and wire bonded to 50 Ω microstrip lines on 10-mil thick alumina. The carrier is attached to a custom aluminum fixture and connected to 2.9-mm coaxial connectors via a microstrip to coaxial transition. Spring loaded pins are used to connect the bias voltages to pads on the chip through 100 pF off-chip bypass capacitors mounted on the CuMo carrier, seen in Fig. 6.9a. Off-chip bypass capacitors are present for testing but are

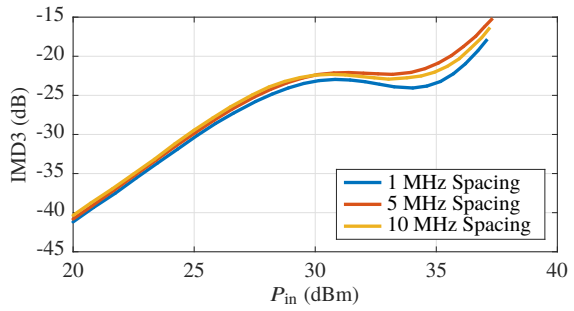


Figure 6.11: Measured third-order intermodulation product relative to the carrier power of one of the MMIC amplifiers at 20 GHz for three tone spacings: 1, 5 and 10 MHz.

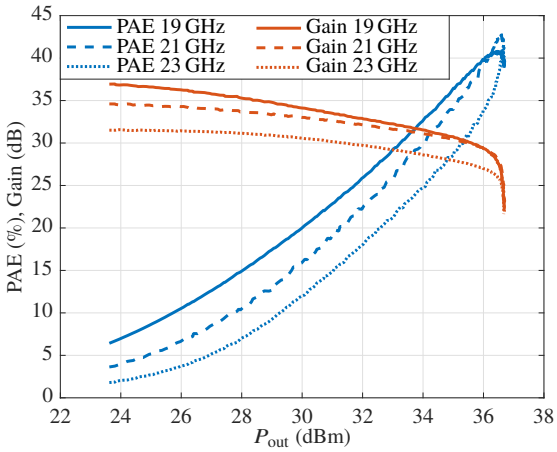


Figure 6.12: Measured large signal amplifier gain and efficiency saturation curves for three frequencies within the band of interest.

not necessary for amplifier stability.

Testing is done with a 20 V drain bias a 100 mA/mm quiescent current. A small signal gain of 33 dB with a ±3 dB gain variation from 18-24 GHz presented in Fig. 6.10a. The input return loss is better than 10 dB from 17.5-25 GHz, with good agreement between simulated and measured results for the mounted packaged amplifier.

The large signal performance over frequency for the chips is shown in Fig. 6.10b. The measurements show a large signal gain of 25 dB with variation of ±2.5 dB from 18.5-23.5 GHz. Large signal performance drops off at 18.5 GHz on the low end and 23.5 GHz on the high end with >35 % PAE for that band. Saturated output power for this band peaks above 36 dBm. This GaN process has been shown to have minimal power droop under high power operation [121].

The third order inter-modulation distortion (IMD3) relative to the power at the 20-GHz carrier frequency can be seen in Fig. 6.11 for three tone spacings. The C/I ratio degrades as function of tone spacing peaking just over -20 dB when the amplifier is saturated. In Fig. 6.12 gain and PAE curves are shown for three discrete frequencies across the band. The PA saturates at the same output power point at the three frequencies and is compressed by 3-5 dB at the point of maximum PAE.

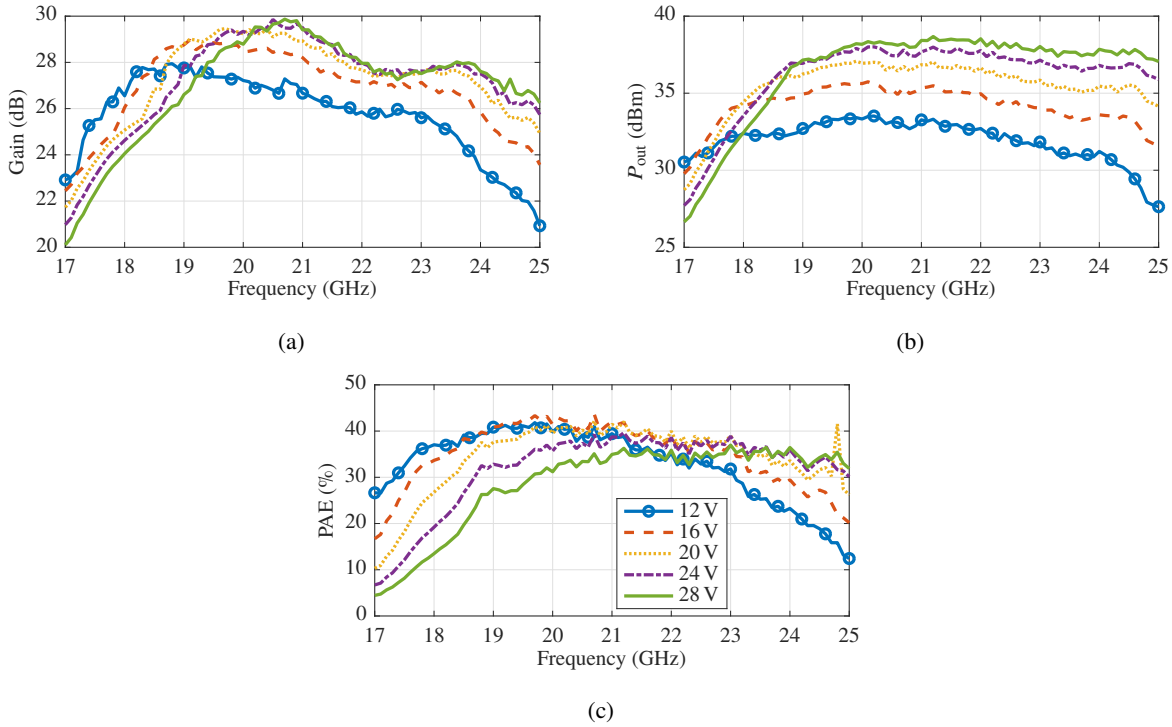


Figure 6.13: Measured gain, output power and PAE for a MMIC mounted in a fixture over 12 - 28 V variation of supply voltage for all three stages simultaneously, shown at peak efficiency.

6.5 Summary

The performance and design methodology of a three stage K-band MMIC are presented. The operational bandwidth of the amplifier extends from 18.5 GHz to 24 GHz, a greater than 25 % fractional bandwidth. The MMIC shows greater than 4 W peak output, a peak efficiency exceeding 40 %, and a saturated gain greater than 22 dB. The MMIC PA is designed with consideration to the supply-voltage dependence of the PAE, P_{out} and bandwidth for intended supply modulation to further increase the efficiency.

Fig. 6.13 shows the measured large-signal gain, output power and efficiency as the supply voltages of all three stages are varied simultaneously. These measurements indicate that the PA is a good candidate for supply modulation with potentially high bandwidth, since it is designed to be stable with minimal capacitance in the drain circuit. Additionally, the gain does not vary substantially over a wide range of supply voltages, implying that relatively simple linearization can be used under dynamic supply operation.

The analysis shown in Fig. 6.1 at 21 GHz predicts the PAE response over drain voltage measured in Fig. 6.13c. The 19-23 GHz range shows an area of optimal supply modulation performance, where peak PAE will be higher (or equal) for lower drain voltages. As the frequency changes to values greater than 23 GHz, the PAE for lower voltages degrades. Similarly, below 19 GHz supply modulation would not be practical due to the drop-off in P_{out} for higher drain voltages, which can be seen by the overlapping lines in Fig. 6.13b. The bandwidth where supply modulation is practical lines up well with the areas of peak PAE seen in Fig. 6.10b.

The chapter presents the design flow, starting with transistor sizing and network design, and includes matching network synthesis for a non-isolated reactive combiner as well as stabilization. Measured PA performance over 5 wafers is statistically analyzed for both small and large signal data on 230 on-wafer probed MMICs. Large-signal measurements are performed on 10 fixture-mounted die, including PAE, P_{out} and saturated gain over frequency and power, and two-tone linearity is characterized.

The details presented in this chapter are contained in publication [57, 80].

Chapter 7

Discrete Supply Modulation of the K-Band PA

Contents

In this chapter a three-stage GaN MMIC K-band PA [57], the design of which is discussed in Chapter 6 is tested at 19.8 GHz with drain supply modulation as shown in Fig. 7.1. An efficient GaN MMIC discrete supply modulator [39], discussed in Section 3.2.2b, is used to generate the drain supply voltage. The supply modulation is designed to increase efficiency while improving linearity over that of a static supply. Using several methods to reduce the switching speed requirements for the supply modulator, a modulation

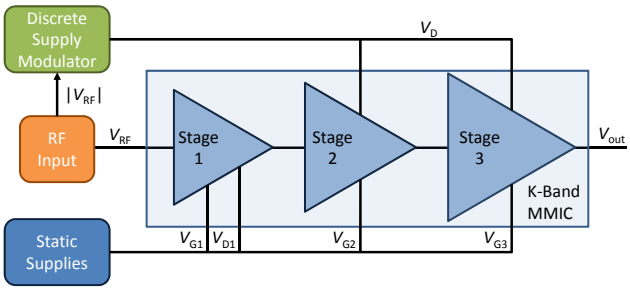


Figure 7.1: Block diagram of supply-modulated transmitter with a dynamic drain voltage V_D on the second and third stage of a three-stage PA, while the first stage supply is static (V_{D1} = const). The three gates are statically biased.

bandwidth of 100 MHz and 250 MHz are both demonstrated. For 100 MHz signals with PAPR>10 dB, we demonstrate an average efficiency improvement from 14% to 20% with a simultaneous linearity improvement in NPR from 23 to 26 dB through a shaping function focused on gain linearization. For 250-MHz signal bandwidth, there is not observed degradation in NPR and the efficiency is improved by 5 percentage points. The results are an extension of the work in [75], where the signal bandwidth was limited to 50 MHz. In addition to extending the signal bandwidth two and five times, we develop a new shaping function design approach, and characterize the effects of finite switching speed of the discrete supply.

Previous work in GaN implementations of both PA and dynamic supply demonstrated modulation bandwidths of up to 80 MHz with continuous supply modulation for a sub 6 GHz PA [122]. Discrete supply modulation has exceeded this with an 8-level tracker showing 100 MHz modulation bandwidth [123] and a 3-level tracker showing a 120 MHz modulation bandwidth [65], both for sub-6 GHz carrier frequencies. X-Band implementations of SM have also been demonstrated, however, the modulation bandwidths have not exceed 20 MHz [40, 124]. At K-band, discrete supply modulation with concurrent gate modulation was shown in GaAs for a signal bandwidth of 1 MHz [101]. Higher modulation bandwidths (20 MHz) were achieved at single-digit efficiency with SM and an off-the-shelf GaAs Q-band (44 GHz) amplifier [125].

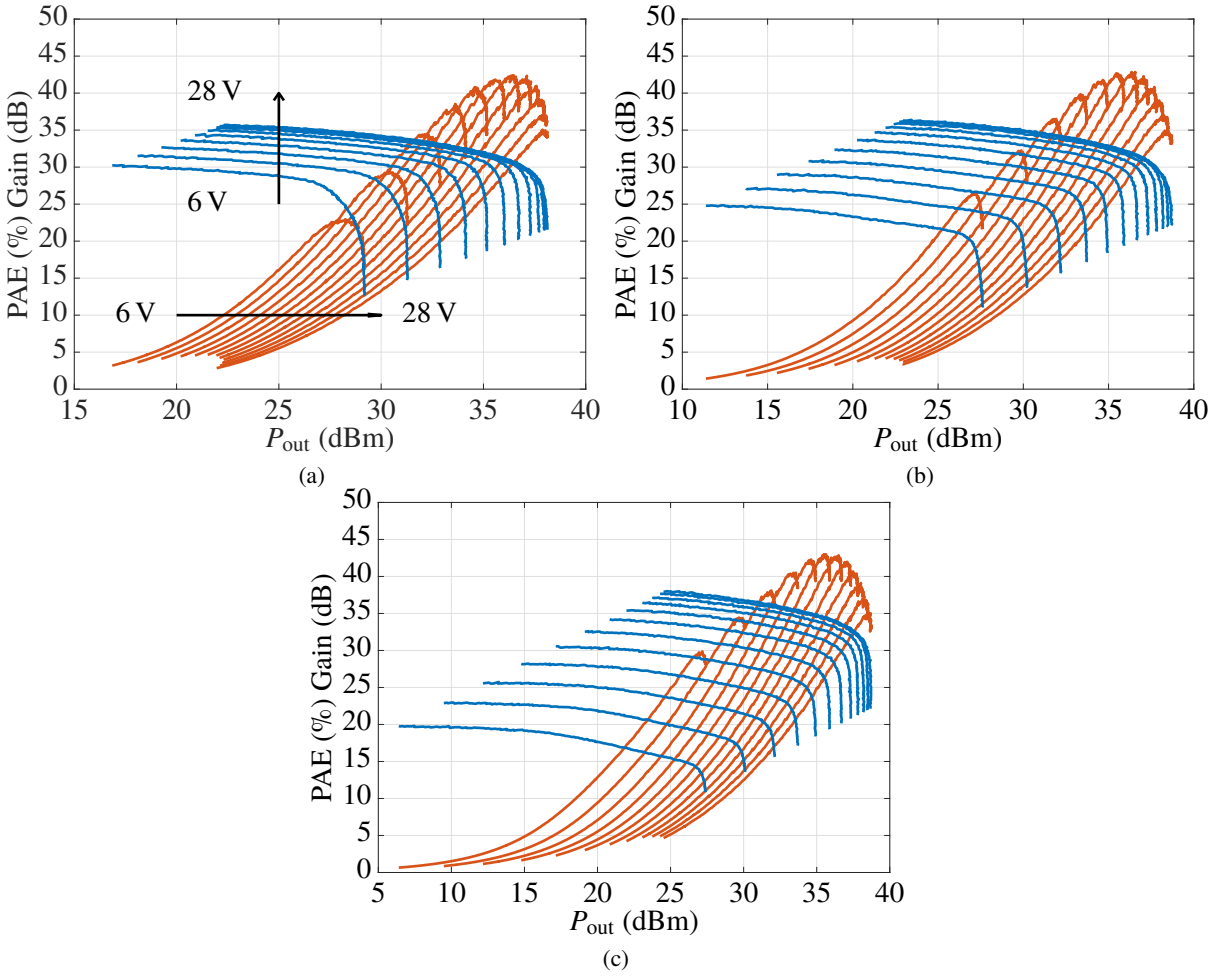


Figure 7.2: Static amplifier gain and PAE performance at 19.8 GHz as V_D varies from 6-28 V in 2 V steps varying (a) the final stage, (b) the final two stages, and (c) the final three stages. Static stages are set to 20 V and biased at 100 mA/mm.

7.1 Amplifier Characterization

Static measurements of the K-band amplifer, seen in Fig. 7.2, show variation in CW performance with a varying drain voltage for different numbers of amplifier stages. This analysis shows that modulating all three stages provides the largest improvement in efficiency with the largest variation in gain, the inverse can be said about modulating one stage. This data is analyzed using the methods described in Section 2.2.1 and it is determined that modulating the two output stages provides the best balance in linearity and efficiency performance.

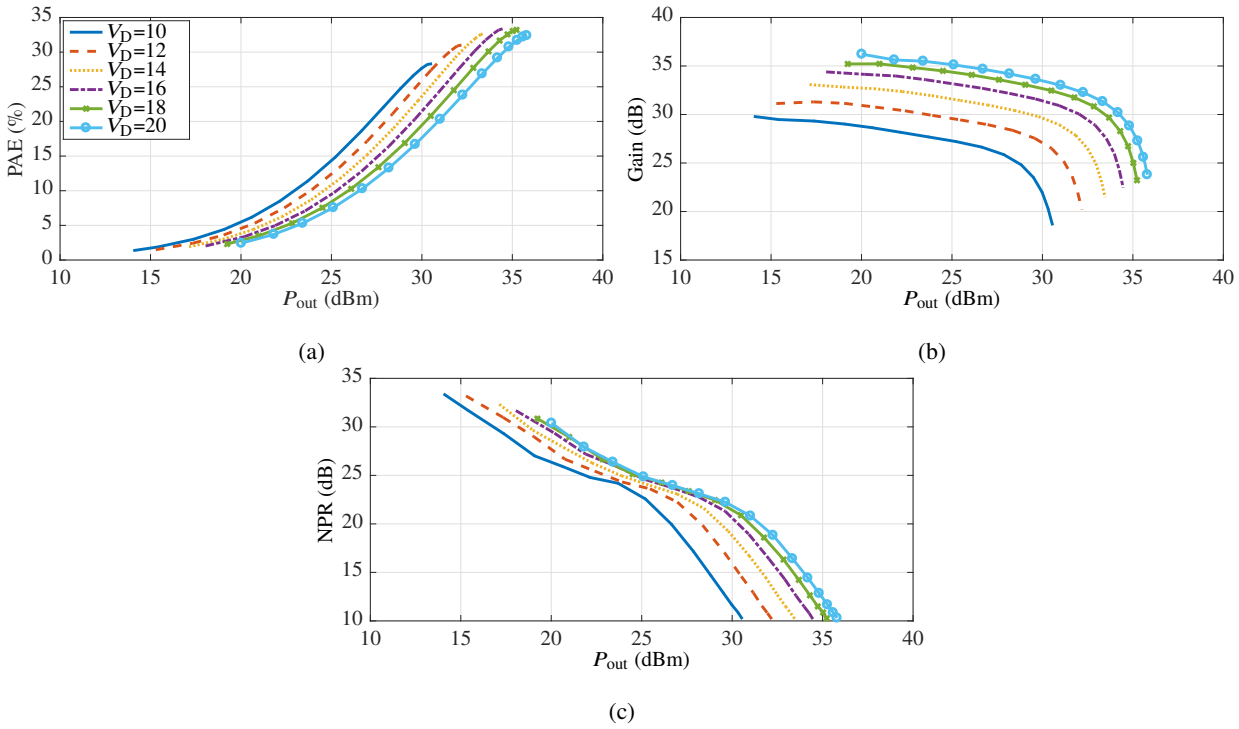


Figure 7.3: Amplifier performance at 19.8 GHz with a 50 MHz noise-like signal for $V_D = \{10,12,14,16,18,20\}$ V. Performance is shown over P_{out} for (a) PAE, (b) gain, and (c) NPR.

The amplifier is then tested with a noise-like signal as discussed in Section 3.3.4. The metric of linearity used with this type of signal is noise power ratio (NPR) which aims to measure the amount of signal that is generated in the notched part of the signal relative to the rest of the signal. Signals generated in this way will have a PAPR > 10 dB, and specifically in this work PAPR = 10.5 dB.

Characterization is first done for $V_D = \{10, 12, 14, 16, 18, 20\}$ V seen in Fig. 7.3 with a 50 MHz noise-like signal at 19.8 GHz. As can be seen in Fig. 7.3a changing the drain voltage moves the peak efficiency point from $P_{out} = 36$ dBm for a 20 V supply to $P_{out} = 30$ dBm for a 10 V supply. These curves help estimate the maximum possible improvement from supply modulation. For supply modulation ranging from 10-20 V the efficiency should be the envelope of these curves, showing a maximum achievable efficiency improvement of ~ 10 pp. Also of interest is the effect of V_D on NPR. Lower drain voltages move the 20 dB NPR point to lower output powers P_{out} by 5 dB as seen in Fig. 7.3c. The gain varies by 5 dB over drain voltage however because the gain is > 30 dB, supply modulation will not degrade gain to the point where is affects PAE. The gain variations can also be mitigated by effective shaping function (SF) design i.e. the relationship between

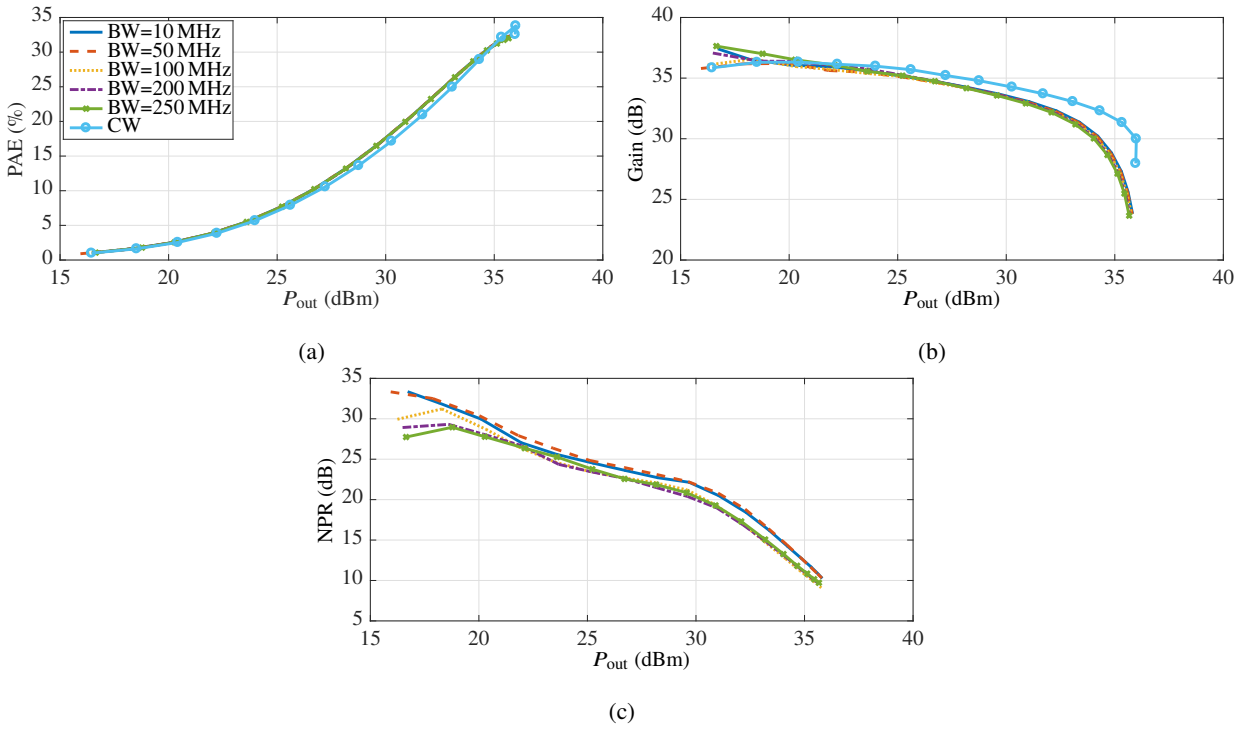
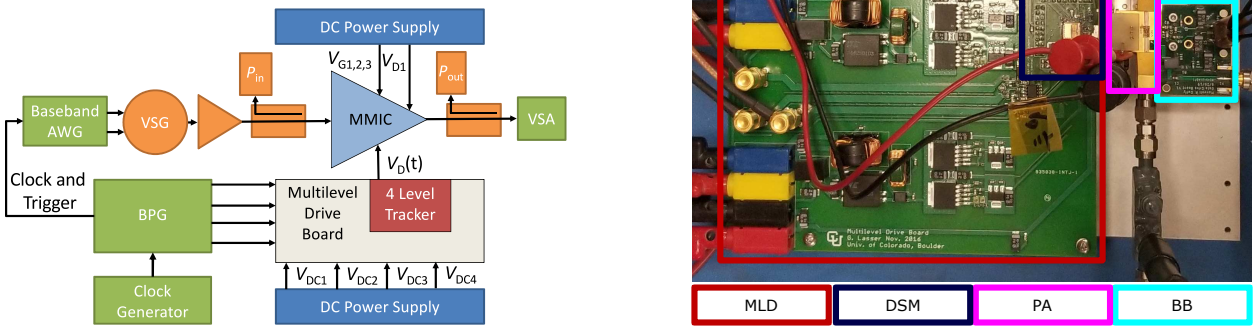


Figure 7.4: Measured (a) PAE, (b) gain, and (c) NPR at 19.8 GHz with V_D=20 V for noise-like signal bandwidths = {10,50,100,200,250} MHz as a function of P_{out}.

the input RF voltage and drain voltage.

Further characterization is the done using noise-like signals for a range of bandwidths (BW)={10, 50, 100, 200, 250} MHz, CW testing is also done for reference. Measurement results are shown in Fig. 7.4 for modulated signals with the same PAPR despite bandwidth variations. The PAE and gain of the amplifier are almost identical for the 5 signal bandwidths shown. Performance variation does not become obvious until linearity is investigated in Fig. 7.4c. Here the biggest degradation in NPR can be seen going from 50 to 100 MHz signal bandwidth. NPR reduces by 1-2 dB for $P_{out} > 25$ dB. Based on this characterization, which shows consistent performance as signal bandwidth increases, this amplifier is a good candidate for testing with broadband signals under supply modulation operation.



(a) (b)

Figure 7.5: (a) Block diagram of test setup. Gate bias voltages 1, 2, and 3 are independently set. Drain supply voltage V_{D1} is static, while dynamic drain voltages $V_{D2} = V_{D3}$ are provided by a 4-level tracker controlled by a bit pattern generator (BPG) that commutates four external voltages, V_{DC1}, V_{DC2}, V_{DC3}, and V_{DC4}. (b) Picture of test setup. Multi-level driver (MLD), discrete supply modulator (DSM), power amplifier (PA), and bias board (BB) are explicitly labeled.

7.2 Supply Modulation Test Bench

The supply modulated PA is characterized using the test bench shown in Fig. 7.5a. This bench is a variant of the one discussed in Section 3.3.2 and makes use of a 4-level DSM discussed in Section 3.2.2b. The 4-level DSM is used to generate the discrete dynamic drain voltage for the amplifier. The DSM is connected to the two final stages of the amplifier through spring loaded pins. This interconnect is made to be as short as possible in order to minimize added inductance. A separate bias board (BB) is used to provide the static voltages for V_{D1}, V_{G1}, and V_{G2}. The static bias connections are bonded directly to off-MMIC 100 pf singe-layer capacitors which are then bonded to the BB which is populated by SMD capacitors enabling low frequency bypassing for the amplifier.

The amplifier is tested using the signals described in Section 7.1. The signal generation bandwidth of the setup is approximately 1 GHz, however the signal receiver bandwidth (for IQ data) is limited by a maximum

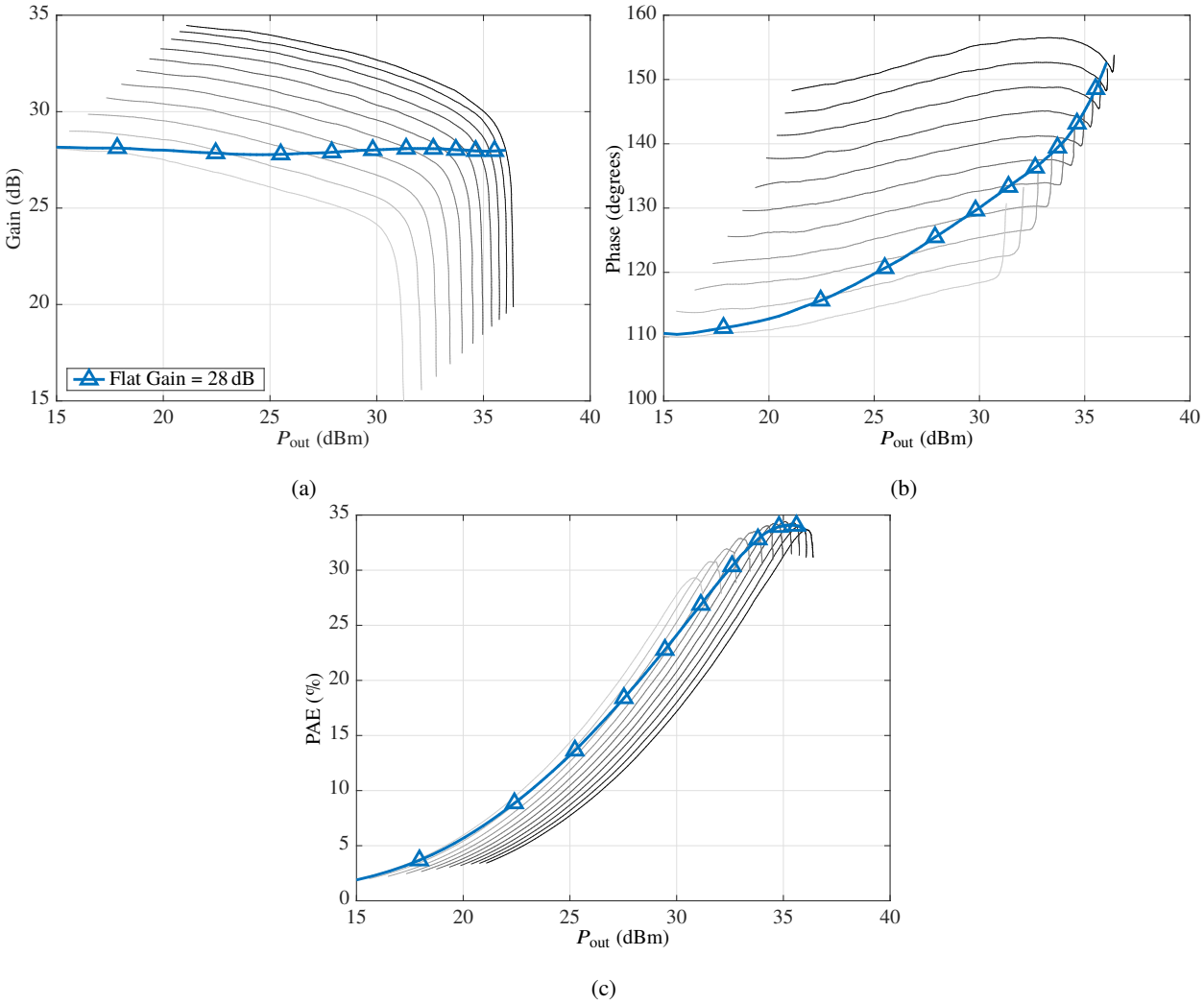


Figure 7.6: Measured (a) gain, (b) phase, and (c) PAE at 19.8 GHz of the three-stage MMIC PA as a function of output power P_{out}. the supply voltage V_{D1} of the first stage is kept constant at 20 V, while $V_{D2} = V_{D3}$ are simultaneously varied from 10-20 V. The static performance is shown in grey lines in 1-V steps darkening with higher V_D. While the gain amplitude stays flat at 28 dB, the phase is expected to vary by 40°.

140 MHz IF bandwidth and a sampling rate of 170 MHz. Received data is time and phase aligned in post processing. Full spectrum measurements are taken at every power level to check stability. A picture of the power amplifier test fixtures is shown in Fig. 7.5b

7.3 50 MHz Supply Modulation Testing

7.3.1 Shaping Function Design

The amplifier is characterized for several supply voltages (6-28 V) using a measurement setup similiat to the one presented in Section 2.1. The drain supply voltages of most interest are 10-20 V shown in Fig. 7.6. Here the drain voltage is modulated to maintain a flat gain over drive power (Fig. 7.6). The gain value is set by the lowest modulation voltage, here 10 V is used for a gain of 28 dB. The voltage is allowed to vary by 10 V up to $V_{\mathrm{Dmax}} = 20$ V, minimizing the negative effects on linearity from the signal discretization.

Static characterization is used to create the shaping functions (SF) shown in Fig. 7.7a. The continuous flat gain SF is discretized for use with the 4-level DSM. For back-off input power levels, the peak power $\hat{P}_{\mathrm{in}}$ does not reach the level where V_{D}=20 V occurs. In these cases the DSM is being underutilized as fewer of the voltage levels are being used and the discrete voltages levels are not adapted well for the real voltage swing. To mitigate this a modified shaping function is designed when the amplifier is backed-off from saturation. This new adaptive shaping function (ASF) should further improve amplifier performance in back-off. The PDFs of a noise like signal are superimposed on top of the SFs for an amplifier being driven to compression and average power P_{in}=-6 dBm.

7.3.2 Results

The DSM provides the V_{D} only for the second and third stage while the first stage uses a static 20 V supply voltage. The time domain V_{D} for different shaping functions can be seen in Fig. 7.7b. Testing is done at 19.8 GHz and noise power ratio (NPR) is used as the metric of linearity.

Fig. 7.8 shows power sweep results for three cases: a static 20 V supply, supply modulation (SM), and supply modulation using an adaptive shaping function (ASF SM). Static measurements successfully predicted the dynamic gain of the amplifier (28 dB) using SM. For P_{out} >24 dBm the SM cases have virtually identical NPR to the static supply case with NPR actually improving over the static supply case from 24-30 dBm. The ASF case improves NPR, PAE, and flattens gain for P_{out} <26 dBm, which is where V_{D} does not reach the

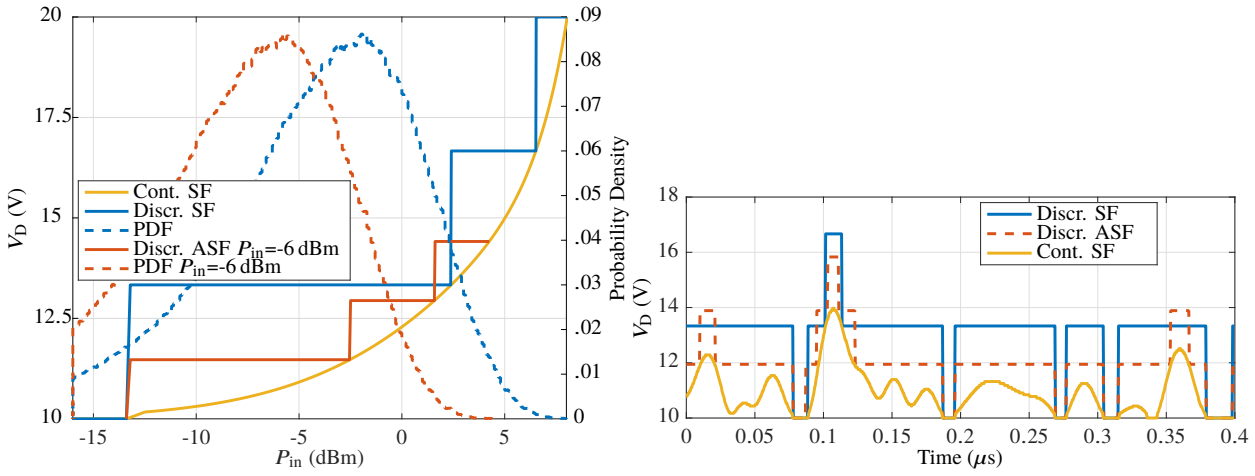


Figure 7.7: (a) Shaping functions derived from static amplifier measurements. Solid lines show three shaping functions: continuous; discretized; and discretized for P_{in}=-6 dBm. This third shaping function is designed for improved efficiency at lower input power levels, compared to a V_D that varies from 10-20 V. PDFs for both discrete cases are shown in dashed lines. (b) Time domain V_D for a 50 MHz noise-like signal at P_{in}=-6 dBm. Three shaping functions are shown: one for discretized 10-20 V variation; the second in which the voltage variation is changed to better reflect the signal statistics; and the third is a continuous function.

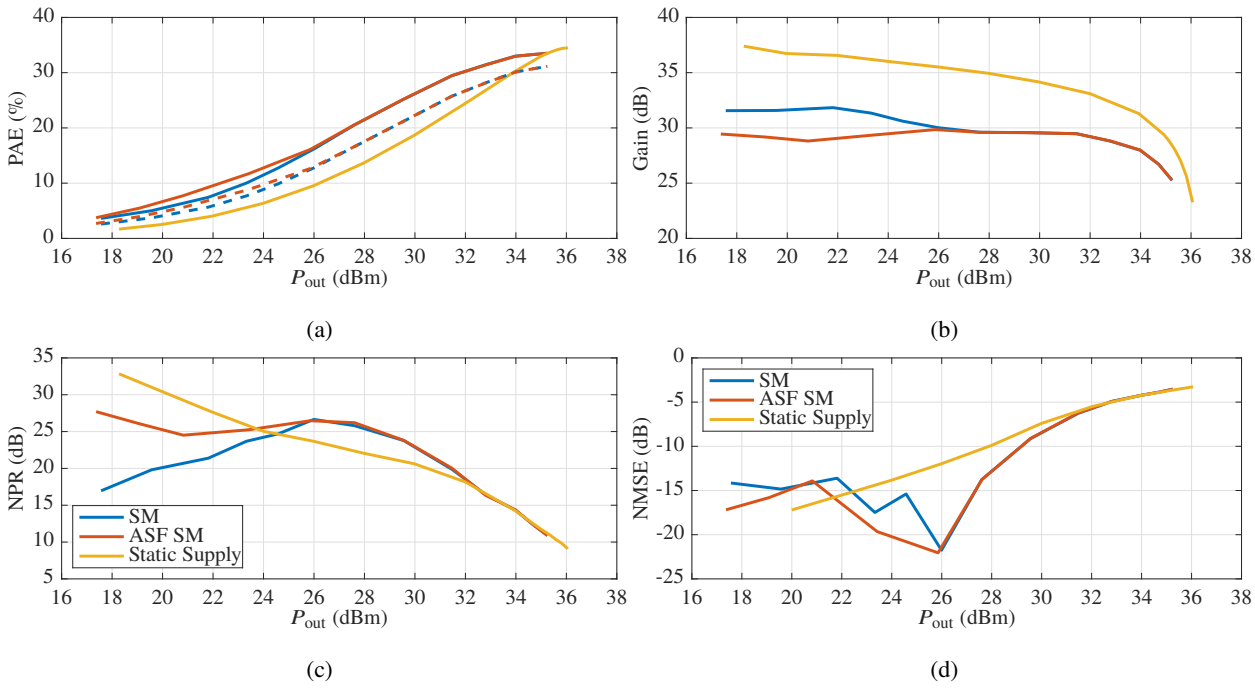


Figure 7.8: Amplifier performance at 19.8 GHz for a static supply, supply modulation (SM), and SM using an adaptive shaping function (ASF). Performance is shown over P_{out} for (a) PAE (efficiency measurements without driver losses are solid while those including driver losses are dashed), (b) gain, (c) NPR, and (d) NMSE.

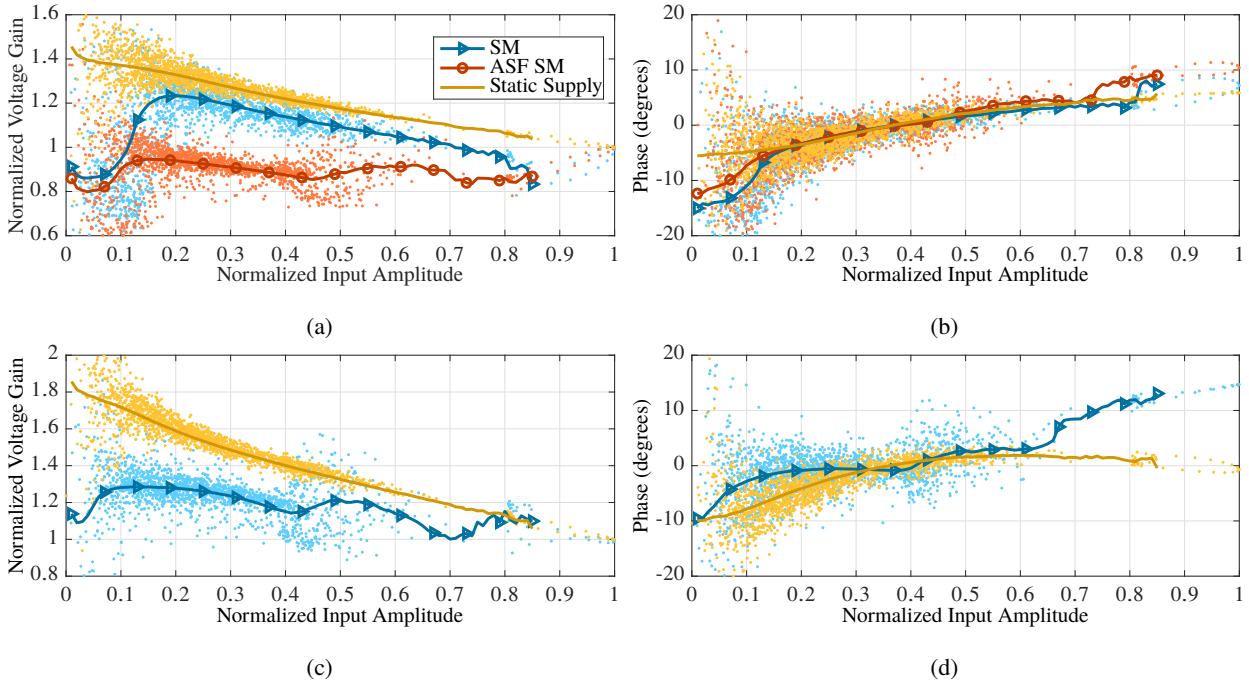


Figure 7.9: Measured performance at 19.8 GHz for *P*out={22,28} dBm showing (a,c) AM/AM and (b,d) AM/PM, respectively, for a 50-MHz NPR signal with a PAPR>10 dB. The blue data points show performance with supply modulation, red points shows supply modulation with an adaptive shaping function, and yellow shows a static supply. The discrete points are faded and a darker trend line is superimposed for clarity. The horizontal axis is normalized to maximum V_{in}. Voltage gain is normalized to unity for the peak input amplitude. At *P*out=28 dBm, the two supply modulation cases give identical performance so only one is plotted.

20 V level using SM. Without driver losses taken into account PAE improves by 9pp for supply modulation, or 4.5pp when factoring in driver losses. A more efficient DSM architecture with reduced driver losses would further benefit transmmitter efficiency.

AM/AM and AM/PM data for two power levels and the three cases of supply modulation can be seen in Fig.7.9, with the following interesting conclusions:

- In the case of lower output power, at P_{out}=22 dBm, both discrete supply modulation shaping functions give improvement in AM/AM distortion, as seen in Fig.7.9a-7.9b.
- Further, the adaptive shaping function (ASF) SM case offers benefits over the SM case for AM/AM, flattening out the gain response. The AM/PM distortion is also reduced for the ASF SM case, while Fig.7.8a shows simultaneous improvement in efficiency.

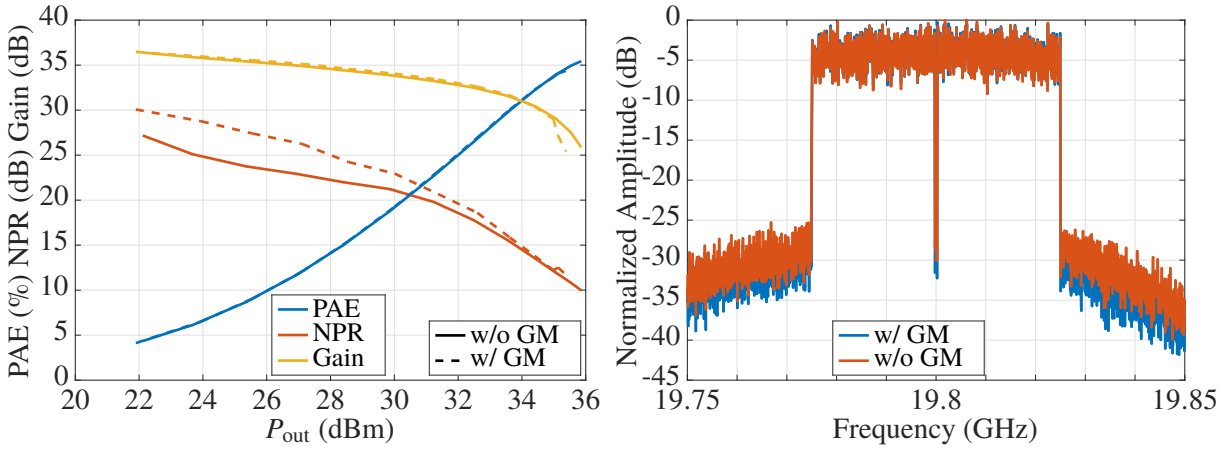
- At higher drive levels SM and ASF SM result in the same shaping function so only one case is shown.
- In the case of higher output power, P_{out}=28 dBm, the AM/AM and AM/PM for the static static supply and discretized supply modulation are shown in Fig. 7.9c-7.9d, with clear improvement in gain amplitude linearity when the PA is supply modulated.
- SM reduces gain variation when compared with the static supply case, but this does *not* come at the expense of efficiency, which is increased as shown in Fig.7.8a.
- This reduction in gain variation is complemented by a rise in phase variation as predicted by static measurements. At this power level, the NPR for the supply-modulated case exceeds the NPR for the static supply case.

For P_{out} >24 dBm the linearity of the static and SM cases are virtually identical while SM increases the efficiency by 9pp. It is shown that in back-off the shaping function between the drain supply and input power can be improved by adapting the SF to account for the actual voltage swing at the amplifier input. This is especially relevant in a DSM where the selected discrete voltage levels determine the resolution of the tracking function.

7.4 50 MHz Gate Modulation Testing

7.4.1 Shaping Function Design

The K-band amplifier is tested with gate modulation. The optimization routines developed in Section 5.4.1 are used to generate a continuous gate shaping function. The dynamic gate signal is provided to the amplifier through the bias board shown in Fig. 7.5b. For this implementation only the first stage of the three stage amplifier is gate modulated. The control signal is directly generated by the AWG which is connected to the bias board. The AWG signal is the AC coupled to amplifier gate through a 100 nF SMD blocking capacitor. The gate voltage offset is supplied through a BCR221 conical inductor from coilcraft. On the MMIC a 50 Ω resistor is connected to a 50 pF capacitor to ground providing a good low frequency termination for the AWG.



(a) (b)

Figure 7.10: (a) Measurement results for gate modulation of a 50 MHz signal. Gate modulation improves NPR over a static supply without degrading PAE or Gain. (b) Output spectrum with and without gate modulation at P_{out}=28 dBm

7.4.2 Results

The optimized gate shaping function is used to realize an improvement in NPR as seen in Fig. 7.10a. The NPR improvement is 3 dB or greater for power levels less than 28 dBm gradually reducing until gate modulation gives approximately the same performance as a static supply, for power levels above 32 dBm. Gate modulation has no effect on PAE or Gain up to 35 dBm output power. If a 25 dB NPR is desired with gate modulation the amplifier can be driven 4 dB deeper into compression (from P_{out}=24 to 28 dBm) improving efficiency from 7 to 15 %. For NPR specifications less than 20 dB this method offers little benefit over a static supply. More broadband signals were not tested due to bandwidth limitations in the gate modulator. The spectrum at P_{out}=28 dBm can be seen in Fig. 7.10b.

7.5 Distortion Mitigation in DSM

Based on the characterization results from Section 7.1 the amplifier is tested for higher bandwidth signals than previously reported (50 MHz). This testing is inhibited by two factors in the test setup. Firstly the multi-level drive board cannot support pulse widths lower than 8 ns. Secondly the VSA cannot receive IQ data for a signal with greater than 140 MHz bandwidth. The pulse widths limitation means that the DSM

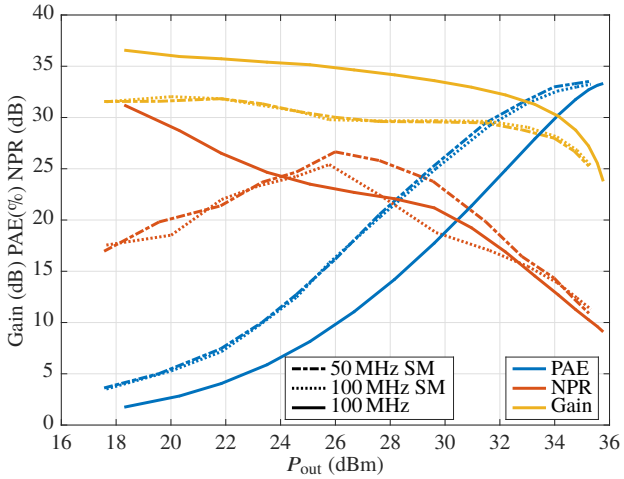


Figure 7.11: Measurement results for three cases: supply modulation of a 50 MHz signal, supply modulation of a 100 MHz signal, and a static supply for a 100 MHz signal. The 100 MHz supply modulation case shows a degradation in NPR while maintaining gain and PAE compared to the 50 MHz case.

control signal needs to be modified from the ideal discretization of a continuous SM shaping function for higher bandwidth signals. To prevent signal clipping for short, high amplitude pulses, the drain supply pulses for these higher amplitude levels are stretched to comply with the maximum switching clock [22, 123, 126].

With these limitations in mind testing is done with both a 50 MHz and 100 MHz signal with a SF based on 4 uniformly distributed drain voltages between 10 and 20 V. The results of this testing are shown compared with a static supply in Fig. 7.11. PAE and gain are identical (< 0.1 pp variation in PAE; < 0.1 dB variation in gain) for the SM cases. Linearity on the other hand matches in backoff $P_{\text{out}} < 25$ dBm but deviates between 26 and 32 dBm. In backoff the 4 level DSM is behaving similarly to a static supply (10 V) with rare switching events. In the higher output power regions the same is happening with the DSM behaving as a static supply (20 V) with rare switching events. The region in the middle corresponds to the area where switching transitions are happening in the middle of the PDF of the signal. With an infinite switching speed this would not be problematic, however the test bench used is limited to a 8 ns pulse width clock (as discussed in Section 7.2).

The non-ideal switching incidents can be visualized by plotting the estimated probability density function (PDF) of the signal amplitude separated for the discrete drain voltages levels V_{D}, as shown in Fig. 7.12. The PDF for a 10 MHz signal can be seen in Fig. 7.12a which approaches an ideal case; the 4 discrete voltage

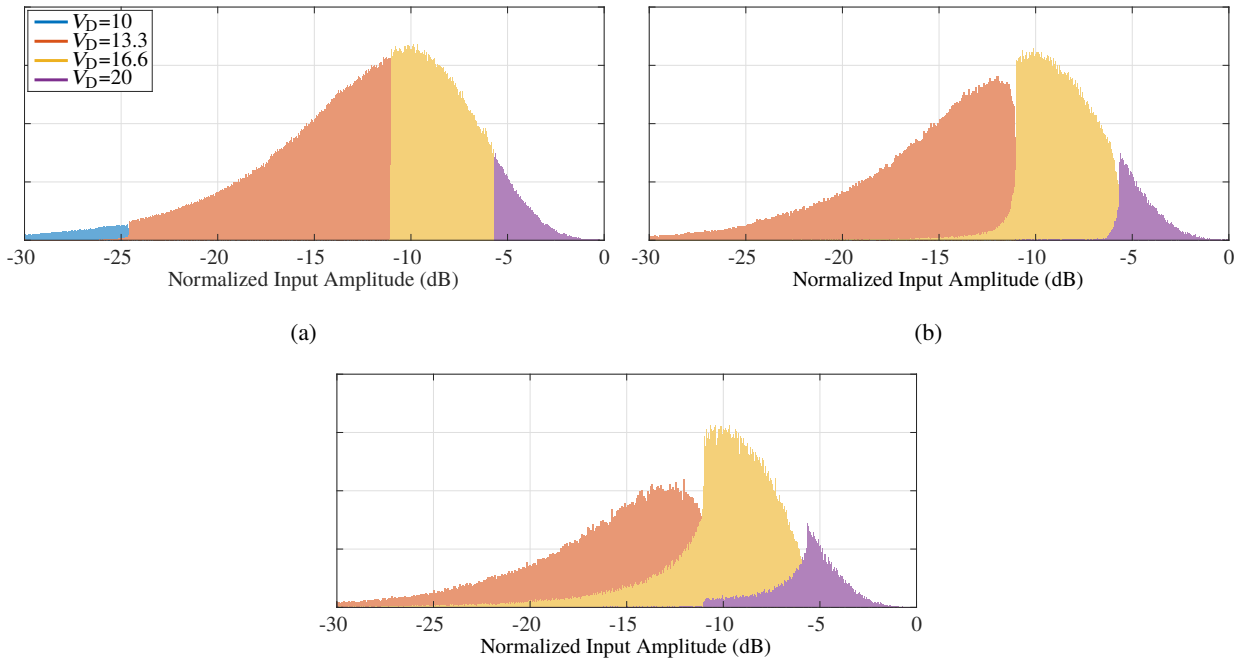


Figure 7.12: Probability density functions (PDF) of different V_Ds for P_{in}=-2 dBm. This is shown for (a) a 10 MHz signal, (b) a 50 MHz signal, and (c) a 100 MHz signal. It can be seen that as the signal bandwidth increases the minimum pulse width of the DSM (8 ns) results in the different V_D values blending together.

levels are clearly separated from one another and the overall shape resembles a continuous PDF. Increasing the signal bandwidth to 50 MHz, seen in Fig. 7.12b, causes a deviation from this ideal case. At the low end V_D=10 V is absorbed into the higher voltage levels. At the other transition points the PDFs of the voltage levels overlap. This means that the higher (non ideal) voltage will be used for lower input power levels than intended. Moving to a 100 MHz signal bandwidth the previously discussed issues become exacerbated, seen in Fig. 7.12c. There is now a large amount of overlap between the voltage levels, to the point that the envelope of the individual PDFs no longer resemble the shape of the original signal PDF.

This effect from reduced switching speed DSM performance is important, but it is not the only cause of disortions. Measurements show the emulated 100 MHz signal still outperforms the actual 100 MHz signal in terms of NPR. From this we can assume that there are other mechanisms that increase distortion for discrete supply modulation.

To further analyze this issue, two cases with a 50 MHz signal were tested. In one case a 8 ns pulse width

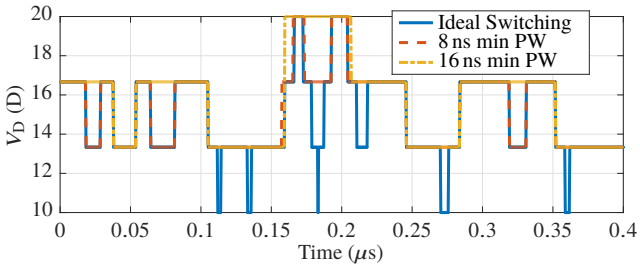


Figure 7.13: Time domain drain voltage waveforms for discrete supply modulation of a 50 MHz noise-like signal with an infinite switching speed, a minimum pulse width of 8 ns and 16 ns.

is used while in the other case a 16 ns minimum pulse width is used to emulate the 8 ns case for a 100 MHz signal. This allows time domain data capture with the bandwidth-limited VSA. The drain voltages used for the two cases compared with the ideal drain waveforms can be seen in Fig. 7.13. We note that the increased pulse widths signals cannot follow the short pulses to low supply levels. In the shown time frame the lowest drain voltage level is only used by the ideal switching trajectory. The differences between the 8 ns and 16 ns minimum pulse width signals are most prominently seen in the transitions between levels two and three.

AM/AM and AM/PM results for those measurements are shown in Fig. 7.14 with Fig. 7.14a-7.14b showing the 50 MHz results with a 8 ns minimum pulse width results and Fig. 7.14c-7.14d showing the 50 MHz with a 16 ns minimum pulse width (emulating a 100 MHz signal) results. For the 8 ns case, a clear distinction can be seen between the 4 voltage levels. For this power level (30 dBm) and minimum pulse width, the lowest voltage level is effectively unused. The composite signal trendline follows the individual trendlines for each voltage during there respective on region. For the 16 ns case there is a thickening of the AM/AM and AM/PM time domain data as compared to the 8 ns case. Additionally it can be seen that the composite trendline deviates from the individual voltage trendlines, indicating that the imperfect switching transitions have a non negligible impact on the AM/AM and AM/PM.

One obvious mechanism is switching noise introduced by the discrete nature of DSM. While shaping function design is meant to minimize the gain step between each voltage level a rapid transition between those steps remains. A results of this is added broadband noise as seen in Fig. 7.15 for a 10 MHz signal. The data is gathered and then the original signal is subtracted out leaving only the error signal. The static supply distortion drops down to the receiver noise-floor within a 40 MHz bandwidth. Conversely in the supply

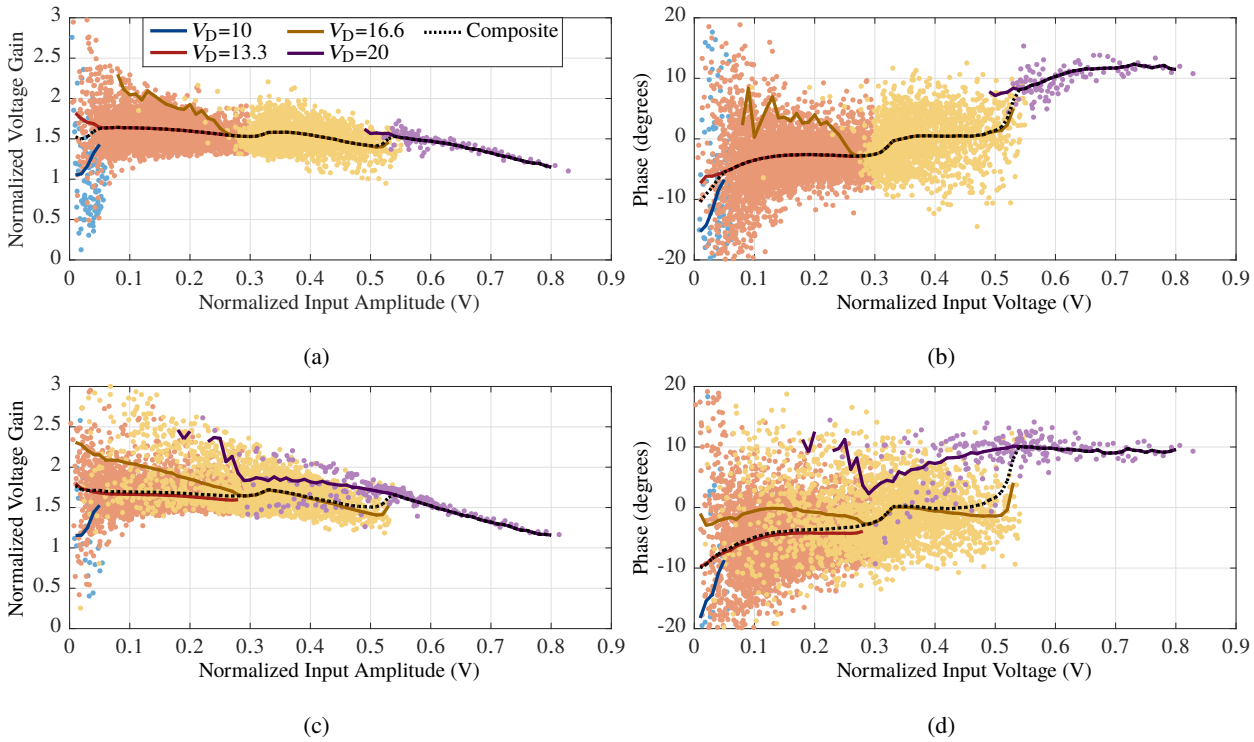


Figure 7.14: Measured supply modulation performance at 19.8 GHz for a minimum minimum pulse width={8,16} ns showing (a,c) AM/AM and (b,d) AM/PM, respectively, for a 50-MHz NPR for P_{in}=-2 dBm and P_{out}=30 dBm. Points are colored based on which drain voltage level V_D is active for a given input. The lower minimum pulse width case has a tighter spread of points and the individual levels are clearly separated. For the higher minimum pulse width case the the points are more spread out and the different levels blend together. The composite trendline also is not as well matched to the individual level trendlines.

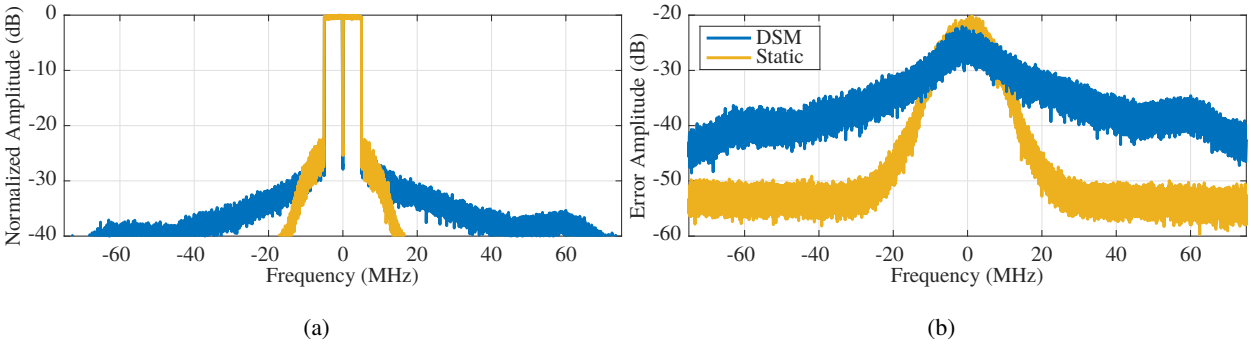


Figure 7.15: (a) Spectrum at P_{out}=28 dBm with a 10 MHz NPR signal for a static supply and discrete supply modulation. (b) Spectrum with original NPR signal subtracted, showing more clearly the distortion.

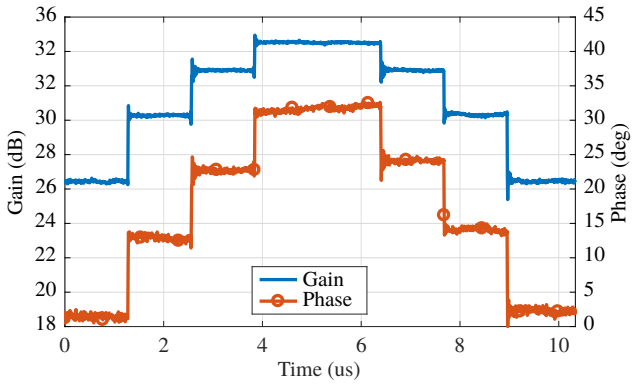


Figure 7.16: Gain and phase of the amplifier driven with a P_{in}=-2 dBm CW signal at 19.8 GHz. The drain is modulated with a staircase using 4 equally spaced voltages between 10 and 20 V.

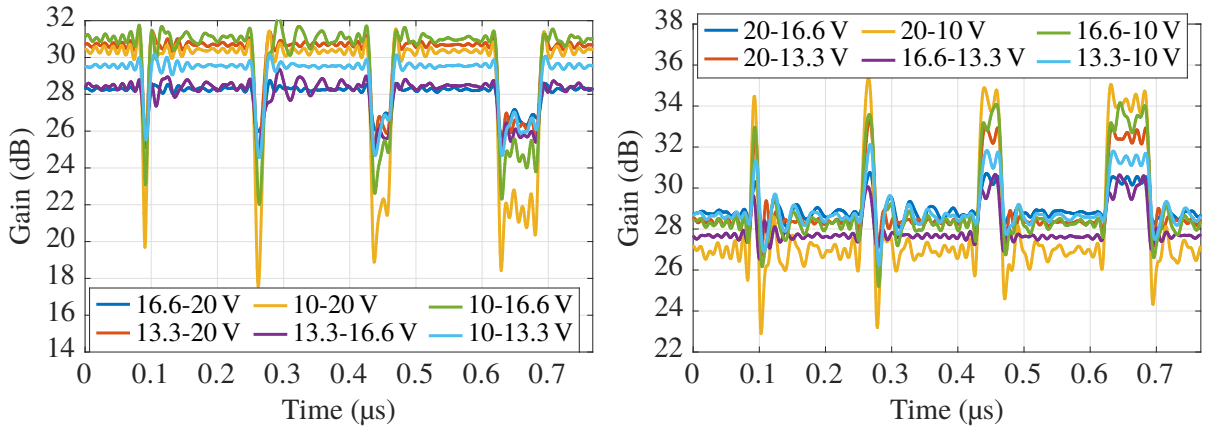


Figure 7.17: Gain of the amplifier driven with a CW signal for P_{out}=29 dBm. Pulse train with four pulses of lengths={8, 16, 32, 64} ns each separated by a 60 ns spacing is modulated onto the drain of the amplifier. (a) Gain switching to a lower voltage during pulses (b) Gain switching to a higher voltage during pulses. This data is upsampled to a 1.25 GHz clock rate during time alignment.

modulation case the error signal is still 10 dB above the receiver noise-floor within the 150 MHz bandwidth. It can be seen that the in-band distortion is actually lower for the DSM case meaning that an in band metric like NPR will improve while an out-of-band metric like ACPR will degrade.

In the time domain this distortion can be visualized as in Fig. 7.16 where the amplifier is driven with a CW signal and it's drain is modulated. There are two things of note here. One is the jump in gain and phase during the transitions from voltage level to level. While the shaping functions in this work are designed for flat gain, they do not account of phase. This can be observed in Fig.7.14 where the amplitude is flat

across input voltage while there is an approximately 10 deg variation in phase for each level transition. These discontinuities in performance can lead broadband spectral content, as in the case of a square wave or step function. Also of note is the ripple at each voltage transition. Upward transitions tend to ripple upwards and then the damped oscillation moves to a steady state, downward transitions do the opposite. The ripple frequency being introduced during each transition varies from 30-80 MHz. This ripple has an impact on linearity, especially when the signals being modulated become more broadband and the settling time is longer than the average pulse-width duration. The fall times during transitions are less than or on the order of one sample (6.4 ns) while the rise times tend to vary between one and two samples (6.4-12.8 ns). The rise and fall times are better seen in Fig. 7.17 for 4 different pulse widths modulated onto the drain. The speed of the transitions creates difficulty in capturing their effects on amplifier performance. Additionally some levels have larger ripple during transitions (ie. 10-16.6 V in Fig. 7.17a) which may be indicative of an imperfect alignment between the two switching events. It should be noted that the bandwidth of the receiver limits the accuracy of these measurements as the spectral content created by the switching transitions can exceed 1 GHz in bandwidth.

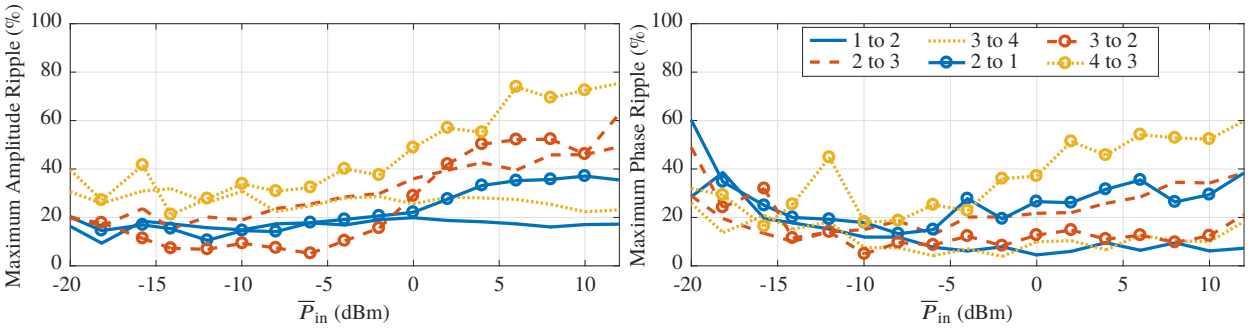
These strategies were investigated experimentally by increasing the minimum drain voltage of the DSM. Also examined is the use of the 4-level DSM as a 3 and a 2-level DSM. This is done to further reduce switching events and thus the effect of transients on the amplifier output. It should be noted that the supply modulator is more efficient for fewer levels as unused levels will not draw driver current.

To quantify the amount of variation possible during switching transitions the ripple is investigated during transitions. We define the relative amplitude ripple betwen levels m and n as:

$$Ripple_{\mathrm{A},m,n} = \frac{|\hat{V}_{\mathrm{RF}m,n} - \overline{V}_{\mathrm{RF}n}|}{|V_{\mathrm{RF}n} - \overline{V}_{\mathrm{RF}m}|}, \tag{7.1}$$

where $\hat{V}_{\mathrm{RF}m,n}$ is the peak RF amplitude deviation in the level m to n transition, and $\overline{V}_{\mathrm{RF}i}$ is the average RF amplitude at level i.

This amplitude ripple and a similarly defined phase ripple can be seen in Fig. 7.18. The ripple during transitions, particularly during downward amplitude transitions, is up to 70 %. This means that during this transient the amplifier will be behaving as though it has almost half the desired gain level and will impact



(a) (b)

Figure 7.18: Relative amplitude and phase ripple for each of the 6 switching transitions of Fig. 7.16 as a function of P_{in}. (a) voltage amplitude ripple, (b) phase ripple.

the linearity. More switching incidents will have a larger effect on dynamic amplifier performance.

With these key distortion processes in mind we develop strategies that will reduce distortion caused by DSM for more broadband signals:

- Moving the switching points away from the peak probability point of the signal as seen in Fig. 7.12. This could involve making changes the SF used.
- Increasing the minimum voltage level for supply modulation (>10 V). This will trade off efficiency improvement and linearity degradation.
- Reducing the number of DSM levels from 4 to 3 or 2. This should trade-off a reduction in switching events (and thus the effects of transients on the signal output) with a reduced DSM resolution.

7.6 Dynamic Amplifier Testing

The 100 MHz signal case from Fig. 7.11 is reexamined making use of a higher minimum V_{D}. In this case it is selected to be 16 V. This is done because this level gives the best tradeoff between linearity and efficiency, improving the linearity over that of a static supply. Measurements are then conducted with the existing supply modulator operating as 2-, 3-, or 4-level DSM, the results are in Fig. 7.19. From this it can be seen that all three cases give the same gain and raw PAE. With driver losses taken into account the PAE degrades more with the number of levels. Looking at the linearity it can be seen that the 2-level has the worst linearity,

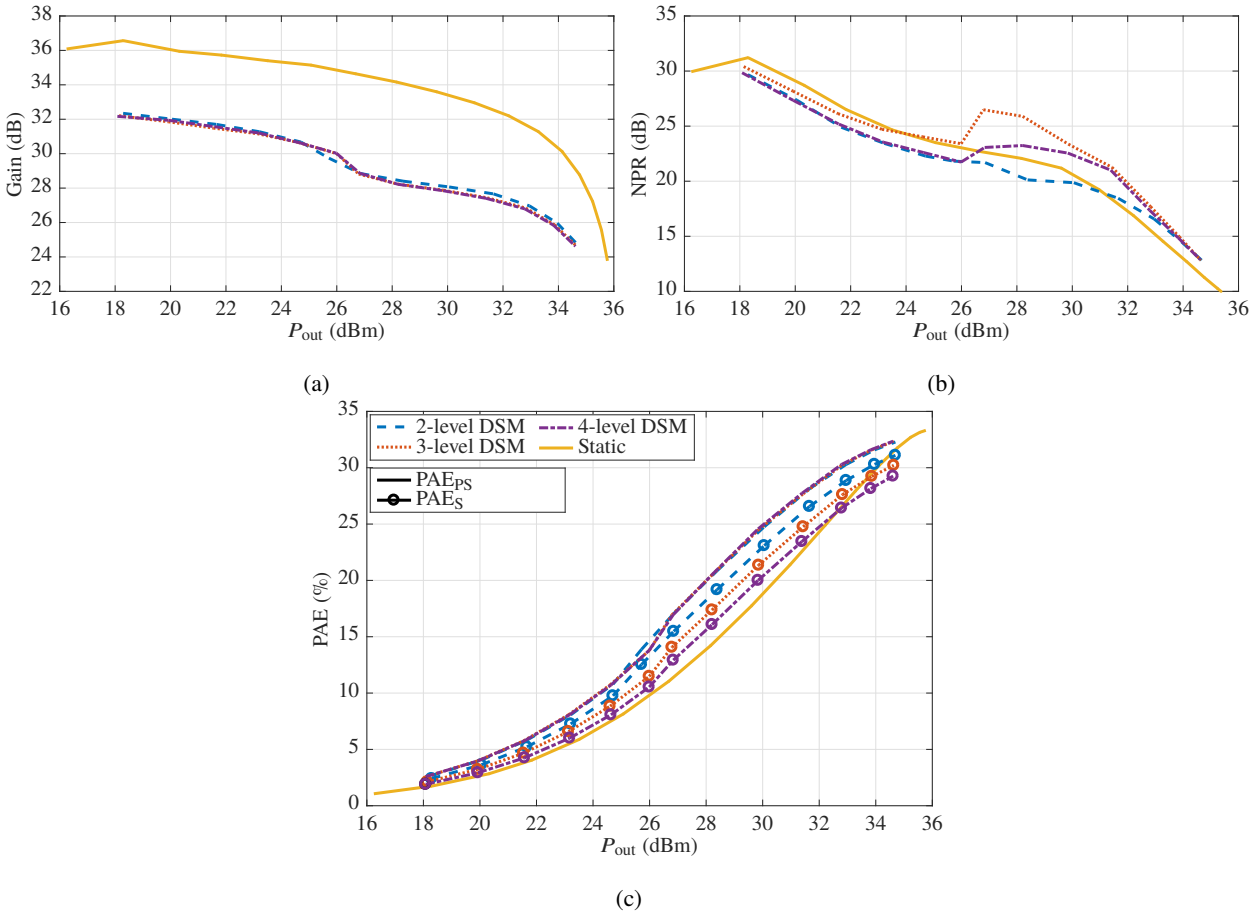


Figure 7.19: Amplifier performance for a 100 MHz NPR signal at 19.8 GHz for a static supply and DSM with 2-, 3-, and 4-levels with a mininum drain voltage of 16 V and a maximum drain voltage of 20 V. Performance is shown over P_{out} for (a) PAE (efficiency measurements without driver losses are lines while those including driver losses have markers), (b) gain, and (c) NPR.

the 3-level has the best, and the 4-level has an intermediate level. Between P_{out}=26 and 33 the 3-level DSM outperforms static supply linearity, at points by 3 dB. This is coupled with a 6-7pp improvement in PAE without accounting for driver losses. Taking into account driver losses halves this benefit. If a specific NPR is desired the amplifier could be driven to a higher (1-5 dB) P_{out} level while maintaining the same linearity of a static supply further improving efficiency. The spectrum for P_{out}=28 dBm is shown in Fig. 7.20.

The degradation of the 2-level case is to be expected as the two voltage levels have to much variation between them leading to an AM/AM and AM/PM that do not match a flat response. The difference between the 3- and 4-level case is more ambiguous. Three level supply modulation has fewer switching events and thus should results in fewer transients than a 4-level DSM. It will also, given our small range of voltages do

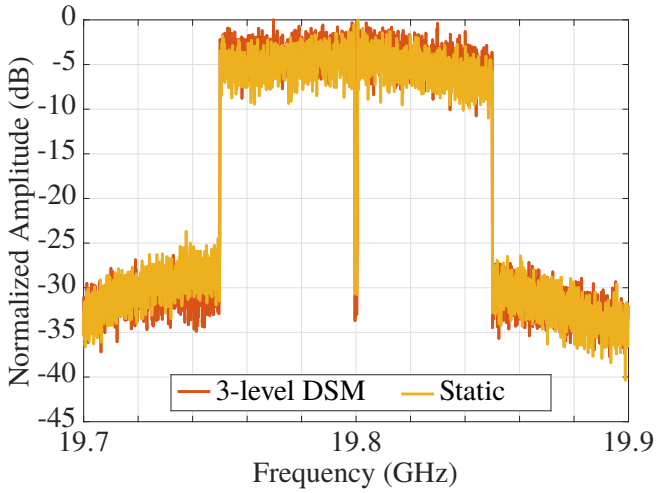


Figure 7.20: Amplifier performance for a 100 MHz NPR signal at 19.8 GHz for a static supply and DSM 3-levels with a minimum drain voltage of 16 V and a maximum drain voltage of 20 V. Performance is shown for P_{out}=28 dBm.

a much better job of tracking the signal than the 2-level case. This does not mean that a 3-level tracker is always the optimal case. This improvement is coupled with many different factors, i.e. the speed limitations on the drive board limiting the switch speed of the DSM and the parasitics of the interconnect between the DSM and PA. If an infinite switching speed were possible a greater number of levels will result in the better linearity, though this might at the cost of DSM efficiency and system complexity.

With this in mind testing was next done on a 250 MHz signal. Because the 3-level performed best on the 100 MHz signal it was used with the 250 MHz signal. The minimum V_D is varied from 15 to 17 volts. It can be seen that all three cases offer an improvement in PAE with the highest efficiency improvement corresponding to the lowest minimum V_D. The back-off gain varies as a function of drain voltage with the highest drain voltage resulting in the highest average gain. Linearity also varies as a function of drain voltage, with the 15 V SF behaving the worst and the 17 V consistently exceeding or equalling the performance of the static supply for $P_{out} > 26$ dBm. For this case (17 V) the efficiency improves by 5pp not factoring in DSM driver losses and 2pp including driver losses. The spectrum for P_{out}=28 dBm is shown in Fig. 7.22.

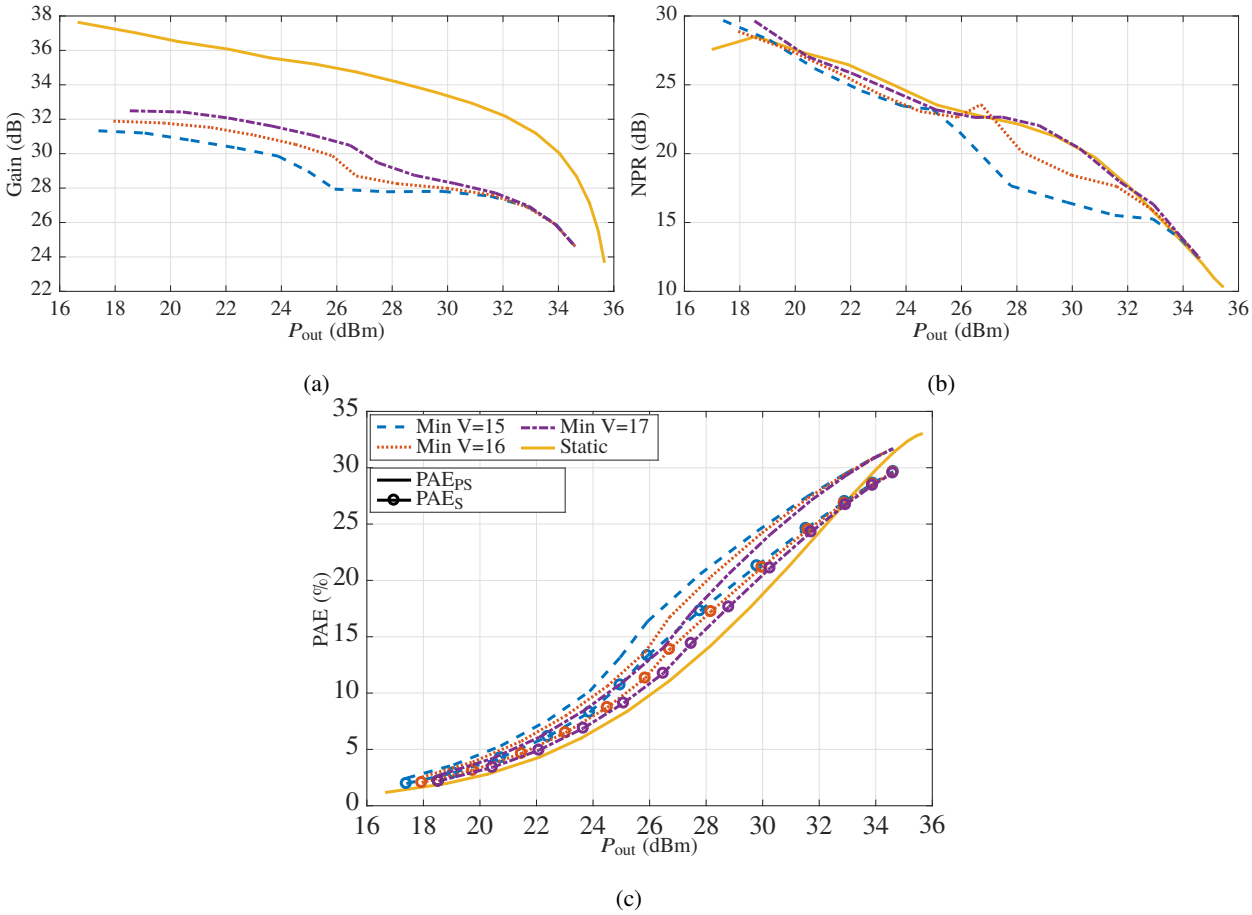


Figure 7.21: Amplifier performance for a 250 MHz NPR signal at 19.8 GHz for a static supply and DSM a 3-level DSM using a minimum voltage of 15,16, and 17 V for a maximum voltage of 20 V. Performance is shown over P_{out} for (a) PAE (efficiency measurements without driver losses are lines while those including driver losses have markers), (b) gain, and (c) NPR.

7.7 Summary

A three-stage K-Band GaN MMIC amplifier is tested and characterized at 19.8 GHz using a DSM. The PA is tested with noise-like signals at 50, 100, and 250 MHz. Through effective shaping function design a simultaneous improvement in efficiency and linearity is possible. This is achieved by reducing the number of switching events to account for a limited switching speed of the DSM by reducing the number of drain voltage levels and raising the lowest drain voltage level.

For a 100 MHz signal with a 3-level DSM the NPR is improved by as much as 3 dB when compared to static supply operation between P_{out}=26-32 dBm. At the same time, average efficiency is improved by 6-7 pp

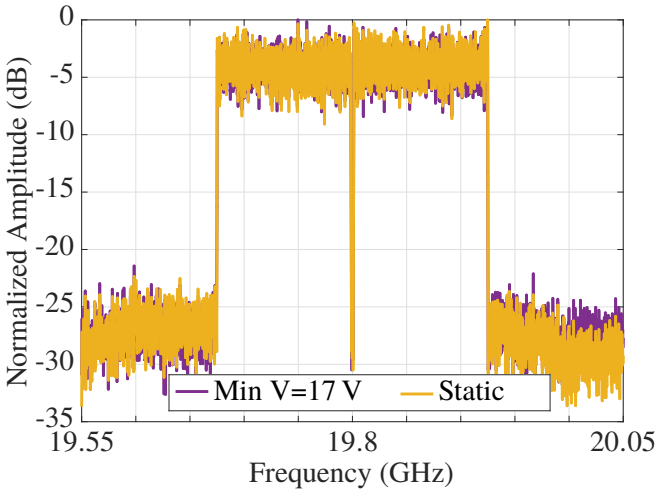


Figure 7.22: Amplifier performance for a 250 MHz NPR signal at 19.8 GHz for a static supply and DSM 3-levels with a minimum drain voltage of 17 V and a maximum drain voltage of 20 V. Performance is shown for P_{out}=28 dBm.

without driver losses and by 3-3.5 pp factoring in driver losses. For this DSM configuration fewer switching levels mean a more efficient DSM. Applying the same methods to a 250 MHz bandwidth signal allows to match the NPR performance of the static PA while improving efficiency by by 5pp without driver losses taken into account.

We show that the shaping function design can be used with discrete supply modulation to improve amplifier linearity without the need for DPD. This method is successfully applied for in-band distortion metrics such as NPR. Due to distortions introduced by switching transition's an improvements in ACPR is not implicit from these results. To the best of the authors knowledge, this is the first demonstration of supply modulation with an efficient GaN tracker for a 250 MHz bandwidth signal without a linearity penalty.

The details presented in this chapter are contained in publication [75, 127].

Chapter 8

Conclusions and Future Work

Contents

8.1 Summary and Contributions

This thesis develops testing methods for RF power amplifier transmitters with broadband supply modulation. The goal of the research is to enable efficient amplification of signals with >100 MHz modulation bandwidths while maintaining linearity. A summary of the results of the thesis work is presented below, highlighting the original contributions.

- A method for efficiently amplifying multiple, simultaneous, widely spaced signals is addressed. The signals can be spaced arbitrarily in bandwidth with individual bandwidths on the order of tens of MHz. This scenario applies to communications with some forms of carrier aggregation and electronic warfare, though the overall bandwidth will be different in the two cases. The composite signal bandwidth in these cases is roughly that of the widest signal spacing, resulting in a signal that is very difficult to amplify efficiently and linearly. While standard supply modulation or envelope

tracking could make the PA more efficient, the supply would be inefficient resulting in a poor overall efficiency. The thesis shows that applying a combination of power tracking and sum-of-envelopes tracking reduces the supply modulation bandwidth from about 5 times the bandwidth of the signal spacing to approximately that of a single signal, making efficient amplification possible. Additionally, the thesis shows that a simple digital pre-distortion (DPD) can be applied, resulting in a linearity that meets current standards. Specifically, this is first demonstrated on an X-band MMIC GaN PA tested with three dynamic 10 MHz unequal-power signals spaced in a ~200 MHz bandwidth. After this initial demonstration, an octave-bandwidth 2-4 GHz GaN hybrid PA is designed with an efficiency above 50% across the band, and efficient and linear amplification demonstrated for two 10 MHz LTE-type signals with a 800 MHz spacing. These results are reported in [55, 70, 74].

- In order to further investigate nonlinearities in supply-modulated PAs, an X-band GaN MMIC is evaluated. The existing two-stage MMIC PA was fabricated in a process with considerable current and gain collapse at lower voltage levels, resulting in strong nonlinearities. In order to mitigate current collapse under dynamic supply operation, gate modulation can be applied. It is shown in the thesis that a two-stage PA has advantages for this linearization technique, as the two separate gate biases can be used to independently control the gain magnitude and phase. This method is applied to LTE and NPR signals with discrete drain supply modulation. The thesis demonstrates 10 MHz and 20 MHz signal amplification with linearity better than in the case of a static supply coupled with an efficiency improvement by 10-20 percentage points. These results are reported in [22, 76–79, 103].

- A custom amplifier is designed to investigate supply modulation at an higher frequency and increased modulation bandwidth. The three-stage 18.5-24 GHz MMIC PA is made using the Qorvo 150-nm GaN on SiC process. The MMIC shows PAE 40 % with 4 W output power and a saturated gain over 25 dB over a ~25 % fractional bandwidth. The drain bias lines of the three stages are separated to allow investigation of supply modulation of the different stages. Additionally, the capacitance on the drain supply lines is minimized for high-bandwidth tracking, while ensuring stability. The design details and measurement results are reported in [57, 80].

- The K-band MMIC is next tested with a 4-level GaN discrete supply modulator. After determining the tradeoff in modulation of different PA stage combinations, supply modulation for a continuous signal is demonstrated for bandwidths larger than previous work, with NPR signals of 50, 100, and 250 MHz bandwidths. Due to limitations in the control signal speed, techniques for reducing switching speed requirements between discrete voltage levels of the dynamic supply were developed. To the best of the authors knowledge, these are the highest bandwidths for supply modulation demonstrated to date with competitive efficiencies and linearity. The results are detailed in [75, 127].

The main contributions of this work are listed as follows:

- Supply modulation for multiple widely-spaced signals is demonstrated with an efficiency enhancement for signals spacings up to 800 MHz. This done through a combination of power and sum-of-envelopes tracking, significantly reducing supply modulator speed requirements. Linearization is demonstrated using a simple digital predistortion maintaining linearity while improving efficiency.

- A three-stage broadband (~25 % fractional bandwidth) 4 W K-band GaN MMIC PA with over 40 % PAE is designed for supply modulation. To the best of the authors knowledge, this PA exhibits state-of-the-art performance in this frequency and power range.

- A test bench for supply modulation, as well as calibration methods for the bench are developed. Specifically, a technique for calibrating ac and dc power measurements is developed in order to obtain accurate efficiency measurements with a linear tracker. Additionally, a method for aligning the RF and LF path using a perturbation in the RF PA output is developed. The technique is effective even if the signals are severely misaligned and only requires one measurement.

- Dynamic effects of the amplifier are not captured through static characterization and thus traditional shaping function design does not work. Using dynamic characterization and modelling, these effects are captured and mitigated with gate modulation resulting in improvement in both linearity and efficiency.

- With a finite switching speed, discrete supply modulation degrades for broadband signals. Reducing

the number of switching incidents through using fewer discrete levels and a smaller voltage swing can mitigate these effects so that both efficiency and linearity enhancement can still be realized.

The methods developed in this work for multi-signal power tracking provide a means for efficiency enhancement of broadly spaced signals. For broad instantaneous bandwidth application discrete supply modulation provides an effective route to efficiency enhancement. Though this work has focused on supply modulation of reactively matched power amplifiers, supply modulation can be used in conjunction with load-modulated amplifiers for further efficiency enhancement [123, 128, 129].

8.2 Future Work

This thesis contributes in the areas of GaN MMIC PA design, integration of MMIC PAs with supply modulators, both digital and analog linearization for broadband signals, and development of a test-bench specifically intended for supply modulated transmitters. Results in each of the sub-topics point to interesting and promising areas for future research, summarized below.

8.2.1 High-Efficiency K-band MMIC PA with static supply

Though this work has focused on efficiency enhancement through supply modulation there are cases where, even for communication signals, a traditional reactively matched PA would be sufficient. As part of an ongoing collaboration with Lockheed Martin an efficient PA was designed for linearity and efficiency. The linearity spec was such that the amplifier could be driven close to saturation and the specification still met. For this a high efficiency amplifier is designed at K-Band in the Qorvo 150 nm process.

The amplifier has returned from fabrication and is waiting to be tested, seen in Fig 8.1a as a bare die and Fig 8.1b packaged. Simulated performance is summarized in Fig. 8.1c. Future work will involve full testing of the chips to evaluate the amplifier for planned use in a space-born system.

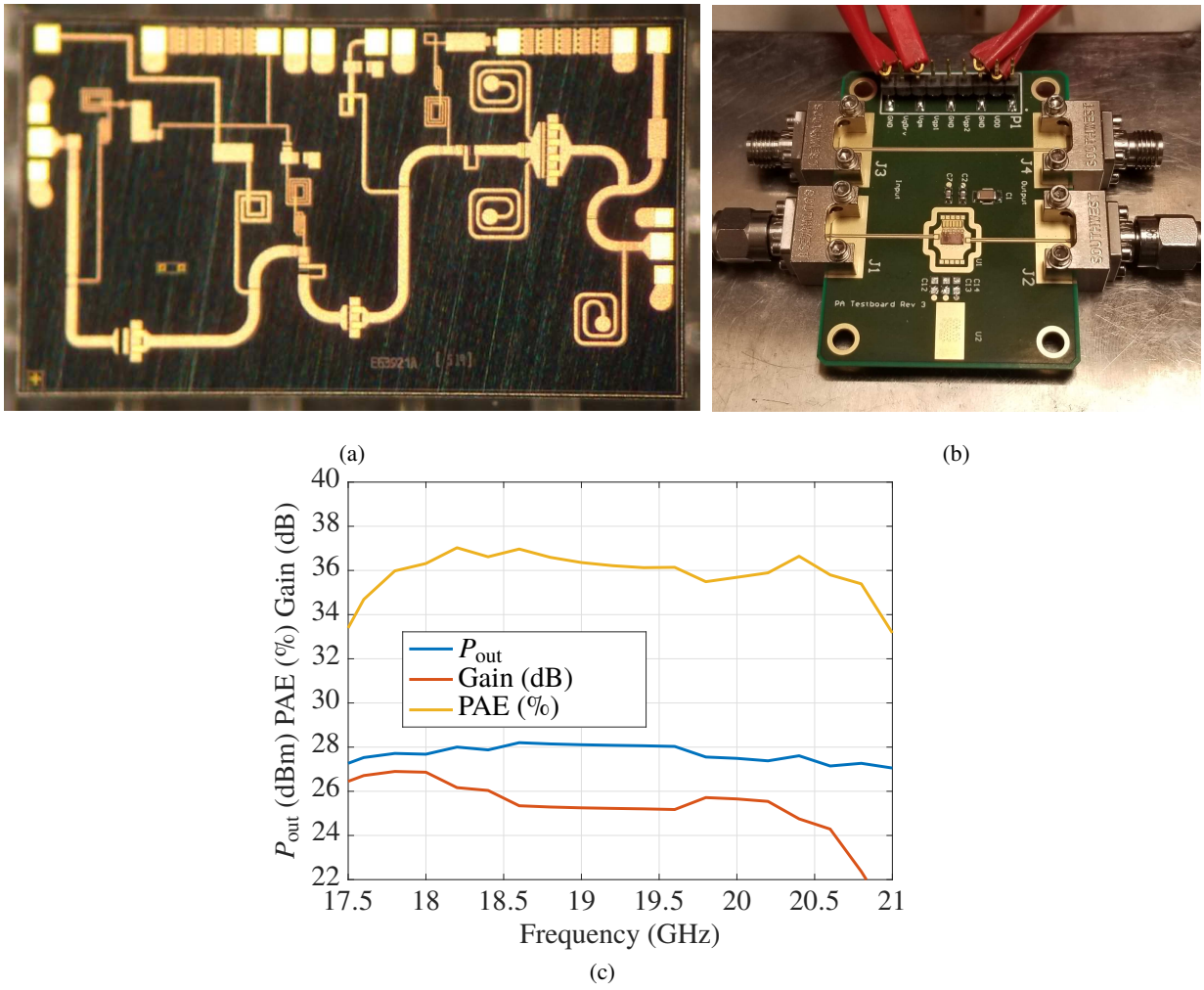


Figure 8.1: (a) Photograph of fabricated 2x3.5mm K-Band GaN MMIC designed in Qorvo 150 nm process. (b) Die mounted, packaged, and bonded. (c) Simulated results using a Qorvo nonlinear model, including full-wave EM simulations, showing over frequency performance for a NPR of 14 dB.

8.2.2 Integration of Supply Modulated Transmitters

The research in this thesis demonstrates that supply modulation, combined with shaping function design and analog or digital linearization, can result in efficient and linear amplification of signals with broad instantaneous bandwidths and PAPRs. The efficiency and linearity demonstrated, with PAs at carrier frequencies ranging from 2 to 20 GHz, shows state of the art results. Transmitters with supply modulation have unique requirements for the PA, dynamic supply, and control circuitry. The RF power amplifier needs to be efficient over a range of supply voltages, and stable without large bypass capacitors on the drain supply

line, which would filter the higher frequency components of the signal determined by the shaping function. Additionally, the efficiency benefit of supply modulation does not exist at the transmitter level without an efficient supply modulator circuit, which simultaneously needs have a wide large signal bandwidth and provide ideally a very low impedance at the amplifier drain. Finally, digital signal processing is required to align the two input signals to the amplifier, provide feedback for linearization, and generates the control signals for the supply modulation circuit.

8.2.2A RF-Input SM

In this work amplifiers are designed which are integrated with supply modulators, however the actual control scheme for the setup are absorbed into a test bench. While this allows for quick testing of different supply modulation methods it also obscures the actual processing power that would be needed to implement the digital system. The goal of any efficiency enhancement technique should be to improve on what is already available. The supply modulated PAs developed in this thesis are not at a stage where they can be implemented simply as drop-in circuits for existing transmitters. At this point the 'gold standard' for an amplifier used with a modulated signal is a Doherty. In it's simplest implementation, the features that make a Doherty so attractive are the fact that is in an RF input RF output amplifier. It requires no special control circuitry save the several bias voltages that are applied. In contrast, a supply-modulated PA requires a modulator and all required controls and is thus more complicated. An important topic for future work is to integrate the control circuitry with the PA and dynamic supply and to assess its impacts on efficiency and complexity. This does not necessarily mean a dedicated ASIC, as an FPGA implementation would be sufficient to give an idea of the energy consumption of such a circuit. While this is an old idea for continuous supply modulation [130], it would be of particular interest for the case of discrete supply modulation where drive signal generation is more complex. This is an excellent topic for future research.

8.2.2B GaN SM Topologies

To optimize system efficiency it is necessary to investigate new driver topologies for GaN integrated supply modulator circuits. Without complementary devices GaN gate drivers for switching supply modulators will

not be as efficient as those integrated in a different technology, despite speed benefits. Investigating more efficient driver technologies would go a long way in improving system efficiency. Additionally leveraging recent technological developments in heterogeneous integration [131] might make it practical to use a driver developed in a different technology that can be placed very close to a GaN power stage. For testing with a continuous supply modulator a linear tracker was used, but it would also be of interest to do testing with an integrated buck converter such as the ones described in [61].

Another topic for future work related to the supply modulator is an investigation of the effects of switching transitions on amplifier linearity during discrete supply modulation. If a model could be developed to capture the effects during switching transitions in amplifiers the main contributors to distortion could be better analyzed. This would be especially interesting for very high speed discrete supply modulation where switching transients are going to have a large impact on linearity performance. Additionally, it would be worthwhile to look at the trade offs of doing filtering at the outputs of the DSM for more narrowband applications, reducing some of the added distortions from the switching transitions and improving linearity. Besides transients during switching, performance variations between voltage levels have a large effect on out of band distortions. If device technologies could be optimized for reduced gain and phase variation as a function of supply voltage, some of the distortions could be mitigated [132].

8.2.3 Extending to Next-Generation Transmitters

Supply modulated PAs are “carrier agnostic" - assuming the supply modulator is capable of providing the correct voltage to the amplifier, it can be used with any PA regardless of RF carrier frequency. With the shaping function programmed in the digital domain, a flexible high-efficiency transmitter results. This initial work opens up possibilities for future research in supply modulation of multiple-frequency or broadband PAs, such as dual-band PAs and broadband PAs, such as a distributed architecture. Proving that supply modulation can give increased efficiency with linearity for these types of PAs could open new applications of this architecture as 5G bands and signals become better defined, as well as for various military communication scenarios.

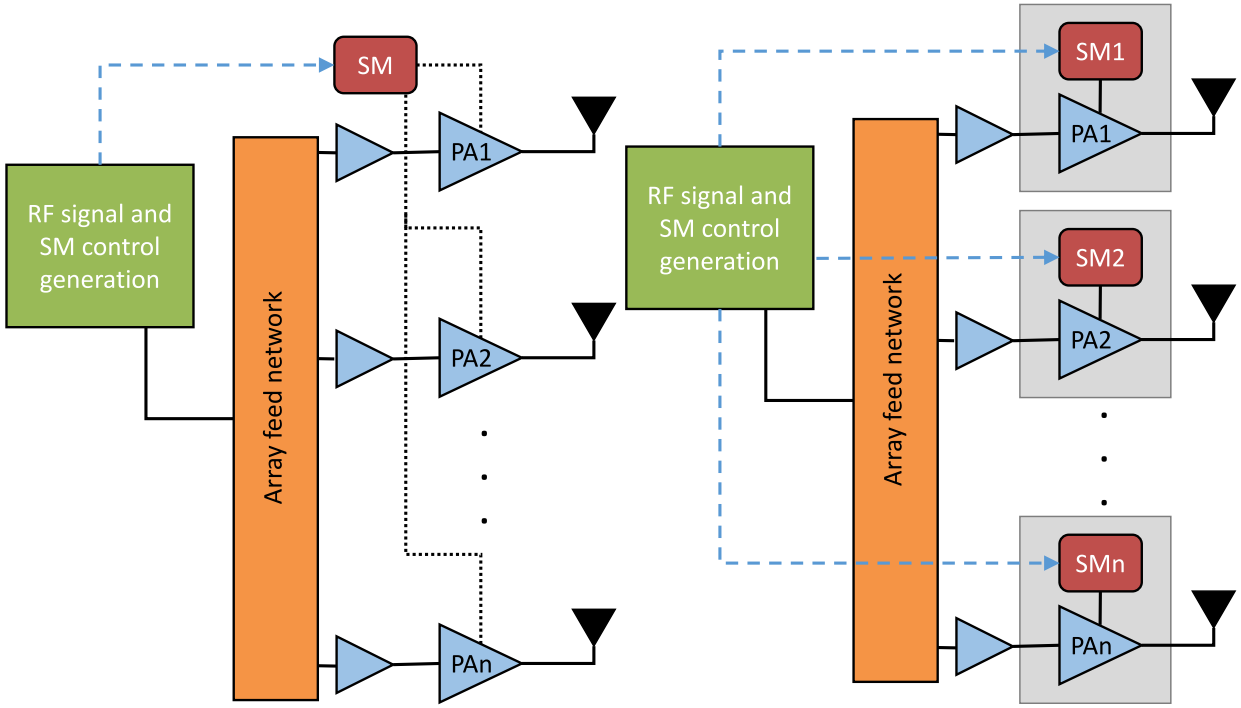


Figure 8.2: (a) A single supply modulator driving multiple phase shifted amplifiers. (b) A supply modulator distributed for each individual amplifier.

8.2.4 Extending to Phased Arrays

At the system level there are some questions of how supply modulation would be implemented in a phased array, which is investigated in [133, 134].

In this case, an investigation of tradeoffs associated with integrating a SM in each element (Fig 8.2b), in a sub-array or at the array level (Fig 8.2a) would be interesting and potentially useful. For phased arrays, which are thermally limited, the integration and associated power consumption of the control circuit needs to be critically evaluated. Using a single supply modulator would reduce size and system complexity by needing only one drive signal, but will most likely not give full performance benefits. On the other hand, using multiple supply modulators would give flexibility in the specific voltage level at each amplifier, allowing some radiation pattern control, but at the expense of increased system complexity and size.

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