Isotrap Pulsed IV Characterization of GaN HEMTs for PA Design

Gian Piero Gibiino, *Member, IEEE*, Corrado Florian, *Member, IEEE*, Alberto Santarelli, *Member, IEEE*, Tommaso Cappello, *Member, IEEE*, and Zoya Popović, *Fellow, IEEE*

***Abstract*— A pulsed characterization of gallium nitride (GaN) high-electron mobility transistors (HEMTs) under a controlled trap and thermal state is performed to evaluate the trapping-induced degradation in the actual operating conditions, corresponding to different classes of power amplifiers (PAs). Two state-of-the-art GaN-on-SiC technologies are evaluated: 0.15-μm Qorvo and 0.25-μm Wolfspeed HEMTs, with examples relative to class-AB, class-E, and supply modulated operation. It is shown that, in order to get an accurate device characterization, the measurements have to be performed by preconditioning the trap state consistently with the intended application.**

***Index Terms*— Gallium nitride (GaN) high-electron mobility transistor (HEMT), power amplifier (PA), pulsed characterization, trapping effects.**

I. Introduction

CHARGE trapping in gallium nitride (GaN) high-electron mobility transistors (HEMTs) is responsible for degraded output power, power-added efficiency (PAE), and linearity of microwave power amplifiers (PAs), especially at higher drain voltages [1]–[3]. Nevertheless, most transistor models do not include a global description of the trapping behavior for multibias PA operation. Due to the asymmetry in the time constants of charge capture and release [1], the trap state associated with large-signal operation can be controlled by the peak voltages on the gate (negative) and drain (positive). The double-pulse (DP) technique [2] uses the first of two consecutive pulses (namely, a prepulse $V_{G,\mathrm{PP}}$ and $V_{D,\mathrm{PP}}$ on the gate and the drain, respectively) to precondition the trap state to a target value, before the actual measurement pulse (v_G and v_D on the gate and the drain, respectively) is applied. In this way, the IV curves are measured under a controlled and fixed trap state (i.e., isotrap), representative of a specific operating regime. Such device characterization can be used to more accurately predict achievable PA performance in the design phase.

This letter presents results of DP characterization for two types of GaN-on-SiC microwave HEMTs: an 8×100 0.15-μm Qorvo and a 6×100 0.25-μm Wolfspeed (G28V4), shown in Fig. 1, and referred to as T1 and T2. State-of-the-art high power and high efficiency monolithic microwave integrated circuit (MMIC) PAs have recently been implemented in these processes (see [4]–[6]). Due to a smaller gate length, the Qorvo process [4] enables higher operating frequencies (30 vs. 18 GHz), whereas the Wolfspeed technology [5] delivers higher power density. The main process parameters are reported in Table I. Trapping-induced degradation is evaluated for HEMTs in operating conditions corresponding to different classes of PA operation.

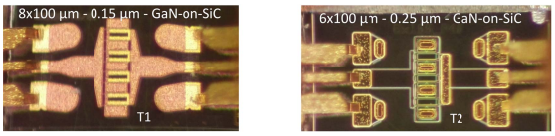

Fig. 1. Photographs of two GaN-on-SiC HEMTs: T1—8×100 μm^2 and 0.15-μm Qorvo and T2—6×100 μm^2 and 0.25-μm Wolfspeed. The main process parameters are reported in Table I.

TABLE I
MMIC Process Main Characteristics

Process	Qorvo 0.15 μm (T1)	Wolfspeed 0.25 μm (T2)
V_{GD}^{B}	$>$ 60 V	$>$ 120 V
I_{max}	1.15 A/mm	1.1 A/mm
I_{D}^{SS}	0.8 A/mm (at $V_D = 5$ V)	0.77 A/mm (at $V_D = 5$ V)
V_{TH}	-3.1 V	-3.1 V
v_G	-7 V to 1.5 V	-8 V to 2 V
P_{max}	4.5 W/mm	6.9 W/mm

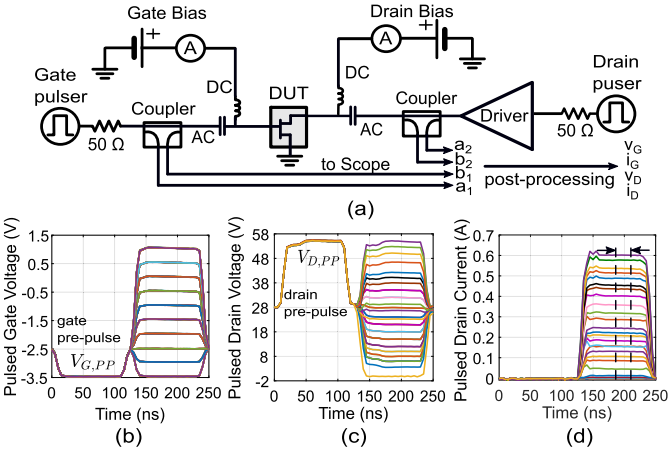

Fig. 2. (a) Block diagram of double-pulsed IV setup. (b) Pulsed gate voltage waveforms. (c) Pulsed drain voltage waveforms. (d) Pulsed drain current waveforms with the indication of the acquisition interval.

II. Double-Pulse IV Method

The measurement setup is shown in Fig. 2 along with acquired DP waveforms in time domain. A two-channel function generator is able to apply pulsed excitations with up

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G. P. Gibiino, C. Florian, and A. Santarelli are with the Department DEI "G. Marconi," University of Bologna, 40126 Bologna, Italy (e-mail: gianpiero.gibiino@unibo.it).

T. Cappello and Z. Popović are with the Department of Electrical Engineering, University of Colorado at Boulder, Boulder, CO 80309 USA.

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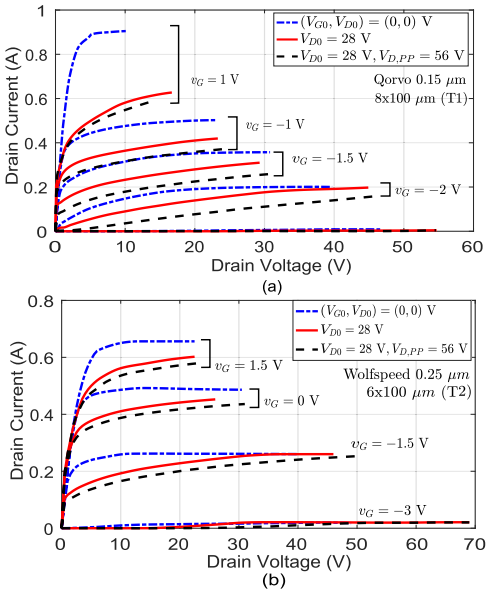

Fig. 3. Single-pulsed and double-pulsed [with $(V_{G,\mathrm{PP}}, V_{D,\mathrm{PP}}) = (-3.5, 56)$ V] IVs (i_D vs. v_D) from $V_{D0} = 28$ V compared against the benchmark reference IV pulsed from $(V_{G0}, V_{D0}) = (0, 0)$ V. (a) T1, $V_{G0} = -2.5$ V. (b) T2, $V_{G0} = -2.8$ V.

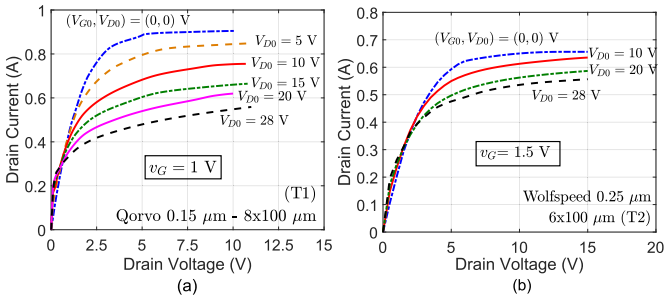

Fig. 4. Pulsed IVs (i_D vs. v_D) at maximum v_G from different V_{D0} and with $(V_{G,\mathrm{PP}}, V_{D,\mathrm{PP}}) = (-3.5, 2\ V_{D0})$ V (see Fig. 5). (a) T1, $V_{G0} = -2.5$ V. (b) T2, $V_{G0} = -2.8$ V.

to 120 MHz bandwidth in a 50-Ω environment [2], while the lower frequency of the ac path of the bias tees is 100 kHz. A benchtop driver amplifier allows to generate pulses with peak-to-peak amplitude up to ≈70 V. In this letter, the prepulse and the measurement pulse widths are ≈100 ns (10 ns rise/fall times), whereas the period is 10 μs (duty cycle ≈2%), ensuring isothermal operation at the base plate temperature at 30°C. Therefore, any measured IV degradation can only be due to charge trapping. The incident ($a_{1,2}$) and reflected ($b_{1,2}$) waves are sensed by the couplers and sampled with a scope, and then converted to IV curves. For device measurements, the bias current densities suggested by the foundries are 40 (T1) and 60 mA/mm (T2). The bias gate voltages V_{G0} are slightly adjusted to maintain 36 and 32 mA for T1 and T2, respectively, at all different V_{D0} values. The maximum drain bias voltage for both T1 and T2 is 28 V. In class-AB PAs, the maximum output power dynamic load line reaches the maximum current $i_D = I_{\max}$ at $v_D \approx V_k$ (knee voltage) and zero current at $v_D = V_{D,\max} = 2V_{D0}$, where $v_G = V_{G,\min}$. With these extremes in mind, Fig. 3 shows device performance for the following cases.

1) Benchmark reference single-pulse (SP) measurements with gate and drain biases set to 0 V. This minimizes the trap-induced degradation and enables the acquisition of the maximum current $\hat{I}_{\max} = 860$ mA for T1 and 617 mA for T2 (measured at $v_D = 10$ V) and the associated $\hat{V}_k$ (defined at 95% of $\hat{I}_{\max}$).
2) SP conventional measurements at the nominal bias point (−2.5, 28) V.
3) DP measurements at the nominal bias point prepulsed with $(V_{G,\mathrm{PP}}, V_{D,\mathrm{PP}}) = (V_{G,\min}, V_{D,\max}) = (-3.5, 56)$ V as indicated in Fig. 2(b) and (c). This DP measurement first prepares the device trap states allowing for a second-pulse measurement corresponding to the maximum load line extension in class-AB.

The data in Fig. 3 shows a considerable difference for the three cases. Despite showing an $I_{\max}$ reduction of 35% (T1) and 13% (T2), and an associated knee voltage V_k increase in ∼ 3.8 V (T1) and ∼ 1.3 V with respect to the reference benchmark, the SP IV characteristic from the nominal bias still underestimates the effects of traps activated in realistic load line conditions for class-AB. In fact, $I_{\max}$ obtained with the DP technique reveals a realistic current collapse of 39% (T1) and 18% (T2), with a slightly higher increase in V_k. These trap-induced effects result in a substantial output power reduction for both the technologies, where the more limited degradation of the 0.25 μm can be attributed to the higher drain voltage breakdown (120 vs. 60 V).

III. Characterization Oriented Toward PA Design

A. Class-AB PA Operation at Increasing Supply Voltage

The greater impact of traps for increasing bias voltage operation has been investigated, and the device output power P obtainable with a class-AB design was compared with respect to the output power $\hat{P}$ that would be extracted from the benchmark (SP) IV. The characteristics shown in Fig. 4 correspond to different V_{D0}, while v_G is kept at the maximum measured value of 1 and 1.5 V for T1 and T2, respectively. Each curve is obtained by setting the trap state to the typical peak voltage $v_D = V_{D,\max} = 2\ V_{D0}$ of class-AB designs. The increasing current collapse and walkout of the knee at increasing operating voltages has the same trend for both the technologies, as reported in Fig. 5. For the calculation of the output power degradation ($P/\hat{P}$), it is assumed that $P \propto I_{\max} V_{sw}$, being $V_{sw} = V_{D,\max} - V_k$, where the proportionality actually holds for every class derived from class-AB, for class-E, and for supply modulated PAs.

B. Class-E Versus Class-AB PA Operation

For a class-E PA delivering about the same power of a class-AB (power utilization factor = 1), the load line theoretically reaches a peak drain voltage $v_D = 3.56\ V_{D0}$. The IV curves pulsed from the same V_{D0} (15 V for T1 and 20 V for T2), but with different prepulse voltages corresponding to class-AB: $V_{D,\mathrm{PP}} = 2\ V_{D0}$ and class-E: $V_{D,\mathrm{PP}} = V_{D,\max} = 3.56\ V_{D0}$ are plotted in Fig. 6 and compared with the benchmark in Fig. 7, clearly showing that the higher peaking of v_D in class-E triggers increased charge trapping, causing a substantial performance reduction.

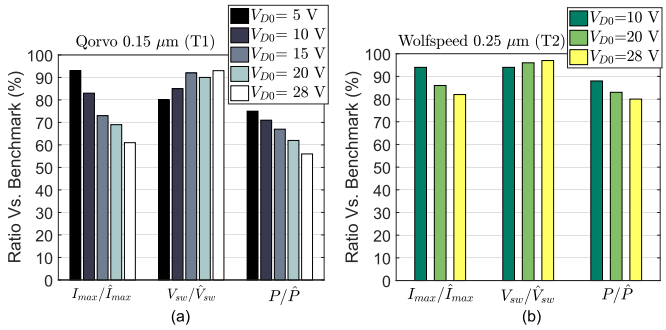

Fig. 5. Class-AB performance versus benchmark IV (indicated with $\wedge$), obtained prepulsing with $(V_{G,\mathrm{PP}}, V_{D,\mathrm{PP}}) = (-3.5, 2V_{D0})$ V. (a) T1. (b) T2.

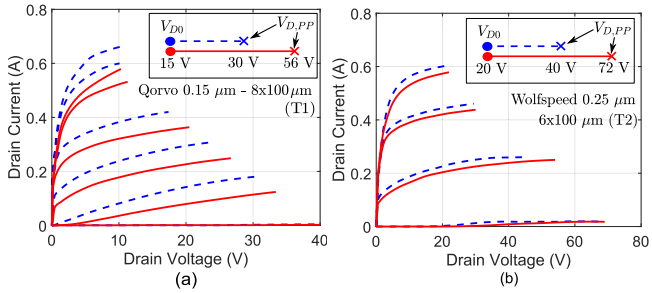

Fig. 6. Comparison of pulsed IVs (i_D vs. v_D) corresponding to class-AB (dashed blue) and class-E (red continuous) load lines. $V_{G,\mathrm{PP}} = -3.5$ V for T1 and T2. (a) T1, $(V_{G0}, V_{D0}) = (-2.5, 15)$ V. (b) T2, $(V_{G0}, V_{D0}) = (-2.8, 20)$ V.

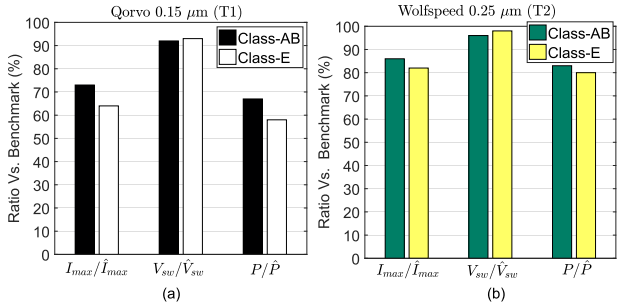

Fig. 7. Comparison between Class-AB and Class-E performance reduction versus benchmark IV (indicated with $\wedge$). (a) T1 with $(V_{G0}, V_{D0}) = (-2.5, 15)$ V. (b) T2 with $(V_{G0}, V_{D0}) = (-2.8, 15)$ V.

C. Supply Modulated PA Operation

The last comparison is devoted to the behavior under supply modulation (SM), used to enhance PA efficiency in the presence of high peak-to-average-power ratio signals. It has been observed [3] that the performance of GaN devices at low supply voltages is strongly deteriorated by the high amount of traps dynamically set when the PA operates at the highest supply level. In fact, since the trap state is set by the peak voltages, and the release of the trapped charge is very slow (up to seconds), all the supply levels are affected by the trap state imposed by the operating regime at the highest supply. In Fig. 8, the IV curves at the highest and lowest measured supply levels quantify the large degradation occurring when the supply level, pushed toward the maximum, triggers the maximum charge trapping. In addition, Fig. 9 reports the relative performance degradation at low supply levels due to the presence of SM ($V_{D,\max} = V_{D,\mathrm{PP}} = 56$ V) compared to the case without SM ($V_{D,\max} = V_{D,\mathrm{PP}} = 2V_{D0}$, indicated with $\sim$).

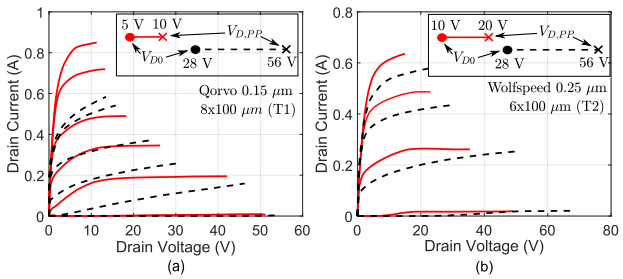

Fig. 8. Pulsed IVs (i_D vs. v_D) for the highest and lowest measured supply. $(V_{G,\mathrm{PP}}, V_{D,\mathrm{PP}}) = (-3.5, 2V_{D0})$ V for T1 and T2. (a) T1, $V_{G0} = -2.5$ V, $V_{D0} = 5$ and 28 V. (b) T2, $V_{G0} = -2.8$ V, $V_{D0} = 10$ and 28 V.

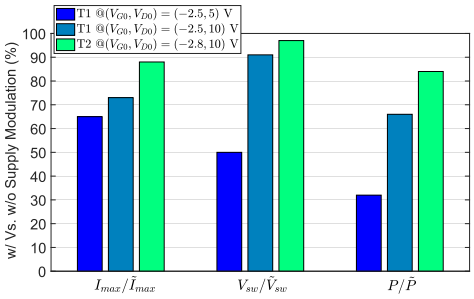

Fig. 9. Performance degradation at $V_{D0} = 5$ V and 10 V in the presence of SM ($V_{D,\max} = V_{D,\mathrm{PP}} = 56$ V) compared to the case without SM ($V_{D,\max} = V_{D,\mathrm{PP}} = 2V_{D0}$, indicated with $\sim$).

As can be seen, trap-related performance degradation results in a much lower output power. Therefore, a compromise between the maximum supply and the decreased output power at lower supply levels should be considered in the design stage.

IV. Conclusion

When the PA operating conditions exploit large drain voltage swings, as it especially happens in class-E and SM, GaN HEMT performance is drastically reduced by charge trapping. Particularly in these cases, the predictions of the achievable PA performance cannot be based on the nominal process parameters, but on custom double-pulsed IVs preconditioned to the trap state enforced by the targeted loadline.

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