

Load Modulation Measurements of X-Band Outphasing Power Amplifiers

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Abstract—This paper presents an in-depth investigation of both isolated and non-isolated outphasing power amplifiers, with and without supply modulation. X-band GaN MMIC power amplifiers with 70% power-added efficiency and 2.7 W output power at 10.1 GHz are configured in hybrid outphasing circuits with several combiners that include bi-directional couplers, enabling calibrated measurements of internal load modulation. It is experimentally demonstrated that the load modulation critically depends on the power balance of the two internal MMIC PAs. Despite the additional loss in the combiner, peak total efficiencies greater than 47% are achieved by full outphasing PAs with more than 3.7 W of output power. A comparison between several outphasing configurations quantifies the improvement in efficiency for both isolated and non-isolated outphasing PAs with supply modulation.

Index Terms—GaN, load modulation, LSNA, outphasing, power amplifiers.

I. INTRODUCTION

INCREASINGLY complex modulation schemes and broader bandwidths used in wireless communications put high demands on the front end transmitter power amplifier (PA), which is required to maintain linearity and efficiency at high powers and over peak-to-average power ratios (PAPR) exceeding 10 dB. Several PA architectures attempt to increase efficiency at power back-off. The Doherty PA [1], now common in cell-phone base stations [2], and the Chireix outphasing PA [3] use at least two PAs combined through a network that provides load modulation. Closely related to the outphasing PA, the LINC PA [4] (Linear amplification with Nonlinear Components) is concerned with linearity and does not operate with load modulation as it utilizes an isolated combiner. Another approach to maintaining efficiency at backed-off power without load modulation is dynamic variation of the DC supply, often referred to as supply modulation or envelope tracking [5], [6]. In this paper, we present several quasi-MMIC, 10.1 GHz outphasing PAs with the goal of investigating internal PA performance and load modulation at internal nodes during outphasing operation, with and without supply modulation. Most reported Outphasing PAs are at frequencies below 5 GHz, with

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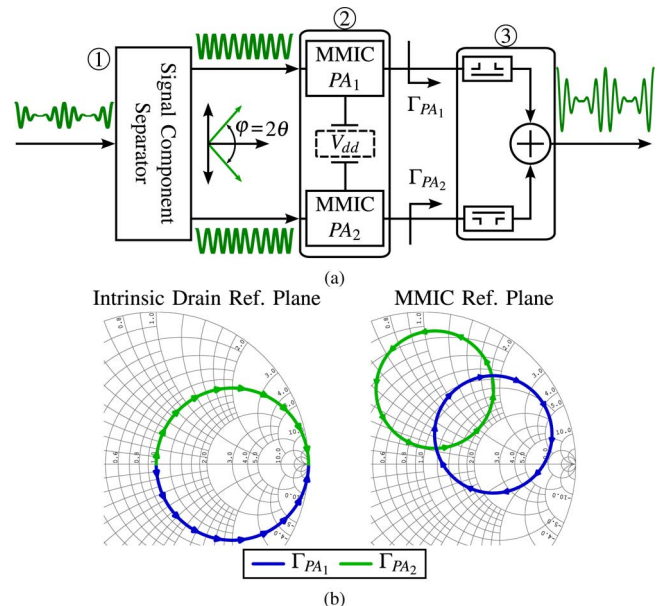


Fig. 1. (a) Flexible, MMIC based outphasing block diagram. Input signal amplitude modulation is converted into additional phase modulation by the signal component separator (SCS). Constant envelope signals drive the internal PAs at maximum efficiency. The combiner reconstructs the amplitude modulation through vector addition. (b) Load modulation at intrinsic drain and MMIC bondwire reference planes, describing the variation in Γ_{PA} with differential phase, φ . All Smith Charts in this paper are normalized to 50 Ω .

the exception of a recently reported fully integrated X-band MMIC PA [7], which does not include internal measurement nodes.

Fig. 1(a) shows our flexible, MMIC based outphasing circuit. The two MMIC PAs (2) are driven by constant amplitude CW signals with varying total differential phase, φ (twice the outphasing angle, θ). Both isolated and non-isolated off-chip combiners (3) include low-loss bi-directional couplers, enabling the measurement of waves at the output of the internal PAs, while constructing the envelope of the signal through vector addition of the differentially phase-modulated signals. Our measurement setup acquires absolute waves (magnitude and phase) at the input to control differential phase, as in [8], but also at the output of the internal PAs in order to investigate their performance and load modulation.

Understanding the interaction between the internal PAs and combiner during outphasing operation is critical, since it determines performance. The choice between isolated (LINC) and non-isolated (Chireix Outphasing) combining is a trade off between linearity and efficiency, respectively [9]. Chireix's approach using a lossless, three-port, non-isolated combiner with

reactive compensation remains prominent [10]–[15]. In this case, each PA is presented with an active, signal dependent load, referred to as load modulation and represented by reflection coefficients Γ_{PA1} , Γ_{PA2} in Fig. 1(a). Load modulation of the internal PAs dictates the system performance. Unfortunately, the analyses describing these dynamics are very idealized. Fig. 1(b) shows the load modulation given by equations in an idealized analysis, such as [16], [17], referenced to the intrinsic drain, which is often not accessible in simulation or measurement. The measured load modulation for a combiner designed to operate with a given, practical PA is quite different. Furthermore, the internal PAs are often assumed to behave as ideal voltage sources as in [18], but this assumption is not realistic as demonstrated in [19]. Our goal is to expand upon theoretical understanding to include practical, non-ideal PAs.

Isolated combiners are employed to simplify and stabilize outphasing operation by eliminating load modulation in LINC PAs. However, efficiency decays rapidly with signal crest factor due to power dissipated in the isolated combiner. To improve high-efficiency output power range, supply modulation can be added. In Multi-Level LINC (ML-LINC), discrete supply levels are varied symmetrically to provide coarse amplitude modulation, reducing power wasted in the isolated combiner by reducing the required differential phase [20]. Supply levels are optimized for the input signal [21], [22]. In Asymmetric Multi-Level Outphasing (AMO), independent variation of discrete supply levels provides increased efficiency through further reduction of required differential phase and power wasted in the isolated combiner [22], [23]. AMO has been validated in [24] and [25].

Our flexible outphasing circuit is extended to include the ML-LINC and AMO architectures. Furthermore, Multi-Level Chireix Outphasing (ML-CO) is presented here for the first time in literature to the best of the authors' knowledge. In Section II the design of the internal PAs and combiners are described. Section III details the specialized outphasing measurement setup introduced in [26], which enables deeper investigation of LINC PAs in this work. Sections IV and V take an investigative look at measurement results of both constant bias and supply modulated outphasing PAs respectively. Section VI considers the practical issues of linearity and prediction of load modulation considering power imbalance.

II. RF COMPONENT IMPLEMENTATION

This section outlines the design of the system's RF components, designated as ② and ③ in Fig. 1. The signal component separator (①) is typically implemented digitally as in [27]. Our analog implementation will be discussed with the measurement setup in Section III.

A. Power Amplifier Implementation

Two high-efficiency, 10.1 GHz, MMIC PAs [28] are used as components of the outphasing PAs. The single-stage design ($10 \times 100 \mu\text{m}$ pHEMT) is biased near pinch-off (5 mA) and optimized for efficiency without intentional harmonic terminations. The MMIC is fabricated in Qorvo's (TriQuint) 0.15 μm GaN

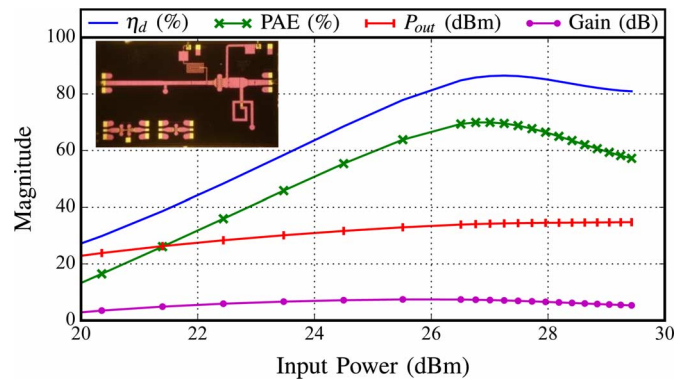


Fig. 2. Performance of the mounted MMIC PA, showing a peak PAE of 70% at 2.7 W of output power. (inset) Photo of the internal MMIC PA (3.8 mm \times 2.3 mm), which is a single-stage design using a $10 \times 100 \mu\text{m}$ pHEMT in Qorvo's (TriQuint) 0.15 μm GaN process.

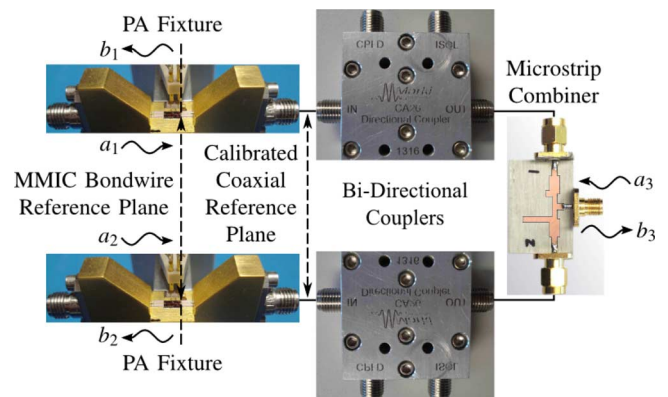


Fig. 3. Detail of PA-combiner assembly. All internal measurements (load modulation and internal PA performance) are de-embedded to the MMIC bondwire reference plane. Microstrip combiner is designed to provide desired load modulation.

process and shown in Fig. 2. The output matching network terminates the harmonics in short circuits, while optimizing the fundamental impedance for efficiency. On the PA fixture, each die is mounted on CuMo carriers and wire-bonded to alumina de-embedding lines with connectorized launchers, as well as DC bias capacitors. PA characterization and internal PA measurements in subsequent sections will be referenced to the MMIC bondwire plane. In Fig. 2 a peak power-added efficiency (PAE) of 70% with 2.7 W of output power and 7.2 dB of gain is measured at 10.1 GHz.

In a practical system, the internal PAs are often designed separately from the combiner [15] and the choice of PA class alters performance [19] and even optimal combiner topology [29]. Furthermore, the realized internal PAs do not behave as ideal voltage sources and class of operation may be unknown, especially at high frequencies. Therefore, the internal PAs are characterized by load-pull measurements at several drain voltages to inform the design of the combiner. PAE and P_{out} contours can be seen in Figs. 4(b) and 5(b).

B. Combiner Design

The combiner (③) in Fig. 1) provides the vital interaction between the internal PAs for outphasing operation. In order to

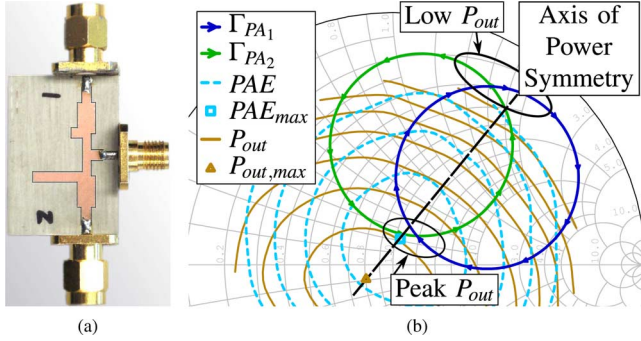


Fig. 4. (a) Non-isolated combiner designed for constant bias outphasing measurements at 10.1 GHz and fabricated on 30 mil Ro4350B substrate. (b) P_{out} and PAE load-pull contours measured at a P_{av} of 26 dBm, with the axis of power symmetry shown for design, and load modulation predicted by (6), (7). CW load-pull measurements have been performed with a LSNA (VTD-SWAP) and a passive tuner at 10.1 GHz. PAE contours are shown from 30% to 60% (with a 10% step) and P_{out} contours are traced from 28 to 35 dBm (with 1 dB step).

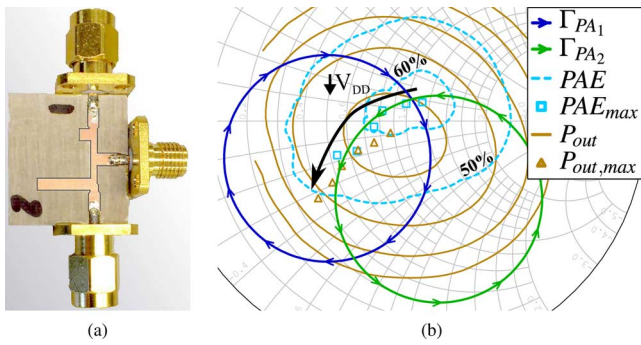


Fig. 5. (a) Non-isolated combiner designed for ML-LINC measurements at 10.1 GHz and fabricated on 30 mil Ro4350B substrate. (b) Measured load-pull data at a P_{av} of 26 dBm and drain voltages of 10, 12, 14, 16, 18, and 20 V. P_{out} contours are traced from 29 to 34 dBm (with 1 dB step) at 20 V supply to aid output power balancing. PAE contours for all voltages are combined into regions designating PAE > 50% and 60%, showing expansion of high efficiency impedances. Load modulation predicted by (6), (7) follow the movement of the PAE and P_{out} maxima with drain voltage.

measure the performance of the internal PAs and the load modulation, it is necessary to include low-loss (≈ 0.2 dB) bi-directional couplers [30] in the combiner topology. Since the load-pull characterization is performed at the MMIC bondwire reference plane, the design of the combiner and its load modulation should occur at this plane as well. As such, all transitions (including the PA fixture) and couplers on the output of the MMIC are measured and included in the combiner design, as detailed in Fig. 3. Off-chip combining adds significant loss (≈ 1 dB), but enables valuable comparison of several outphasing architectures are made. Next, details of three microstrip combiners used in this work are presented.

1) *Isolated Combiner*: The isolated combiner is a standard 180° rat-race circuit, providing both the sum and difference of the internal PAs. The return loss at each input is better than 19.5 dB, with an isolation between driven inputs of 22.5 dB, and through losses between 1.0 and 1.4 dB. The phase balance to the summing output is 4.5° , while the phase balance to the difference output is 173° .

2) *Non-Isolated Combiner*: Small-signal analysis predicts the load modulation of a lossless, 3-port combiner at the funda-

mental frequency, and yields equations useful for designing the load modulation contours. The reflected waves at the PA ports (1 and 2) are defined at the combiner reference planes in Fig. 3 as

$$b_1 = S_{11} a_1 + S_{12} a_2 + S_{13} a_3 \quad (1)$$

$$b_2 = S_{21} a_1 + S_{22} a_2 + S_{23} a_3. \quad (2)$$

In outphasing, the input power waves at the PA ports are phase shifted (θ) and possibly scaled (x) versions of each other

$$a_1 = x a_2 e^{j2\theta}, \quad a_2 = \frac{1}{x} a_1 e^{-j2\theta}, \quad a_3 = 0 \quad (3)$$

where port 3 is assumed to be matched, x predicts the effect of PA output power imbalance, and θ is the outphasing angle. Substituting these excitations into (1) and (2), the reflected waves become

$$b_1 = S_{11} a_1 + S_{12} \frac{1}{x} a_1 e^{-j2\theta} \quad (4)$$

$$b_2 = S_{21} x a_2 e^{j2\theta} + S_{22} a_2. \quad (5)$$

The reflection coefficients at each input port of the combiner, corresponding to the load modulation at the output of each internal PA, are solved as

$$\Gamma_{PA1} = \frac{b_1}{a_1} = S_{11} + \frac{1}{x} S_{12} e^{-j2\theta} \quad (6)$$

$$\Gamma_{PA2} = \frac{b_2}{a_2} = S_{22} + x S_{21} e^{j2\theta}. \quad (7)$$

The microstrip combiner shown in Fig. 4(a) is based on a tee-junction topology and optimized with conjugate susceptances [3]. The goal of the design is to intersect the load modulation contours, Γ_{PA1} and Γ_{PA2} , at the measured peak efficiency at the same outphasing angle (θ) and remain in the highest efficiency impedance region possible, while balancing over the axis of power symmetry, which is obtained from load-pull measurements at 20 V. The predicted load modulation contours in Fig. 4(b) achieve the design goal.

3) *Non-Isolated Combiner for Supply Modulation*: Fig. 5(a) shows another non-isolated combiner which is designed to account for the movement of peak efficiency loads as the drain supply varies from 10 V to 20 V. The predicted load modulation is overlaid on the measured load-pull characterization in Fig. 5(b). The region of PAE > 50% is expanded through the use of multiple supply levels. The trajectory of this combiner is designed to intersect at an outphasing angle (θ) at the peak PAE load for 20 V drain supply, follow the movement of the peak PAE and P_{out} impedances and maintain output power balance over the various supply conditions. P_{out} contours are shown only for 20 V, but balancing the output power is difficult across various supply levels as the line of symmetry shifts.

III. INTERNAL MEASUREMENT SETUP

A dedicated outphasing measurement setup is established for both internal PA and system measurements of various outphasing PAs. The near-field method to measure internal interactions in a Doherty PA in [31] requires specialized equipment (field probe, 3-D positioner) and continuous numerical simulation (HFSS). In this work, the absolute RF voltage

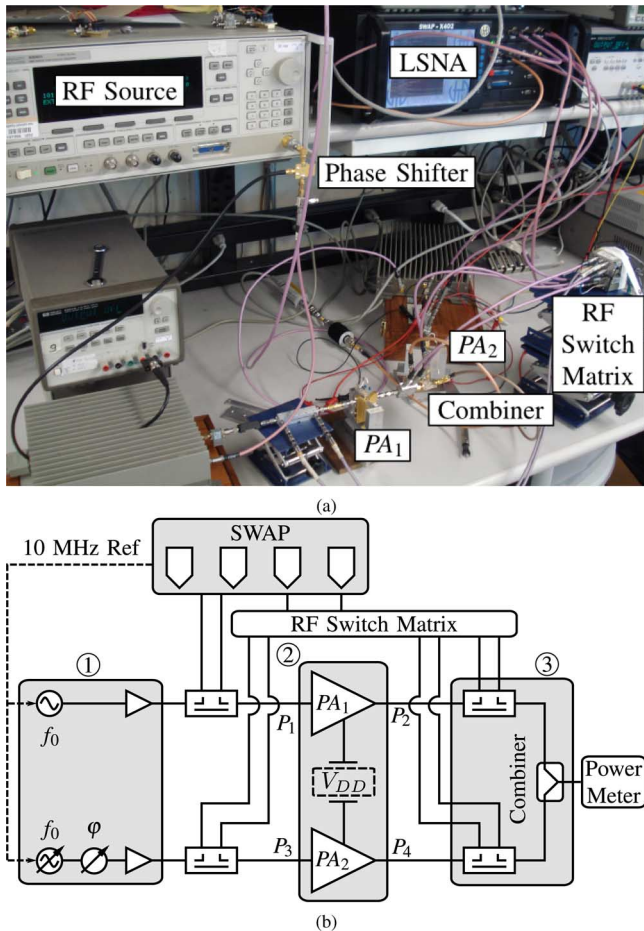


Fig. 6. (a) Photo of measurement setup. (b) The measurement setup is based on a 4-port LSNA. The two output couplers are included in the combiner, enabling measurement of internal load modulation and internal PA performance. A phase shifter (φ) sweeps the differential phase, while the source for that branch varies amplitude to maintain a balanced input power level which saturates both PAs.

and current waves of the internal PAs, within the outphasing system, are measured at both the input and the output through the inclusion of bi-directional couplers in the output combiner (as described in Section II.B).

The measurement setup in Fig. 6 is based on a four-port Large Signal Network Analyzer (LSNA), the VTD SWAP X-402 [32], but this work can be done with a VNA in receiver mode [33]. Typically, a four-channel, time-domain receiver is used for two-port DUT measurements, but here it is extended to measure two two-port DUTs (internal PAs) with the use of an RF switch matrix, which includes four RF SPDT switches. The calibrated coaxial reference planes are denoted P_1 , P_2 , P_3 , and P_4 , which are at the coaxial launchers of the MMIC fixture. In post-processing, the internal PA measurements are de-embedded further, to the MMIC bondwire. In this setup, port P_1 is measured continuously to provide a phase reference for the other three ports, which are measured sequentially using the RF switch matrix. Sequential measurements are aligned in the time-domain by adding a delay to force the phase of the fundamental voltage at port P_1 , $v_1(f_0)$, to 0° . Taking the input voltage as a phase reference is not an issue in an outphasing setup, because the input power level remains constant and large.

The calibration of this system consists of three sequential two-port calibrations (P_1 - P_2 , P_1 - P_3 , P_1 - P_4) corresponding to the three switch configurations. Each two-port calibration uses a VNA SOLT method along with an absolute power calibration on port P_1 in forward mode with a power meter, yielding an eight-term error matrix

$$\begin{pmatrix} v_1 \\ i_1 \\ v_2 \\ i_2 \end{pmatrix} = \begin{bmatrix} \alpha_1 & \beta_1 & 0 & 0 \\ \gamma_1 & \delta_1 & 0 & 0 \\ 0 & 0 & \alpha_2 & \beta_2 \\ 0 & 0 & \gamma_2 & \delta_2 \end{bmatrix} \cdot \begin{pmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{pmatrix} \quad (8)$$

where r_i is the raw-data acquired on the ADCs, and v_i and i_i are the RF voltages and currents respectively. During the outphasing measurements, the RF power applied to port P_1 , the input of PA_1 , is set for peak efficiency of the internal PA. A phase-shifter is placed after the second source and applied to port P_2 , the input of PA_2 , to sweep the differential phase $\varphi = \angle\{V_{in2}(f_0)/V_{in1}(f_0)\}$ between the internal PAs. The amplitude of the second source is adjusted for each phase to compensate for the variable losses in the phase-shifter, and maintain input amplitude balance. In addition to constant bias outphasing measurements, the drain supply of each internal PA, V_{DD1} and V_{DD2} , is varied during measurement both symmetrically (ML-LINC, ML-CO) and asymmetrically (AMO).

IV. CONSTANT SUPPLY OUTPHASING PAs

In addition to the qualitative insight into outphasing PAs this work provides, two parameters are defined to support quantitative comparison of prototypes within this paper: ΔP_{out} is the output power range where the total efficiency (η_{tot}) remains within 10 points of its peak value, and the dynamic P_{out} range is the difference between the maximum and minimum measured output powers. System performance is described by total efficiency because the input power should be considered and PAE unintuitively drops below zero when $P_{out} < P_{in}$

$$\eta_{tot} = \frac{P_{out}}{P_{dc} + P_{in}}. \quad (9)$$

A. LINC

The measured load modulation in Fig. 7(a) is small but nonzero. Due to the finite isolation, imperfectly matched ports, and any internal MMIC PA imbalance, one internal PA injects power into the other, leading to a measured output power imbalance between 0.5 dB and 1.6 dB. The internal PA load contours intersect at the peak PAE and P_{out} impedance.

Fig. 7(b) shows system and internal PA performances. The isolation is sufficient to maintain flat internal PA efficiencies throughout operation, but the power imbalance previously mentioned causes separation between them. Since the internal PAs are operating at nearly constant efficiency with differential phase, the system efficiency is most influenced by the output power characteristic, which rolls off sharply in outphasing as $\cos^2(\theta)$. Table I summarizes the system power and efficiency performance.

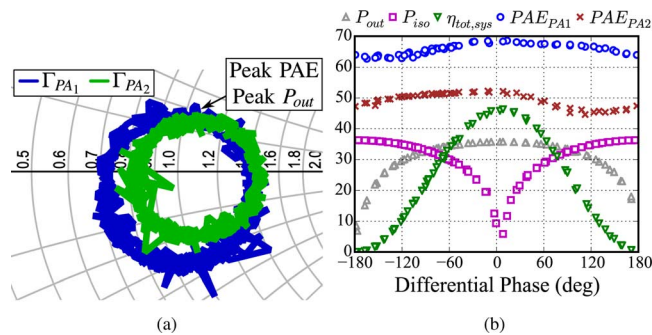


Fig. 7. (a) Measurement of load modulation presented to internal PAs (MMIC bondwire reference plane) when loaded with isolated rat-race combiner. (b) Measured LINC output power and efficiency, as well as internal PA efficiencies, at 20 V supply voltage. System achieves a peak η_{tot} of 47.6% at $\varphi = 8.2^\circ$ and a maximum P_{out} of 35.8 dBm at $\varphi = 3.7^\circ$, while internal PA efficiencies are flat signifying good isolation between PAs.

TABLE I
CONSTANT SUPPLY OUTPHASING PA PERFORMANCE

Architecture	Peak P_{out} (dBm)	Peak η_{tot} (%)	ΔP_{out} (dB)	Dynamic P_{out} Range (dB)
LINC	35.8	47.6	0.95	28.9
Chireix	35.7	47.0	1.9	32.1

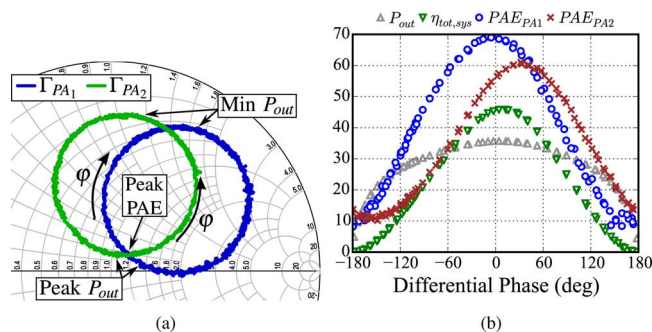


Fig. 8. (a) Measurement of load modulation presented to internal PAs (MMIC bondwire reference plane) when loaded with the non-isolated combiner from Fig. 4(a). (b) Measured Chireix outphasing output power and efficiency, as well as internal PA efficiencies, at 20 V supply voltage. System achieves a peak η_{tot} of 47.0% at $\varphi = 10.3^\circ$ and a maximum P_{out} of 35.7 dBm at $\varphi = 5.4^\circ$, while internal PA efficiencies vary drastically due to load modulation.

B. Chireix Outphasing

The measured load modulation for Chireix outphasing in Fig. 8(a) corresponds to a differential phase sweep from -180° to 180° . The peak PAE is obtained at the intersection of the two load contours, while the impedance for peak P_{out} is close, due to the proximity of the load contours to the peak power impedance. The minimum output power occurs at the edge of the Smith Chart.

Fig. 8(b) shows system and internal PA performances. The internal PA efficiencies, labeled as PAE_{PA1} and PAE_{PA2} , show significant variation due to the load modulation. Furthermore, the two are separated and do not peak at the same differential phase, due to the internal PA output power imbalance between ± 1.5 dB. Reference (6), (7) explain the effect of power imbalance on load modulation through the variable x . Although the load modulation appears balanced (equal radii), the power imbalance causes a subtle counter-clockwise (CCW) rotation as

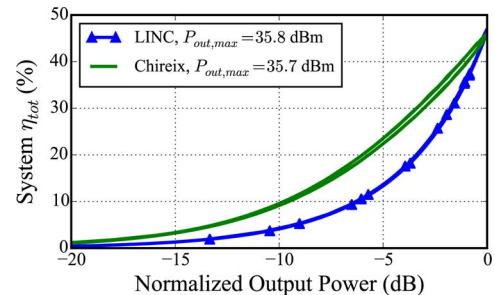


Fig. 9. Comparison of measured system η_{tot} for constant bias LINC and Chireix outphasing PAs. Chireix outphasing shows an improvement of 10 points at -5 dB $P_{out,n}$.

well as slight enlarging of the Γ_{PA2} contour. Table I summarizes the system performance, and shows improvement in both ΔP_{out} and dynamic P_{out} range by 0.95 dB and 3.2 dB, respectively, over the LINC PA.

In Fig. 9, the η_{tot} of both the LINC and Chireix outphasing PA is plotted against normalized output power ($P_{out,n}$). Chireix outphasing improves η_{tot} by up to 10 points at -5 dB $P_{out,n}$. One shortcoming of the constant supply outphasing PAs is the small output power range of high-efficiency amplification (ΔP_{out}). This can be improved with the addition of supply modulation, as is discussed in the next section.

V. SUPPLY-MODULATED LINC PAs

A. Multi-Level LINC

In the ML-LINC PA, the drain supply voltages are varied between n discrete levels symmetrically, reducing outphasing angle range and power dissipated in the isolated combiner. Our prototype ML-LINC PA is similar to that in [20], except a rat-race combiner is used rather than a Wilkinson.

Increased performance at lower output power is demonstrated in Fig. 10(a), where the efficiency is increased by 10–26 points compared to the 20 V case. The optimal operating points (solid blue) are chosen for peak η_{tot} , which aligns with the method in [20] of choosing the supply level to be as small as possible while reaching the desired P_{out} . Table II summarizes the performance showing a ΔP_{out} improvement of 1.2 dB over Chireix outphasing and 2.15 dB over LINC. In the following figures, the optimal operation (green circles) shows discontinuities corresponding to discrete supply steps. Fig. 10(b) exhibits the reduction in differential phase required, where the optimal operation only requires $-24^\circ < \varphi < 55^\circ$ above 28 dBm (8.5 dB below peak power), 60° less than for 20 V supply.

The reduced differential phase improves η_{tot} because less power is dissipated in the isolated combiner. In Fig. 11(a), the optimal operation dissipates less than 0.92 W of RF power in the combiner, and provides 3.28 W of improvement over 20 V operation 16.5 dB below peak power (20 dBm). Aside from this expected mechanism for efficiency improvement, Fig. 11(b) demonstrates a secondary effect. As in envelope tracking, the DC power consumed by the internal PA reduces with supply voltage. Below 29.6 dBm (7 dB below peak power), the DC power consumption is reduced by 6.6 W. Therefore, the

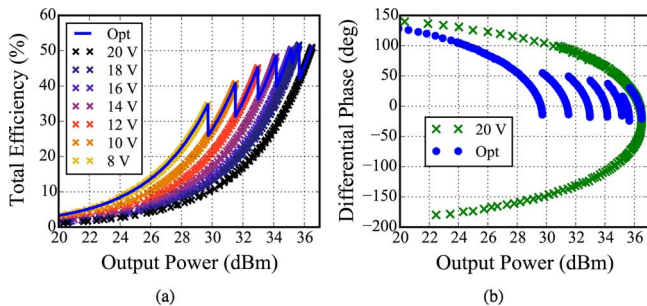


Fig. 10. (a) Measured system total efficiency of ML-LINC PA for swept differential phase at drain voltages of 10, 12, 14, 16, 18, and 20 V demonstrating advantageous new peaks. Optimal operation selected for peak η_{tot} at each output power. (b) Comparison of measured differential phase for 20 V showing a range of $-24^\circ < \varphi < 115^\circ$ and optimal operation showing a reduction to $-24^\circ < \varphi < 55^\circ$ above 28 dBm (8.5 dB below peak power).

TABLE II

MEASURED SYSTEM PERFORMANCE OF SUPPLY MODULATED LINC PAs

Architecture	Peak P_{out} (dBm)	Peak η_{tot} (%)	ΔP_{out} (dB)	Dynamic P_{out} Range (dB)
ML-LINC	36.5	51.7	3.1	39.5
AMO	36.5	52.5	4.9	41.1
ML-CO	36.8	51.3	5.25	10.5

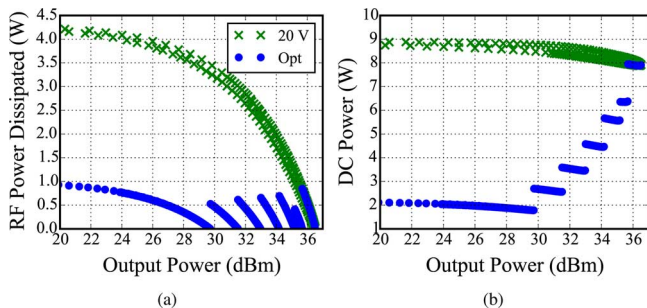


Fig. 11. (a) Measured RF power dissipated in the isolated combiner for 20 V and optimal operation of the ML-LINC PA. Dissipated power remains below 0.92 W in optimal operation down to 20 dBm (16.5 dB below peak power), where an improvement of 3.28 W is achieved. (b) Measured DC power consumption of internal PAs is seen to reduce by 6.6 W below 29.6 dBm (7 dB below peak power) for optimal operation.

benefits of both outphasing and supply modulation contribute to improve performance.

B. Asymmetric Multi-Level Outphasing

The AMO PA only differs from ML-LINC in that the supply levels are allowed to vary independently as in [22] and [23]. New combinations of supply levels give rise to more peaks in efficiency. In Fig. 12(a) supply levels from 10 V to 20 V in 2 V increments include combinations of adjacent levels. In doing so, n supply levels now yields $(2n - 1)$ efficiency peaks rather than n in ML-LINC. This improvement is more pronounced for fewer supply levels. Table II summarizes the performance showing a further ΔP_{out} improvement of 1.8 dB compared to ML-LINC.

As in ML-LINC, the differential phase range is reduced in Fig. 12(b) to $-75^\circ < \varphi < -5^\circ$ down to 32 dBm (4.5 dB below peak power), 55° of improvement over 20 V supply. The same two mechanisms are again reducing lost power.

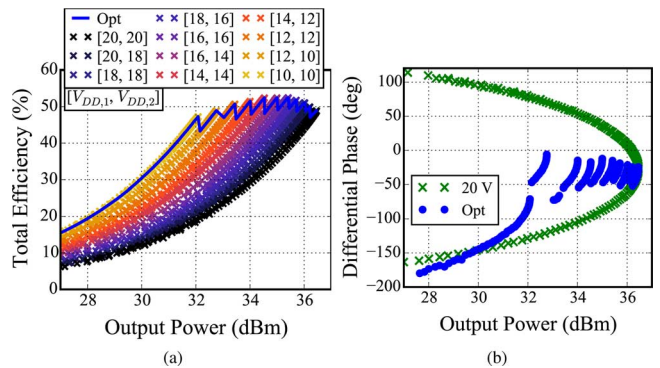


Fig. 12. (a) Measured system total efficiency of AMO PA for swept differential phase at drain voltages of 10, 12, 14, 16, 18, and 20 V and combinations of adjacent levels ($2n - 1$ total), demonstrating more peaks than ML-LINC. Optimal operation selected for peak η_{tot} at each output power. (b) Measured differential phase for 20 V and optimal operation of AMO PA, showing a reduction to $-75^\circ < \varphi < -5^\circ$ down to 32 dBm (4.5 dB below peak power).

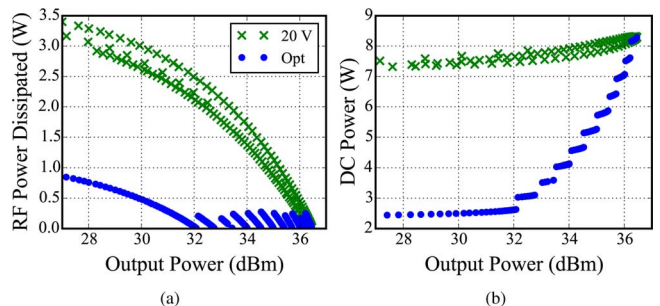


Fig. 13. (a) Measured RF power dissipated in the isolated combiner for 20 V and optimal operation of the AMO PA. Under optimal operation, dissipated power remains below 0.48 W down to 30 dBm (6.5 dB below peak power), where an improvement of 2.5 W is achieved. (b) Measured DC power consumption of internal PAs is seen to reduce by 4.9 W below 31.2 dBm (4.4 dB below peak power) for optimal operation.

Fig. 13(a) illustrates the reduced RF power wasted in the isolated combiner, remaining below 0.48 W down to 30 dBm (6.5 dB below peak power), where an improvement of 2.5 W is achieved. Fig. 13(b) validates the supply modulation effect through the decreased DC power consumption of the internal PA, which is improved by 4.9 W below 31.2 dBm (4.4 dB below peak power). As shown in the AMO η_{tot} , the increased number of supply level combinations provides a more continuous reduction in wasted RF and DC power.

Commonly, AMO systems utilize only discrete supply levels and combinations of adjacent levels. This restriction is placed because the combining efficiency of an isolated combiner decreases as the difference between supply levels increases, leading to a negligible improvement in efficiency [22]. An explanation for this can be seen in Fig. 14, which shows the load modulation, internal PA efficiency, and system efficiency for the following supply voltage combinations: $[V_{DD1}, V_{DD2}] = [10 \text{ V}, 20 \text{ V}], [15 \text{ V}, 20 \text{ V}], [20 \text{ V}, 20 \text{ V}], [10 \text{ V}, 10 \text{ V}], [20 \text{ V}, 15 \text{ V}],$ and $[20 \text{ V}, 10 \text{ V}]$. As the internal PA output powers become imbalanced (by asymmetric supply levels), the isolation in the combiner is insufficient to prevent substantial load modulation (Fig. 14(a)). Fig. 14(b) shows that this amount of load modulation is enough to decrease the efficiency of one internal PA as well as the system. Compared to the efficiency

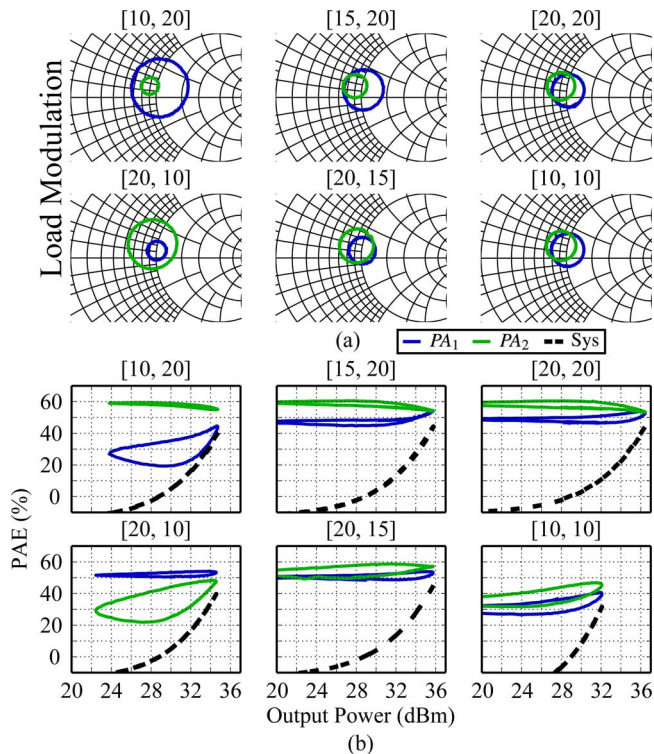


Fig. 14. Measured (a) load modulation, and (b) internal PA and system PAE for the AMO PA with supply levels demonstrating large and small differences: $[V_{DD1}, V_{DD2}] = [10 \text{ V}, 20 \text{ V}], [15 \text{ V}, 20 \text{ V}], [20 \text{ V}, 20 \text{ V}], [10 \text{ V}, 10 \text{ V}], [20 \text{ V}, 15 \text{ V}],$ and $[20 \text{ V}, 10 \text{ V}]$. Significant load modulation occurs for large supply differences, leading to the decrease in internal PA and system efficiency.

for combinations of adjacent levels in Fig. 12(a), the system efficiency for large supply imbalances is greatly decreased.

Further confirmation for the restriction to adjacent supply levels is established in Fig. 15, which exhibits operating points, chosen for peak efficiency, for all combinations of the drain voltages from 10 V to 20 V in 1 V steps. For each output power contour (solid black lines), the optimal η_d and η_{tot} in (a) and (b), respectively, lies on the trajectory of symmetric supply levels (dashed black line). While the optimal continuous trajectory maintains balanced supply levels, AMO offers efficiency improvement over ML-LINC when implementing discrete supply levels through additional adjacent asymmetric level combinations.

C. Multi-Level Chireix Outphasing

To the best of the authors' knowledge, the supply modulated outphasing PA with a non-isolated combiner, called Multi-Level Chireix Outphasing (ML-CO), is presented for the first time in literature. As described in Section II.B, the non-isolated combiner used here provides load modulation in the opposite direction as that used for constant bias Chireix outphasing. Since ML-CO maintains balanced supply levels, (6) and (7) are valid.

Fig. 16(a) shows the system η_{tot} , which exhibits hysteresis caused by the difference in efficiency between load modulation paths from peak to minimum power in non-isolated combiners. The hysteresis widens at lower drain supply levels, which improves performance and reduces the number of discrete levels required to maintain high efficiency. Fig. 16(b) compares the

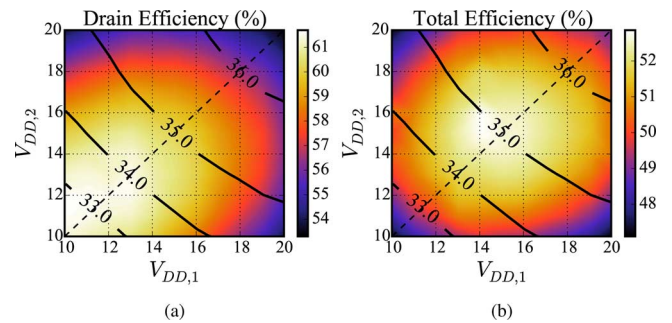


Fig. 15. 2-Dimensional visualization of AMO measurements for all combinations of drain voltages from 10 V to 20 V in 1 V steps, showing (a) drain efficiency (η_d) and (b) total efficiency (η_{tot}), with solid black lines designating P_{out} and the dashed black line designating supply level symmetry. For each output power, the most efficient choice of supply levels is symmetric.

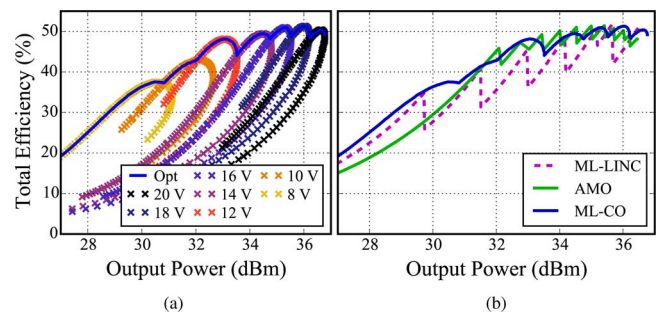


Fig. 16. (a) Measured system total efficiency of ML-CO PA for swept differential phase at drain voltages of 10, 12, 14, 16, 18, and 20 V. Optimal operation, selected for peak η_{tot} at each output power, takes advantage of load modulation hysteresis to maintain high η_{tot} . (b) Comparison of system η_{tot} between all supply modulated LINC PAs, demonstrating the prospect of ML-CO.

optimal η_{tot} trajectories for the three supply modulated outphasing PAs, where the ML-CO PA performs similarly to the others at peak power and surpasses them below 31.5 dBm (5 dB below peak power). Table II summarizes the system performance, showing a further increase in ΔP_{out} of 0.35 dB beyond the AMO PA and a 30 dB decrease in dynamic P_{out} range. The reduction results from the sweeps not completing the full load modulation contours near the edge of the Smith Chart, which only affects very low power operation. However, simulation confirms comparable range under full load modulation sweeps.

Unlike the LINC PAs, the ML-CO PA is 'lossless' in the sense that no power is wasted in the combiner to provide isolation. Therefore, the only mechanism improving performance is the reduction of DC power consumption with the supply level. In Fig. 17(a), the DC power consumption of optimal operation is consistent with that of the AMO PA, and shows a reduction of 8 W compared to 20 V operation at 30 dBm (6.8 dB below peak power). In Fig. 17(b) the required differential phase is decreased for optimal ML-CO operation to $-80^\circ < \varphi < -3^\circ$ down to 29 dBm (7.8 dB below peak power), a 75° improvement over 20 V operation.

The measured load modulation in Fig. 18 explains the advantageous widening hysteresis in the efficiency. The optimal phase trajectory starts at the peak P_{out} load and moves toward the peak PAE load. At high supply voltages, both peak loads occur near the center of the Smith Chart, and the optimal trajectory moves toward the edge. At 12 V drain voltage, however, the

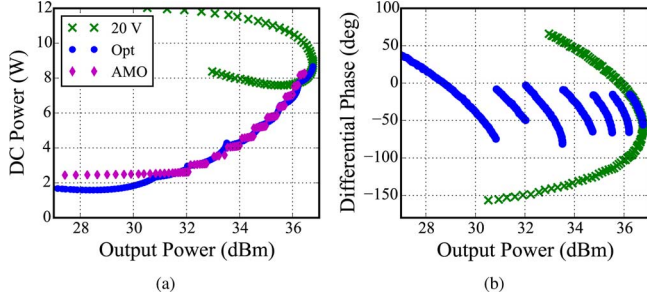


Fig. 17. (a) Comparison of measured internal PA DC power consumption between 20 V, optimal ML-CO operation, and AMO. ML-CO reduces consumption by 8 W over the 20 V supply, and exhibits the same smooth decay as the AMO PA. (b) Measured differential phase for 20 V and optimal operation of ML-CO PA, showing a reduction to $-80^\circ < \varphi < -3^\circ$.

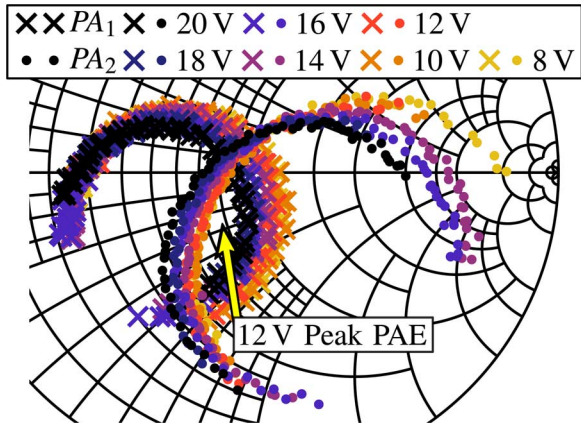


Fig. 18. Measured internal load modulation in the ML-CO PA. Imbalance in impedance loci radii exposes the difficulty in maintaining internal PA P_{out} balance, but is mitigated through reduced differential phase requirements and balanced supply levels.

peak P_{out} is between the load modulation intersections, while the peak PAE stays near the upper one. Now the upward phase trajectory remains in the high PAE region for a larger range of P_{out} . The separation of peak PAE and P_{out} loads at lower supply levels leads to wider hysteresis.

The load modulation also demonstrates the difficulty in maintaining internal PA output power balance over several supply levels through the imbalanced radii of the impedance loci. This issue may lead to instability, but the ML-CO PA mitigates the risk by reducing the required differential phase as well as symmetrically adjusting the supplies. Risk could be further reduced by integrating the design in a single MMIC, since the internal PAs would be more balanced. Simulation shows that no new peaks in PAE are introduced by asymmetrically varying the supplies with a non-isolated combiner, and doing so creates more load modulation imbalance.

VI. DISCUSSION

A. System Nonlinearity

Although specific linearity measurements (two-tone test, ACLR, EVM) are not performed, linearity indicators can be ascertained from CW characterization. Gain and phase imbalances between the branches are key contributors to nonlinearity

TABLE III
MEASURED GAIN AND PHASE IMBALANCE IN LINC PAS

Architecture	Max Gain Imbalance (dB)	Max Phase Imbalance ($^\circ$)	Max Encoding Distortion ($^\circ$)
LINC	1.26	20.67	3.74
Chireix	2.01	25.01	5.39
ML-LINC	1.21	17.75	-24.25
AMO	1.48	16.31	-26.4
ML-CO	2.79	52.52	-103.2

in all outphasing PAs [34], and are caused by imbalances in the internal PAs and/or the combiner [35], [36]. Branch imbalances restrict the cancellation of the wide bandwidth quadrature signal component, leading to residue in adjacent channels [37]. The maximum measured gain and phase imbalances are listed in Table III, which come from the optimal operating points for the supply modulated outphasing PAs. The isolated combiner achieves the lowest gain imbalance, but AMO degrades slightly due to imbalanced supply levels. In [38] phase imbalance is shown to be more dependent on the gain imbalance than branch electrical length imbalance, which explains the measured phase imbalances without significant branch length differences. As such, the large phase imbalance of ML-CO can be anticipated since it operates under both load and supply modulation, adjusting the loading and response of the internal PAs differently.

An additional source of nonlinearity in outphasing PAs is the nonlinear phase transformation [35], [39], which is found to be inherent in non-isolated combiners due to impedance mismatching [40]. However, this nonlinearity can be separated into encoding and clipping distortions [41]. The encoding distortion is listed in Table III, and is a phase offset that shifts the peak output power from $\theta = 0^\circ$, which is visible in Figs. 7(b), 8(b) as well as in the measured differential phases of the supply modulated outphasing PAs in Figs. 10(b), 12(b), 17(b). In the supply modulated cases, the encoding distortion changes with supply level, so the largest distortion is listed.

After subtracting this offset, the clipping distortion is examined using two representations from measurements. First, the theoretical and measured differential phases are compared. From the output power with respect to outphasing angle in [10], the theoretical differential phase can be deduced using the measured $P_{out,n}$

$$\varphi = 2 \arccos(10^{P_{out,n}/20}). \quad (10)$$

The difference between the theoretical and measured differential phases is plotted. Second, the measured differential phase and $P_{out,n}$ are plotted. In all cases, the solid blue trace shows the ideal (linear) characteristic.

Fig. 19 establishes the near linear response of the LINC PA, which only deviates by 8° from ideal in (a) and follows the ideal output power response closely in (b). The Chireix outphasing PA, deviates up to 25° in (a) and 2.7 dB in (b) from linear operation.

Variation of the supplies in ML-CO exacerbates the nonlinearity of Chireix outphasing. In Fig. 20, the ML-CO PA shows up to 50° in (a) and 7.5 dB in (b) of deviation from linear operation. On the other hand, the divergence of the ML-LINC PA

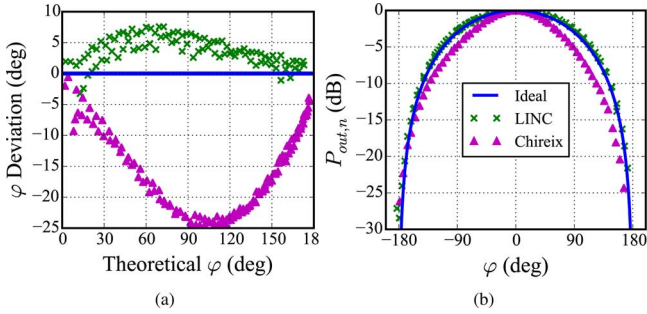


Fig. 19. (a) Measured differential phase deviation, and (b) Measured output power with respect to differential phase for both LINC and Chireix outphasing PAs. While the LINC PA follows closely the ideal relationships, the Chireix outphasing PA deviates up to 25° in (a) and 2.7 dB in (b).

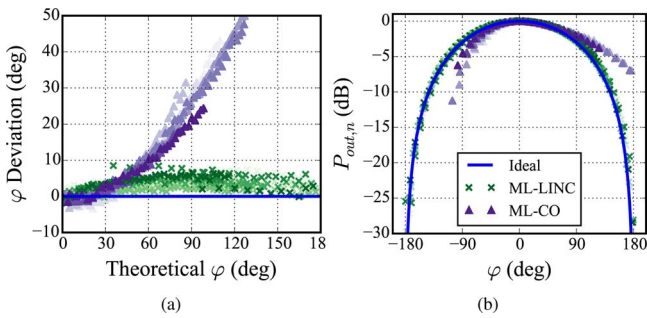


Fig. 20. (a) Measured differential phase deviation, and (b) Measured output power with respect to differential phase for both ML-LINC (green x) and ML-CO (purple triangles) PAs. The shading reveals the supply level from 10 V (lightest) to 20 V (darkest). While the ML-LINC PA follows closely the ideal relationships, the ML-CO PA deviates up to 50° in (a) and 7.5 dB in (b).

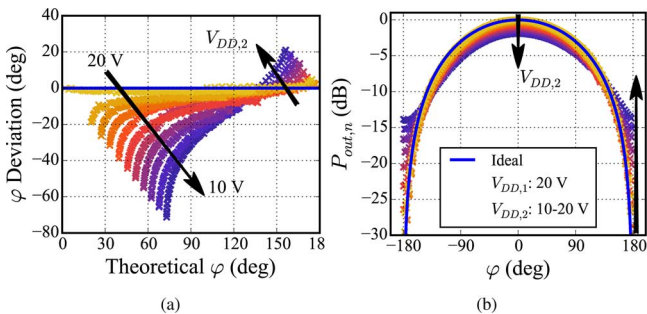


Fig. 21. (a) Measured differential phase deviation, and (b) Measured output power with respect to differential phase for the AMO PA. V_{DD1} is 20 V, and V_{DD2} is varied from 10 V to 20 V in 1 V steps. As the supply level difference increases, the nonlinear phase transformation becomes more pronounced.

from linear operation remains below 8° in (a) and is negligible in (b).

Interestingly, the AMO PA experiences increasingly nonlinear phase transformation as the difference in its supply levels increases. In Fig. 21, $V_{DD1} = 20$ V and V_{DD2} varied from 10 V to 20 V. As V_{DD2} decreases, the deviation from linear phase relationship increases to 75° in (a). In (b), not only does the peak power decrease, but the minimum power increases by upwards of 20 dB. These factors significantly degrade the linearizability of the system, which adds to the previously determined reasons to utilize only adjacent combinations of supply levels.

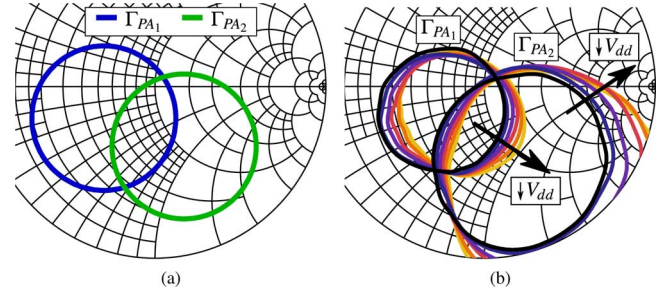


Fig. 22. (a) Simulation predicting the load modulation of a measured combiner based on (6) and (7) while internal PAs are biased at 20 V. (b) Simulated predicted load modulation using feedback to account for internal PA output power imbalance at supply levels between 10 V and 20 V in 2 V steps.

While these measurements show significant nonlinearity, especially in ML-CO, the authors are hopeful adequate linearization can be achieved as proven in [15], [25], [39]. Nevertheless, these measurements provide insight into the linearizability of each architecture.

B. Predicting Load Modulation With Power Imbalance

Though (6) and (7) include a variable, x , to account for power imbalances at the driven ports, entering a single value for x will not accurately predict load modulation. As illustrated in the measurements presented, the power imbalance induced by the loading is not constant with differential phase. Furthermore, in ML-CO the output power balance varies with supply voltage, seen in the varying deformations shown in Fig. 18. In order to aid in the combiner design for these cases, a measurement based simulation method is developed that uses feedback to accurately predict load modulation with power imbalance. Because each internal PA is characterized, this method will predict the imbalances caused by the differences in the two die.

The procedure is as follows.

- Characterize each internal PA with load-pull measurement at all desired supply levels.
- Interpolate load-pull measurements.
- Simulate or measure S-parameters of combiner at the same frequency and reference plane as internal PA characterizations.
- Calculate initial values of Γ_{PA1} and Γ_{PA2} from (6) and (7), as seen in Fig. 22(a).
- From load-pull interpolation, find P_{out} for each internal PA at initial values of Γ_{PA1} and Γ_{PA2} .
- Calculate power imbalance, the difference in P_{out} between the internal PAs.
- Re-calculate values of Γ_{PA1} and Γ_{PA2} from (6) and (7) inserting the calculated power imbalance as the variable x , as seen in Fig. 22(b).

The procedure is performed for the measured combiner used in ML-CO measurements. The predicted load modulation in Fig. 22(b) shows the same expansion of the Γ_{PA2} and shrinking of the Γ_{PA1} circles, and compares extremely well qualitatively to the measurement in Fig. 18. Note that the load-pull characterization had a limited range of $|\Gamma|$, so the load modulation at the

edge of the Smith Chart will not be accurate due to interpolation error.

VII. CONCLUSION

We have presented a method for measuring internal PA performance and load modulation in outphasing PAs with and without supply modulation, through the inclusion of bi-directional couplers in the combiner. Additionally, comparisons can be drawn between the five outphasing PAs in this work: LINC, Chireix, ML-LINC, AMO, and ML-CO. For the isolated combiner, AMO demonstrates the largest output power range with high-efficiency operation (ΔP_{out}), 1.8 dB more than ML-LINC, by utilizing nearly twice as many supply levels. Exploiting only adjacent combinations of supply levels not only maintains higher efficiency by reducing both the wasted RF power and the DC power consumption, but limits the amount of load modulation and corresponding internal PA performance reduction.

ML-CO has not been discussed in the literature, but is shown to provide a competitive alternative to AMO by achieving the highest ΔP_{out} among the supply modulated outphasing PAs. The shape of its hysteresis indicates fewer supply levels are required to maintain performance.

Finally, practical concerns of these PA architectures are discussed. Observable indications of linearity are found in the branch gain and phase imbalances, as well as the nonlinear phase transformation. A method for accurately predicting load modulation considering output power imbalance is developed to aid in combiner design, especially over varying supply levels.

REFERENCES

- [1] W. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. IRE*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.
- [2] J. Kim, J. Moon, D. Kang, S. Jee, Y. Y. Woo, and B. Kim, "Doherty power amplifier design employing direct input power dividing for base station applications," in *Proc. Eur. Microw. Conf.*, Sep. 2010, pp. 866–869.
- [3] H. Chireix, "High power outphasing modulation," *Proc. IRE*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.
- [4] D. Cox, "Linear amplification with nonlinear components," *IEEE Trans. Commun.*, vol. 22, no. 12, pp. 1942–1945, Dec. 1974.
- [5] C. Buoli, A. Abbiati, and D. Riccardi, "Microwave power amplifier with "envelope controlled" drain power supply," in *Proc. Eur. Microw. Conf.*, Sep. 1995, vol. 1, pp. 31–35.
- [6] G. Hanington, P.-F. Chen, P. Asbeck, and L. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.
- [7] C. Xie, D. Cripe, J. Keyland, D. Landt, and A. Walker, "Development of high-efficiency X-band outphasing transmitter," in *Proc. IEEE Compound Semiconduct. Integr. Circuit Symp.*, Oct. 2014, pp. 1–4.
- [8] C. Andersson, D. Gustafsson, J. C. Cahuana, R. Hellberg, and C. Fager, "A 1–3-GHz digitally controlled dual-RF input power-amplifier design based on a Doherty-outphasing continuum analysis," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 10, pp. 3743–3752, Oct. 2013.
- [9] A. Birafane, M. El-Asmar, A. Kouki, M. Helou, and F. Ghannouchi, "Analyzing LINC systems," *IEEE Microw. Mag.*, vol. 11, no. 5, pp. 59–71, Aug. 2010.
- [10] I. Hakala, D. Choi, L. Gharavi, N. Kajakine, J. Koskela, and R. Kautisto, "A 2.14-GHz chireix outphasing transmitter," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 6, pp. 2129–2138, Jun. 2005.
- [11] J. Grundlingh, K. Parker, and G. Rabjohn, "A high efficiency Chireix out-phasing power amplifier for 5 GHz WLAN applications," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2004, vol. 3, pp. 1535–1538.
- [12] W. Gerhard and R. Knoechel, "Differentially coupled outphasing WCDMA transmitter with inverse class F power amplifiers," in *Proc. IEEE Radio Wireless Symp.*, Jan. 2006, pp. 355–358.
- [13] J. Qureshi, M. Pelk, M. Marchetti, W. Neo, J. Gajadharsing, M. Van der Heijden, and L. C. N. De Vreede, "A 90-W peak power GaN outphasing amplifier with optimum input signal conditioning," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 8, pp. 1925–1935, Aug. 2009.
- [14] D. Perreault, "A new power combining and outphasing modulation system for high-efficiency power amplification," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1713–1726, Aug. 2011.
- [15] D. Calvillo-Cortes, M. van der Heijden, M. Acar, M. de Langen, R. Wesson, F. van Rijs, and L. de Vreede, "A package-integrated Chireix outphasing RF switch-mode high-power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 10, pp. 3721–3732, Oct. 2013.
- [16] B. Stengel and W. Eisenstadt, "LINC power amplifier combiner method efficiency optimization," *IEEE Trans. Veh. Technol.*, vol. 49, no. 1, pp. 229–234, Jan. 2000.
- [17] W. Gerhard and R. Knoechel, "Improved design of outphasing power amplifier combiners," in *Proc. German Microw. Conf.*, Mar. 2009, pp. 1–4.
- [18] F. Raab, "Efficiency of outphasing RF power-amplifier systems," *IEEE Trans. Commun.*, vol. 33, no. 10, pp. 1094–1099, Oct. 1985.
- [19] J. Yao and S. Long, "Power amplifier selection for LINC applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 8, pp. 763–767, Aug. 2006.
- [20] Y.-C. Chen, K.-Y. Jheng, A.-Y. Wu, H.-W. Tsao, and B. Tzeng, "Multi-level LINC system design for wireless transmitters," in *Proc. Int. Symp. VLSI Des. Automat. Test.*, Apr. 2007, pp. 1–4.
- [21] J. Guan, A. Aref, and R. Negra, "System-level performance study of a multistandard outphasing transmitter using optimised multilevels," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2011, pp. 1–4.
- [22] S. Chung, P. Godoy, T. Barton, E. Huang, D. Perreault, and J. Dawson, "Asymmetric multilevel outphasing architecture for multi-standard transmitters," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2009, pp. 237–240.
- [23] J. Hur, O. Lee, K. Kim, K. Lim, and J. Laskar, "Highly efficient uneven multi-level LINC transmitter," *Electron. Lett.*, vol. 45, no. 16, pp. 837–838, Jul. 2009.
- [24] P. Godoy, S. Chung, T. Barton, D. Perreault, and J. Dawson, "A highly efficient 1.95-GHz, 18-W asymmetric multilevel outphasing transmitter for wideband applications," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2011, pp. 1–4.
- [25] P. Godoy, S. Chung, T. Barton, D. Perreault, and J. Dawson, "A 2.4-GHz, 27-dBm asymmetric multilevel outphasing power amplifier in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2372–2384, Oct. 2012.
- [26] M. Litchfield, T. Reveyard, and Z. Popovic, "X-band outphasing power amplifier with internal load modulation measurements," in *Proc. Eur. Microw. Conf.*, Oct. 2014, pp. 1428–1431.
- [27] Y. Li, Z. Li, O. Uyar, Y. Avniel, A. Megretski, and V. Stojanovic, "High-throughput signal component separator for asymmetric multilevel outphasing power amplifiers," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 369–380, Feb. 2013.
- [28] S. Schafer, M. Litchfield, A. Zai, Z. Popovic, and C. Campbell, "X-band MMIC GaN power amplifiers designed for high-efficiency supply-modulated transmitters," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2013, pp. 1–3.
- [29] R. Beltran, F. Raab, and A. Velazquez, "HF outphasing transmitter using class-E power amplifiers," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 757–760.
- [30] *CA-26 Data Sheet* Marki Microwave, Morgan Hill, CA, USA, 2011.
- [31] R. Hou, M. Spirito, J. Gajadharsing, and L. de Vreede, "Non-intrusive characterization of active device interactions in high-efficiency power amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, June 2013, pp. 1–3.
- [32] P. Roblin, "Large-signal vector measurement techniques with VNAs," in *Nonlinear RF Circuits and Nonlinear Vector Network Analyzers*. Cambridge, MA, USA: Cambridge Univ. Press, 2011, ch. 2, pp. 17–65.
- [33] T. Reveyard, T. Gasseling, D. Barataud, S. Mons, and J.-M. Nebus, "A smart load-pull method to safely reach optimal matching impedances of power transistors," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 1489–1492.

- [34] F. Casadevall and J. Olmos, "On the behavior of the LINC transmitter," in *Proc. IEEE Veh. Technol. Conf.*, May 1990, pp. 29–34.
- [35] A. Birafane and A. Kouki, "Sources of linearity degradation in LINC transmitters for hybrid and outphasing combiners," in *Proc. Can. Conf. Electr. Comp. Eng.*, May 2004, vol. 1, pp. 547–550.
- [36] J. Yi, Y. Yang, and B. Kim, "Effect of efficiency optimization on linearity of LINC amplifiers with CDMA signal," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, May 2001, vol. 2, pp. 1359–1362.
- [37] L. Sundstrom, "Automatic adjustment of gain and phase imbalances in LINC transmitters," *Electron. Lett.*, vol. 31, no. 3, pp. 155–156, Feb. 1995.
- [38] S. Ampem-Darko and H. Al-Raweshidy, "Gain/phase imbalance cancellation technique in LINC transmitters," *Electron. Lett.*, vol. 34, no. 22, pp. 2093–2094, Oct. 1998.
- [39] A. Huttunen and R. Kaunisto, "A 20-W chireix outphasing transmitter for WCDMA base stations," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2709–2718, Dec. 2007.
- [40] A. Birafane and A. Kouki, "On the linearity and efficiency of outphasing microwave amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 7, pp. 1702–1708, Jul. 2004.
- [41] S. Moloudi and A. Abidi, "The outphasing RF power amplifier: A comprehensive analysis and a class-B CMOS realization," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1357–1369, Jun. 2013.



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Prof. Popović was the recipient of the 1993 and 2006 Microwave Prizes presented by the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) for the best journal papers and the 1996 URSI Issac Koga Gold Medal. In 1997, Eta Kappa Nu students chose her as a Professor of the Year. She was the recipient of a 2000 Humboldt Research Award for Senior U.S. Scientists of the German Alexander von Humboldt Stiftung. She was elected a Foreign Member of the Serbian Academy of Sciences and Arts in 2006. She was also the recipient of the 2001 Hewlett-Packard (HP)/American Society for Engineering Education (ASEE) Terman Medal for combined teaching and research excellence.

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