HIGH-EFFICIENCY POWER AMPLIFIERS FOR LINEAR TRANSMITTERS

by

NÉSTOR DAVID LÓPEZ

B.S., University of Puerto Rico, 2001

M.S., University of Puerto Rico, 2003

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written by Néstor David López

has been approved for the

Department of Electrical and Computer Engineering

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Prof. Zoya Popović

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Prof. Dragan Maksimović

Date _____

The final copy of this thesis has been examined by the signatories;

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High-Efficiency Power Amplifiers for Linear Transmitters

Thesis directed by Prof. Zoya Popović

Digital modulation techniques used in wireless communications with radio frequency (RF) carriers can increase channel capacity, improve transmission quality, enhance security, and provide services not possible with analog modulation. Improving spectral efficiency by allowing the envelope of the RF signal to vary with time can enhance channel capacity. Envelope variations introduce RF power amplifier (RFPA) linearity requirements. The power conversion efficiency of RFPAs operating in linear modes is limited to less than 25% for signals with high envelope variations. Poor conversion efficiency leads to significant dissipated power that is wasted as heat, and it also shortens the lifetime of battery operated equipment.

This thesis focuses on the design and implementation of high-efficiency but non-linear RFPAs that can be linearized with dynamic biasing techniques, such as polar modulation. In polar modulation the signal that is modulated in both amplitude and phase is separated into two components; an envelope varying baseband signal that contains the amplitude modulation, and a phase modulated signal with constant envelope. The non-linear PA can efficiently amplify the constant envelope signal, while envelope variations can be injected by the supply. The RFPA can reconstruct the amplitude and phase modulated signal by operating as a time-domain multiplier. A 56% efficient linear polar transmitter with +20 dBm of output power was designed and implemented for the EDGE modulation scheme. This is the highest efficiency reported to date for a polar EDGE transmitter.

This thesis also studies the use of transistors such as GaN HEMTs, and SiC MESFETs in the design of high-power high-efficiency RFPAs and how they com-

pared to a high-efficiency RFPA implemented with standard Si LDMOS. Wide-bandgap semiconductors have better intrinsic material properties than silicon, i.e. larger energy gap (support higher internal electric fields before breakdown), lower relative permittivity (lower capacitive loading), higher thermal conductivity (higher heat handling), and higher critical electric fields (higher RF power). A 45-W, 87% efficient UHF non-linear transmission line hybrid Class-E RFPA is designed with a GaN HEMT on a SiC substrate.

Dedication

A Mabel, Lourdes, Jackie y Esther.

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Introduction & Thesis Outline

1.1 Introduction

Digital modulation techniques used in wireless communications with radio frequency (RF) carriers increase channel capacity, improve transmission quality, enhance security, and provide services not possible with analog modulation [1]. Improving spectral efficiency by allowing the envelope of the RF signal to vary with time can enhance channel capacity. Envelope variations introduce radio frequency power amplifier (RFPA) linearity requirements. A metric used to quantify required linearity is the crest factor or the peak-to-average ratio (PAR), which relates to waveform peak amplitude to its mean value:

$$\mathrm{PAR} = 10 \log_{10} \left[\frac{\max(|x(t)|^2)}{\mathrm{mean}(|x(t)|^2)} \right] \tag{1.1}$$

where $x(t)$ is the signal to be transmitted.

The envelope is constant for signals that have predominantly phase and frequency modulation such as Q-PSK or G-MSK (GSM) and the corresponding PAR is 0 dB. This means that a non-linear high-efficiency RFPA can used to amplify such signals. On the other hand, WCDMA signals have a large peak-to-average

ratio, between 9 dB and 11 dB, requiring a RFPA that is able to amplify both small and large amplitude signals with equal fidelity. One way to achieve linearity is to back-off the RFPA input power from its 1 dB compression point by an amount of approximately the PAR value to accommodate the signal envelope variation [1]. Backing-off the amplifier input power significantly degrades power consumption efficiency as well as average output power. For example, a 100 W (+50 dBm) amplifier for WCDMA is needed for transmitting an average power of 10 W (+40 dBm). The corresponding mode of RFPA linear operation is typically in class A or backed-off class AB modes. These linear operating modes limit the efficiency of the RFPA to less than 25% where linearity is traded for efficiency [2].

The goal of this thesis is to make significant contributions towards obtaining linear amplifiers that are simultaneously efficient. A number of researchers have investigated dynamic biasing techniques that can simultaneously provide high efficiency and good linearity, and most notable examples are Envelope Elimination and Restoration (EER), and polar modulation [3] - [11]. Dynamic biasing techniques achieve linearity by allowing the RFPA supply voltage to follow the signal envelope, since the output voltage to a constant load vary proportional to the supply voltage. These types of transmitters are more complex, and the total transmitter efficiency depends on both the RFPA and the supply modulating circuit efficiency, as shown if Figure 1.1.

Polar transmitters achieve high-efficiency with the use of both a high-efficiency envelope tracker (ET) and a high-efficiency RFPA. Switch-mode power supplies (SMPSs) are ideal for the role of envelope tracking, because they can achieve ultra high-efficiencies, are light and can step up or down the DC voltage. High-efficiency class-E non-linear power amplifiers are ideal for the role of the RFPA because they can also achieve ultra high-efficiencies and more than that, the voltage delivered to a constant load is linearly proportional to the supply voltage, achieving relatively

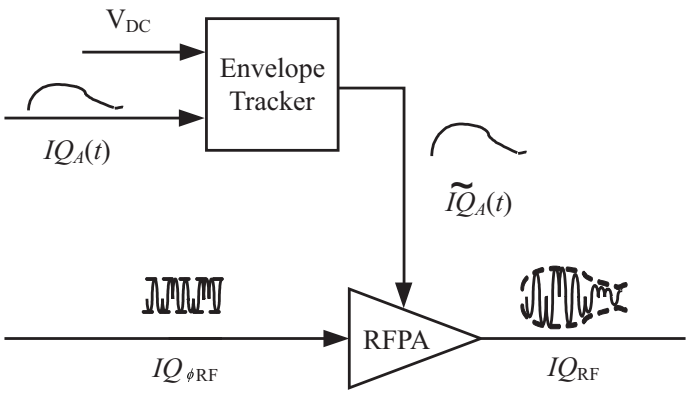


Figure 1.1: Diagram of a polar transmitter. The RFPA is fed with two signals; $IQ_{\phi\mathrm{RF}}$ and $\widetilde{IQ}_A$. $IQ_{\phi\mathrm{RF}}$ is a phase modulated RF signal with constant envelope, while $\widetilde{IQ}_A$ is a baseband signal that contains the signal envelope. The RFPA functions as a time-domain multiplier, reconstructing the desired signal IQ_{RF}. Time alignment between the two signals is crucial to avoid distortion. The total transmitter efficiency is the product of the efficiency of the envelope tracker and the RFPA.

linear amplifiers without the need of pre-distortion techniques.

This thesis discusses the design of high-efficiency non-linear class-E power amplifiers that can be linearized with dynamic biasing techniques such as polar modulation. Results are presented for two polar transmitters; a 10-GHz polar transmitter implemented with a transmission line class-E RFPA and a linear assisted switch-mode power supply as the ET [12] - [14], and a 880-MHz polar transmitter implemented with a hybrid transmission line class-E RFPA and a Buck converter as the ET [15] - [17]. Also, UHF Class-E high-efficiency high-power amplifiers are design with wide-bandgap transistors and their performance is compared to an amplifier implemented with standard Si LDMOS using the same techniques [18] - [19].

The main motivation of this work is to save the prime resource that is power. Figure 1.2 shows the normalized dissipated power as a function of supply efficiency. If a power amplifier is 25% efficient, it means that for every 1 W of RF output power, the power supply needs to provide 4 W while the remaining 3 W

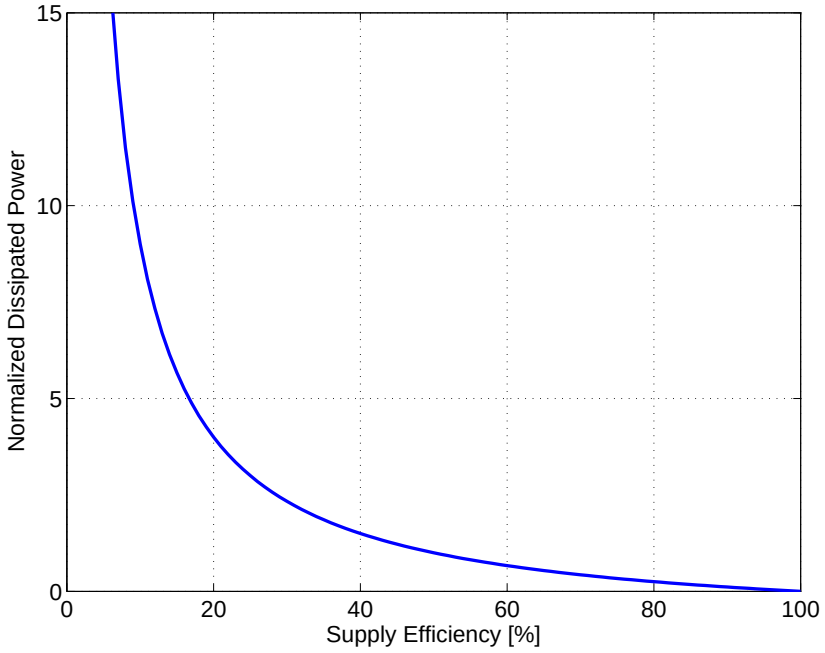


Figure 1.2: Normalized dissipated power versus efficiency. Typical RFPA efficiencies for linear amplifiers is below 25%. Due to the nonlinear relation between dissipated power and efficiency, for efficiencies below 40%, increasing the efficiency by a small amount reduces significantly the dissipated power enhancing the lifetime of battery operated equipment and reducing required heatsink mass.

are dissipated as heat. This ratio is maintained as the RF output power increases to 100 W or 500 W of RF output power, where heat dissipation increases to 300 W and 1.5 kW respectively. Increasing the amplifier efficiency from 25% to 40% reduces the amount of dissipated power by half, so that the dissipated power is only 1.5 W for every 1 W of RF output power. This also means that the heatsink mass can be halved or that a cellphone battery will last 1.6 times longer. Farther increasing the efficiency to 75% means that only 1/3 W is dissipated for every 1 W of RF output power. In this case the heatsink mass is farther reduced to approximately a tenth of the original mass at 25% efficiency and a cellphone battery will last 3 times as long. Due to the nonlinear relation between dissipated power and efficiency, for efficiencies below 40%, increasing the efficiency by a small amount reduces significantly the dissipated power enhancing the lifetime of battery op-

erated equipment and reducing the heatsink mass. This work demonstrate that efficiencies higher than 50% can be achieve in polar transmitters, while maintaining transmitter linearity.

1.2 Thesis Organization

Following this introductory chapter which briefly describes the motivation for the work, six additional chapters provide details of the background and contributions as follows:

- **Chapter 2** - This chapter covers the basic definitions used throughout the thesis and gives a background of different modes of RFPA operation. In this context, the choice of switch-mode class-E operation used in the other chapters and its transmission line version is explained. In addition to basics of power amplifiers, this chapter also gives a brief discussion of different methods that can be used to obtain high-efficiency and linear PAs.

- **Chapter 3** - This chapter discusses in detail polar transmitters, which is the particular choice of linearity adopted in this thesis. As an example, a 10-GHz polar transmitter is implemented with a transmission line class-E RFPA and a linear assisted switched-mode power supply as the envelope tracker. Load-pull data under Cartesian and polar two-tone excitation is presented for amplifier output impedance matching selection.

- **Chapter 4** - This chapter covers the design, implementation and performance of a high-efficiency linear polar transmitter for EDGE modulated communication signals (one of the current standards for cellular communications). The 880-MHz transmitter uses a non-linear transmission line hybrid class-E high-efficiency RFPA and an ultra-fast high-efficiency switch-

mode power supply as the envelope tracker. The polar transmitter meets the EDGE envelope mask with +20 dBm of output power and 56% efficiency.

- **Chapter 5** - This chapter covers the steps for the design of high-efficiency UHF PAs with $P\mathrm{OUT} > 50\,\mathrm{W}$. The steps are illustrated with the design of a high-efficiency RFPA that uses a GaN HEMT on a SiC substrate prototype from RFMD as the active device. Load-pull characterization shows a significant tradeoff between optimum output power and optimum efficiency contours. An optimization procedure based on a weighted Euclidean distance is developed in order to take this tradeoff into account for the final amplifier design.

- **Chapter 6** - This chapter discusses the design and implementation of UHF high-efficiency power amplifiers with four different transistor technologies; GaN HEMTs on a Si substrate, GaN HEMTs on a SiC substrate, SiC MESFETs and Si LDMOS. The goal is to achieve more than 40 W of output power with over 80% drain efficiency at 370-MHz with four different device technologies, Si LDMOS being an old and established technology while the others are emerging new semiconductor devices. The prototype amplifiers are compared in terms of performance and static distortion.

- **Chapter 7** - This chapter highlights the contributions of the presented work, gives additional examples of the proposed optimization procedure introduced in Chapter 5 and discusses future work.

Chapter 2

Background

2.1 Introduction

As discussed in Chapter 1, it is a challenge to design high-efficiency and linear power amplifiers. The digital modulation schemes used to enhance data rates in a limited bandwidth result in signals with PAR as high as 10 dB. The linear RFPAs used to amplify these signals typically suffer from low power conversion efficiency. There are two trends to conciliate linearity and efficiency; (1) enhance the efficiency of linear amplifiers and (2) enhance the linearity of high-efficiency non-linear power amplifiers. An overview of these techniques is presented in this chapter, but first some basic definitions are given along with an overview of classes of PA operation and PA testing procedures.

2.2 Efficiency Definitions

In the amplification process, the RF input signal ($P_{\text{IN RF}}$) is amplified by converting available DC power (P_{DC}) to RF output ($P_{\text{OUT RF}}$). The remainder of the power not converted to $P_{\text{OUT RF}}$ is dissipated as heat. The closed system, as shown in Figure 2.1, has two inputs, $P_{\text{IN RF}}$ and P_{DC} and two outputs $P_{\text{OUT RF}}$ and

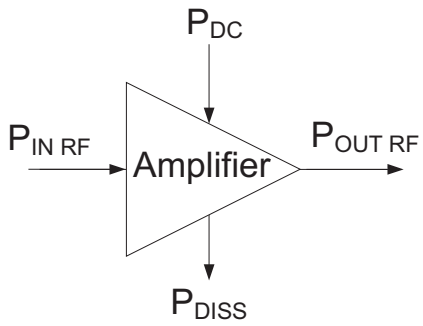


Figure 2.1: Power diagram of an RFPA. The inputs are $P_{\text{IN RF}}$ and P_{DC} and the outputs are $P_{\text{OUT RF}}$ and P_{DISS}. The P_{DC} not converted to $P_{\text{OUT RF}}$ is dissipated as heat.

P_{DISS}. Because this system has multiple inputs there are several ways to define power conversion efficiency. The equations to be presented next assume power levels to be given in Watts. The supply efficiency (η_{S}), relates the consumed DC power to the obtained $P_{\text{OUT RF}}$ and it is given by

$$\eta_{\text{S}} = \frac{P_{\text{OUT RF}}}{P_{\text{DC}}} \tag{2.1}$$

This ratio is also known as collector efficiency (η_{C}) or drain efficiency (η_{D}) depending on whether a bipolar or a FET is used as the active device. This ratio does not takes into account $P_{\text{IN RF}}$, that might be significant for RFPAs. The power-added efficiency (PAE) takes into account this input power and is given by

$$\text{PAE} = \frac{P_{\text{OUT RF}} - P_{\text{IN RF}}}{P_{\text{DC}}} \tag{2.2}$$

$$= \frac{P_{\text{OUT RF}} - \frac{P_{\text{OUT RF}}}{G_{\text{RF}}}}{P_{\text{DC}}} \tag{2.3}$$

where G_{RF} is the amplifier RF gain. Comparing η_{S} to PAE, it is evident that PAE is always smaller than η_{S} and is a more conservative number to quote for efficiency. The difference between these two power ratios increases when G_{RF} decreases. A third way to define efficiency of an amplifier is with the overall efficiency and is

defined by

$$\eta_{\text{overall}} = \frac{P_{\text{OUT } RF}}{P_{\text{DC}} + P_{\text{IN } RF}} \tag{2.4}$$

Although η_{overall} gives the best indicator to the dissipated power P_{DISS}, η_{S} and PAE are the two most common methods to quote RFPA efficiency.

2.3 PA Sweeps

Figure 2.2 shows a diagram of a bench for testing PAs where all impedances are matched to Z_0. All the parts are discussed in Chapter 5. The setup allows calibration and measurement of $P_{\text{IN RF}}$ and $P_{\text{OUT RF}}$. Once a prototype of an amplifier is designed, the characteristic impedance Z_0 (usually $50\,\Omega$) is presented to the input and output of the RFPA. The setup allows for several testing methods such as, input power sweep and supply voltage sweep that are the most useful for polar PA design:

- **Input Power Sweep** - the amplifier is biased at the desired quiescent point. $P_{\text{IN RF}}$ is increased within a defined range and parameters such as $P_{\text{IN RF}}$, $P_{\text{OUT RF}}$, gain, η_{S} and PAE are measured and recorded. This type of sweep allows measurements such as 1 dB compression point and drive level for optimum PAE.

- **Supply Voltage Sweep** - the input power is fixed, usually at the value that optimizes PAE and the supply voltage is swept within a defined range. Again, parameters such as $P_{\text{IN RF}}$, $P_{\text{OUT RF}}$, gain, η_{S} and PAE are measured and recorded as a function of supply voltage. In this type of sweep it is also important to measure parameters such as AM-to-AM and AM-to-PM distortion. AM-to-AM relates the supply voltage to the output voltage

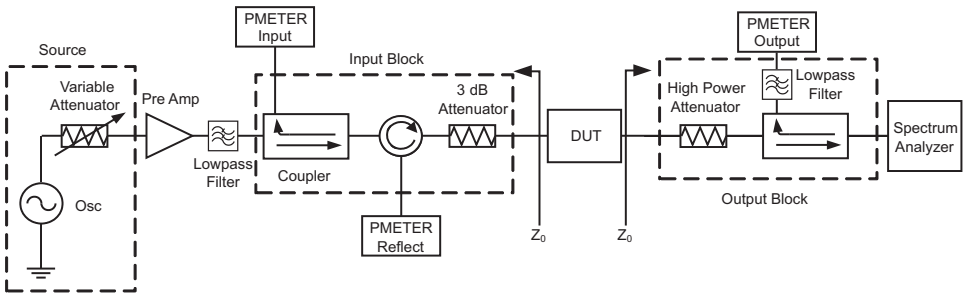


Figure 2.2: Diagram of a bench setup for testing PAs where all impedances are matched to Z_0. The setup allows to carefully calibrate and perform input power and supply sweeps to measure parameters such as $P_{\text{IN RF}}$, $P_{\text{OUT RF}}$, gain, η_S and PAE.

across a constant load. In polar transmitters it is desirable for this relation to be linear. The AM-to-PM relates how the delay through the amplifier varies as a function of the supply voltage. In polar transmitters it is desired for this response to be flat. Supply voltage sweeps are important when implementing dynamic biasing techniques.

2.4 Classic Amplifier Modes of Operation

The classic amplifiers mode of operation, such as Class-A, Class-AB, Class-B, and Class-C are defined in terms of conduction angle, 2θ [20]. In all the cases matching conditions are such that maximum output power is achieved. Excellent references about amplifier modes of operation are [2], [20] - [22]. The conduction angle (Figure 2.3) is defined as the portion of the RF cycle during which the device is in the active region [20] and it is a function of drive level, as well as the quiescent bias point [2].

- **Class-A** - Class-A amplifiers are linear amplifiers and they are biased so that the transistor remains in the active region during the entire RF cycle and the conduction angle is 2θ=360°. A drawback of Class-A amplifiers is

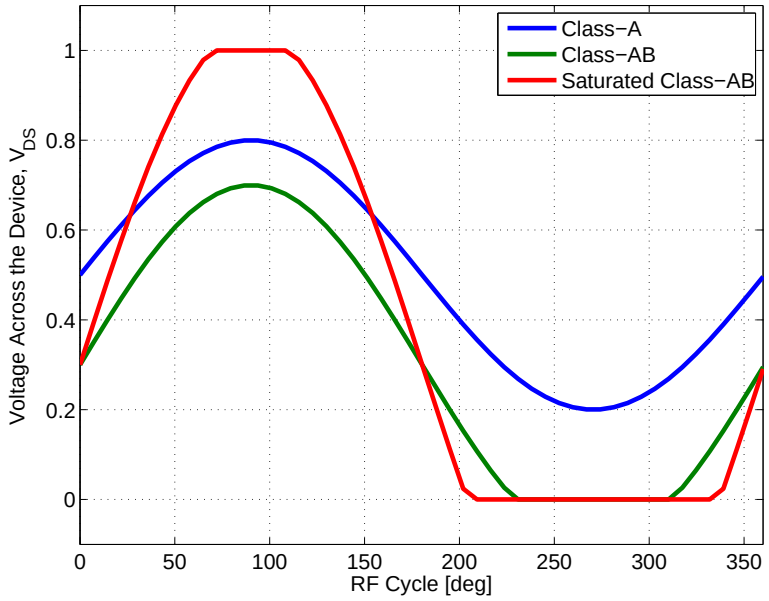


Figure 2.3: Voltage waveform across the transistor versus RF cycle. In Class-A (blue) the transistor remains in the active region during the entire RF cycle (360°). In Class-AB (green) the transistor remains in the active region between $180° < 2\theta < 360°$ and it is driven into cut-off for part of the RF cycle. For large input signals the transistor can also be driven into saturation (red).

that significant DC power is dissipated even if no RF input is present. The maximal theoretical supply efficiency is 50%.

- **Class-AB** - The conduction angle for Class-AB amplifiers is between $180° < 2\theta < 360°$, so that the transistor remains in the active region for more than 50% but less than of the full RF cycle. They are not linear amplifiers and signals with an amplitude-modulated envelope will be distorted significantly at peak power levels. However, the change in conduction angle causes a useful increase in efficiency at the expense of drive power and gain [2].

- **Class-B** - For transistor to operate in this mode the conduction angle is set to $2\theta = 180°$ so that the transistor remains in the active region during 50% of the RF cycle. The theoretical optimum efficiency for this mode is 78.5% [2] at the expense of gain reduction compared to Class-AB. [2] suggests the use

of high gain technologies, such as GaAs HBT and pHEMT to compensate for the gain reduction in this mode of operation.

- **Class-C** - In this mode the conduction angle is small (2θ <180°) and the transistor remains in the active region for less than 50% of the RF cycle. This mode of operation is highly nonlinear; the RF input signal turns "ON" the device and the gain is highly dependent upon input power.

One of the main advantages of reducing the conduction angle is efficiency enhancement, in the trivial case less power is dissipated with no input drive. Class-B and Class-C are biased so that no power is consumed in the absence of input drive. Modulation types such as FM or GMSK (GSM), do not require linear amplification of the input signal allowing the use of these efficient modes of operations.

2.5 RF Power Amplifiers with Harmonic Terminations

Device nonlinearities are exhibited as generation of harmonics and intermodulation products in the output RF signal. These harmonics can be used to shape the voltage and current waveforms across the device. For example, in Class-F operation the harmonics are terminated so that the voltage waveform across the transistor is a square wave and this leads to benefits in both power and efficiency [2]. The number of terminated harmonics depends on several parameters, e.g. the f_t of the device, its output capacitance (C_{OUT}), the complexity of the circuit, and passive circuit insertion loss.

At microwave frequencies, transmission line stubs can be used to implement harmonic terminations [23]. This passive circuitry can be designed very precisely

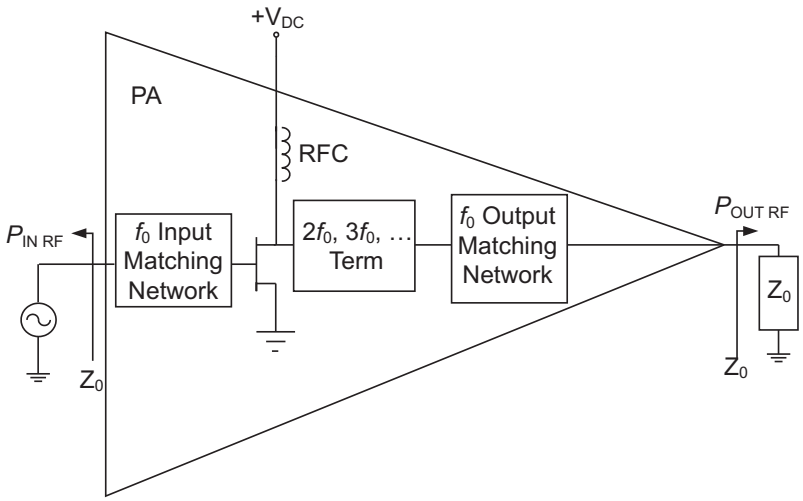


Figure 2.4: Diagram of transistor with input and output matching networks. The output matching network contains a pre-matching circuit that terminates harmonics with desired reflective terminations to shape the voltage and current waveforms across the device. Shaping the transistor waveforms can enhance, for example, power conversion efficiency.

with full wave EM software to present the desired impedance conditions. A brief description of modes of operation with terminated harmonics is given next.

- **Class-F** - In this mode the transistor operates as a saturated controlled current source [2]. Terminating the even harmonics with a short circuit, and the odd harmonics with an open circuit produce an approximate square-wave voltage and a half sine-wave current waveform across the device.

- **Class-F^{-1}** - In the inverse class-F the even harmonics are now terminated with open circuits, while the odd harmonics are terminated with short circuits, producing an approximate square-wave current and a half sine-wave voltage across the device.

- **Class-E** - For Class-E operation all the harmonics are terminated with an open circuits, while the fundamental is terminated with a particular impedance that achieves soft-switching. The next section discusses the

Class-E mode in greater depth.

- **Class-E^{-1}** - In the inverse Class-E, again the fundamental impedance is matched to a particular impedance that achieves soft-switching, but now the harmonics are terminated with a short circuit.

- **Class-J** - This mode is similar to a Class-AB amplifier with a large shunt capacitance following the device. This capacitance is of precise value so that the harmonics are shorted, but the fundamental impedance can still be matched [2].

Because power amplifiers are driven with large signals they usually display strong nonlinear behavior. The active devices are driven into saturation or cut-off for a certain portion of the RF cycle. Modeling these strong nonlinear effects is a difficult task, even if CAD models and tools are available [20]. The load-pull technique, discussed in more detail in Chapter 5, can be used to obtain an empirical model for the active device as a starting point for amplifier design.

2.6 Class-E Power Amplifiers

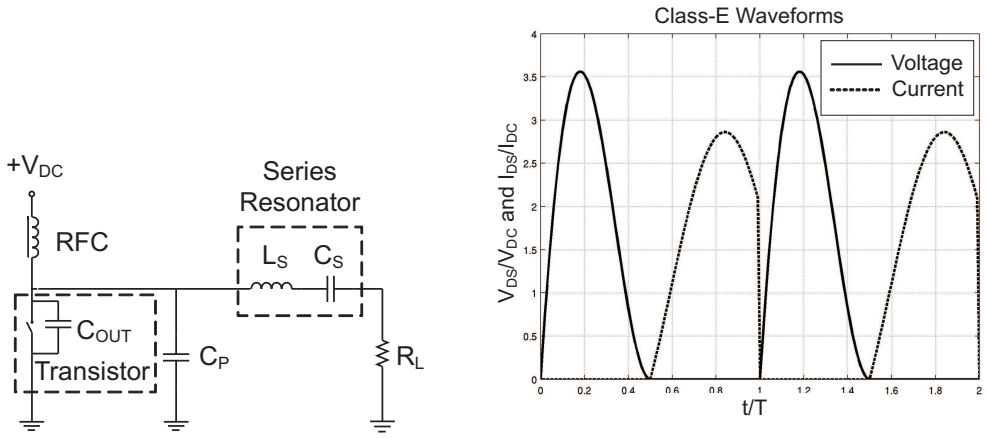
There are several sources of loss in power amplifiers: dissipated power in the active device; loss due to power in generated harmonics; insertion loss of input and output matching networks; loss in the bias network; losses in connections to the outside world; and radiation loss. However, the dominant loss is the dissipated power in the active device due to simultaneous presence of V and I. This loss can be minimized by operating the transistor as a switch. Ideal switches have this temporal orthogonality by instantaneous toggling between open and short circuit conditions so that there is zero current if the switch is open and zero voltage when the switch is close. In reality, when operating transistors as switches there

are two sources of loss; (1) the transistor ON resistance (R_{ON}) responsible for the presence of voltage under the short circuit condition, and (2) the output capacitance (C_{OUT}) that limits how fast can the switch toggle between states also producing simultaneous presence of V and I.

In practice, R_{ON} can be made very small and depends on the transistor power capabilities and technology. C_{OUT} also depends on these parameters and it is responsible for limiting the maximal frequency the transistor can operate as a switch. At low frequencies (hundred of kHz range) switch-mode power supplies can achieve efficiencies in the order of 90% [24]. As the operating frequency increases, resonant techniques such as zero-voltage-switching (ZVS) and soft-switching help to decrease power lost in C_{OUT} by discharging it right before the switch is closed. In soft-switching (Class-E) the voltage across the transistor is not only zero, but its derivative is also zero.

Figure 2.5(a) shows a diagram of the classical Class-E amplifier. The transistor is modeled as a switch with an intrinsic output capacitance and it is followed by a series resonator (L_{S} and C_{S}). Shunt capacitance (C_{p}) can be added externally at lower frequencies to shape the voltage and current waveforms across the device. Figure 2.5(b) shows there is no overlap between ideal voltage and current waveforms across the device leading to a 100% efficiency assuming no transient effects and zero ON resistance. An important characteristic of Class-E is that the voltage across the device can be higher than $3.56\times V_{\mathrm{DC}}$. V_{DC} needs to be kept below $V_{\mathrm{DSS}}/3.56$, where V_{DSS} is the breakdown voltage of the transistor, to avoid permanently damaging the device.

In Class-E operation the transistor behaves as a switch; the device is biased close to cut-off and driven into compression. The transistor turns ON and OFF with the RF drive which also provides the switching frequency. For the device to operate in ideal Class-E mode, all the harmonics must be terminated in an open



(a) (b)

Figure 2.5: (a) Diagram of the Class-E power amplifier. The transistor operates as a switch with its intrinsic output capacitance and it is followed by a series resonator (L_S and C_S). Additional shunt capacitance (C_P) can be added to shape the waveforms across the device. (b) Voltage and current waveforms across the device. Ideal maximum efficiency in Class-E mode is 100%. An important characteristic of Class-E is that the voltage across the device can be higher than $3.56\times V_{DC}$. V_{DC} needs to be kept below $V_{DSS}/3.56$, where V_{DSS} is the breakdown voltage of the transistor, to avoid permanently damaging the device.

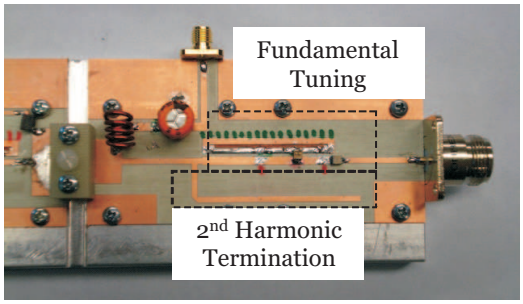
circuit, while the fundamental is matched to the Class-E impedance which depends on the operating frequency and the device intrinsic output capacitance [23], [25] - [30]; and is shown to be:

$$Z_E = \frac{0.28}{2\pi f_s C_{OUT}} e^{j49^\circ} \tag{2.5}$$

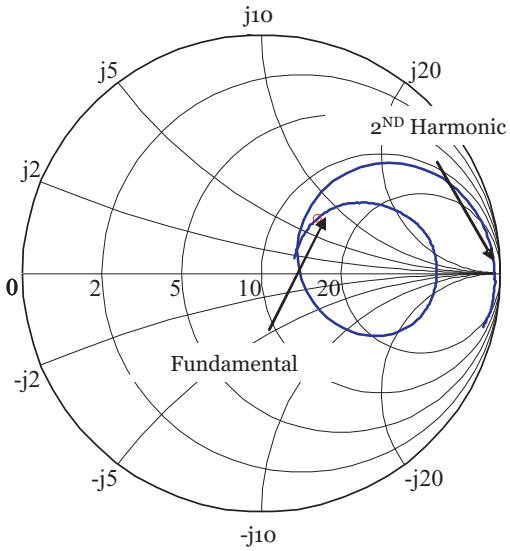
Class-E power amplifiers have been shown to achieve 95% in the low MHz range and 70% drain efficiency at X-Band [25] - [31]. For excellent reviews on Class-E operation the reader is refered to [20] - [22], [32], [34].

2.6.1 Transmission-Line Class-E

Lumped-component losses and parasitic effects are significant at microwave frequencies and the transmission line class-E PA is more appropriate in these frequen-



(a)



(b)

Figure 2.6: (a) Photograph of the output circuit of a transmission line hybrid class-E PA. A $\lambda_g/8$ open stub at a $\lambda_g/8$ distance is used to terminate the 2$^{\text{nd}}$ harmonic, where λ_g is the guided wavelength at the fundamental frequency. Lumped components are used to match the fundamental impedance. (b) Measured output impedance as a function of frequency in a 10-Ω Smith Chart. A high-impedance is presented at the 2$^{\text{nd}}$ harmonic, while the fundamental is matched to the class-E impedance, Z_{E}.

cies [32], [34]. In the transmission line class-E PA, harmonics are terminated with open stubs. The number of harmonics that should be terminated depend on the f_t and C_{OUT} of the device. Significant efficiency enhancement is usually achieved by terminating only the 2^{nd} harmonic. Additional harmonics can be terminated for small improvements in efficiency at the expense of circuit complexity. A $\lambda_g/8$ open stub at $\lambda_g/8$ distance from the transistor can be used to terminate the 2^{nd} harmonic, where λ_g is the guided wavelength at the fundamental frequency. The fundamental impedance matching is also implemented with stubs, but depending on the fundamental frequency the use of lumped components might be more appropriate, resulting in a transmission line hybrid class-E power amplifier as shown in Figure 2.6(a). Figure 2.6(b) shows the measured output impedance in a 10-Ω Smith Chart. A high impedance is presented to the transistor 2^{nd} harmonic, while the fundamental is matched to Z_{E}.

2.7 High Efficiency and Linear Power Amplifiers

As was discussed in the introduction there are two trends when designing high-efficiency linear power amplifiers: (1) enhancing the efficiency of linear power amplifiers, and (2) enhancing the linearity of high-efficiency power amplifiers. These two methods are discussed next.

2.7.1 Enhancing Efficiency of Linear PAs

As was mentioned in section 2.4 the easiest way to enhance the efficiency of a linear amplifier is to reduce the conduction angle as in Class-AB amplifiers. However, it is important to consider that there is a tradeoff between linearity and efficiency and that Class-AB amplifiers are not linear since they exhibit strong nonlinearities at peak power levels [2]. At the expense of little additional degradation in

linearity the efficiency can be farther enhanced if the harmonics are terminated as in Class-F or Class-J. It is important to point out that biasing conditions and fundamental matching networks are chosen to achieve amplifier linearity and output power. More advanced techniques such as the Doherty architecture also enhance the efficiency of linear amplifiers, this time by active load-pulling the RF load by applying current from a second RFPA. An excellent review of the Doherty amplifier is in [2]. This architecture can be costly for high power PAs because it uses 2 devices, however the output power is not doubled.

2.7.2 Enhancing Linearity of High-Efficiency PAs

There are two techniques to enhance the linearity of non-linear high-efficiency power amplifiers; (1) outphasing and (2) dynamic biasing. A brief description of these techniques is presented next.

Outphasing

The idea behind the outphasing technique is that an amplitude and phase modulated signal can be resolved into two constant envelope signals that are out of phase and that are applied to two highly efficient, highly nonlinear power amplifiers whose outputs are then summed appropriately [1]. The outphasing technique is covered in detail in [1], a brief description is presented here for completeness. The complex representation of a signal that is modulated in both amplitude and phase can be represented as

$$s(t) = r(t)e^{j\theta(t)} \tag{2.6}$$

For outphasing, this signal is split into two signals with constant amplitudes with modulated phases:

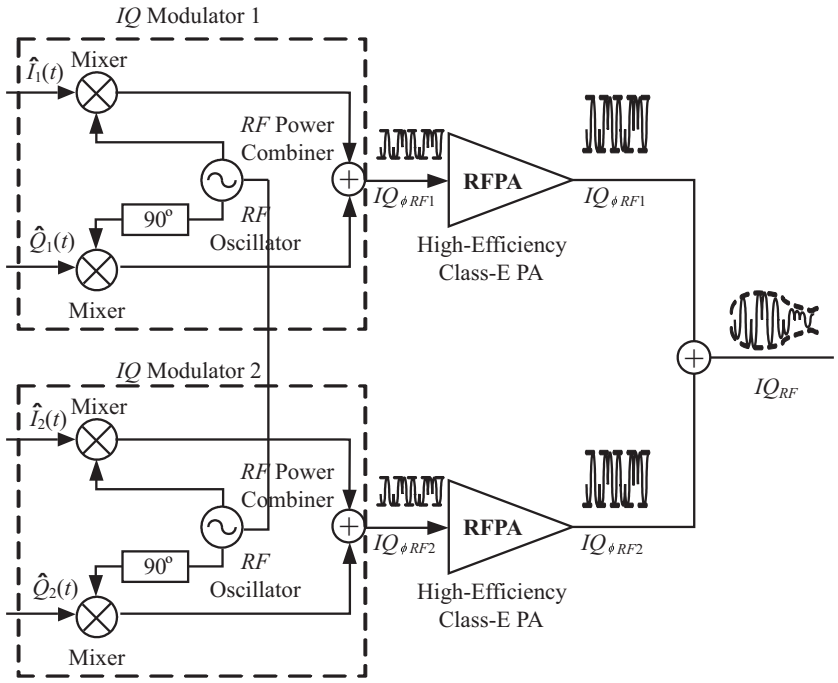


Figure 2.7: Diagram of an outphasing architecture. The signal that is modulated in both amplitude and phase is divided into two constant envelope phase modulated signals. This two signals when combined reconstruct the original signal. Due to the envelope removal, nonlinear high-efficiency RF power amplifiers can be used at each of the branches. Typical combiners will dissipate the out-of-phase component, however advance techniques such as Chireix combiners reduce this loss.

$$S_1(t) = s(t) - \xi(t) \tag{2.7}$$

$$S_2(t) = s(t) + \xi(t) \tag{2.8}$$

where $\xi(t)$ is the quadrature signal and is defined by

$$\xi(t) = js(t)\sqrt{\frac{r_{\max}^2}{r^2(t)} - 1} \tag{2.9}$$

When combining these two signals in a power combiner, the in-phase signal components add together and the out-of-phase signal components cancel out. Because these two signals have constant envelopes, non-linear high-efficiency power

amplifiers can be used in each of the branches. Imperfections in the system such as path imbalance (gain and phase), result in distortion. However, predistortion techniques can be used to compensate for some of these nonidealities. Traditional combining techniques are lossy because they dissipate the out-of-phase component. However, recycling techniques such as [37], [36] can be used to reduce this loss. More advance combining techniques such as Chireix architecture [1], [2] can be used to efficiently combine the two signals.

Dynamic Biasing

Dynamic biasing techniques, such as Envelope Elimination and Restoration (EER) [3], [5] and polar transmitters [6] - [17], modulate the RFPA supply voltage to proportionally scale the output voltage across a constant real load. Figure 2.8(a) shows a diagram of an EER system. The amplitude and phase modulated RF signal is converted to polar form. This can be accomplished with an envelope detector to obtain the envelope signal that is used as a reference for an envelope tracker, and a amplitude limiter to remove all the envelope to produce a constant envelope phase modulated signal. The envelope tracker supplies the envelope signal to the RFPA through the supply. The RFPA is used as a time domain multiplier to amplify and reconstruct the RF signal. In polar transmitters, Figure 2.8(b), the signal conversion to polar form is done in the baseband digital domain but otherwise the principle is the same as EER. Chapter 3 talks in detail about polar transmitters and its components, which are the approach taken in this thesis.

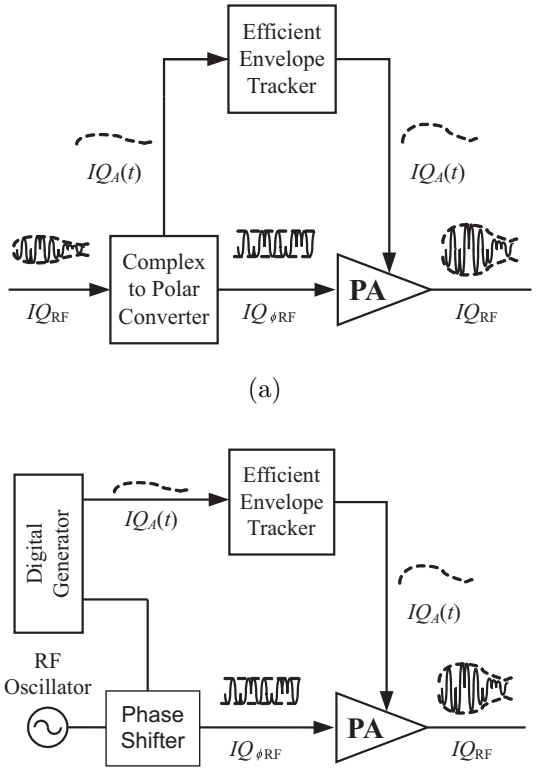


Figure 2.8: Diagrams that illustrate dynamic biasing techniques. The RFPA is fed with two signals; $IQ_{\phi\mathrm{RF}}$ and $\widetilde{IQ}_A$. $IQ_{\phi\mathrm{RF}}$ is a phase modulated RF signal with constant envelope, while $\widetilde{IQ}_A$ is a baseband signal that contains the signal envelope. The RFPA functions as a time-domain multiplier, reconstructing the desired signal IQ_{RF}. Time alignment between the two signals is crucial to avoid distortion. The total transmitter efficiency is the product of the efficiency of the envelope tracker and the RFPA. In EER (a) the RF signal is divided into polar form, while in polar transmitters (b) the baseband signal is converted digitally to polar form.

Chapter 3

High-Efficiency Linear Polar Transmitters

3.1 Introduction

Polar modulation has become increasingly popular in RF transmitters due to its potential to simultaneously achieve linearity and efficiency [6] - [17]. Increasing the transmitter efficiency reduces heat dissipation and extends the lifetime of the battery in portable equipment. Digital modulation uses symbols that are encoded with in-phase (I) and quadrature (Q) baseband components. An IQ modulator is used to combine and frequency shift these two signals to the RF carrier, creating the modulated RF signal IQ_{RF} as shown in Figure 3.1.

Depending on the modulation scheme used, the IQ_{RF} signal might vary in both amplitude and phase. A polar representation of this signal is

$$IQ_A = |IQ_{\mathrm{RF}}| \tag{3.1}$$

$$IQ_{\Phi_{\mathrm{RF}}} = \frac{IQ_{\mathrm{RF}}}{|IQ_{\mathrm{RF}}|} \tag{3.2}$$

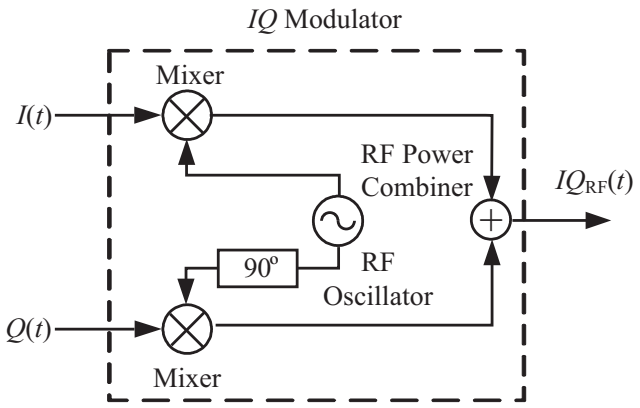


Figure 3.1: Diagram of an IQ modulator. The baseband I and Q signals modulate the RF carrier. The output is the RF modulated signal, IQ_{RF}.

The resultant is the baseband signal IQ_A and the constant amplitude phase modulated RF signal $IQ_{\Phi\mathrm{RF}}$. The original IQ_{RF} signal can be recovered from

$$IQ_{RF} = IQ_A \cdot IQ_{\Phi\mathrm{RF}} \tag{3.3}$$

A way to obtain the $IQ_{\Phi\mathrm{RF}}$ signal is with normalized $\hat{I}$ and $\hat{Q}$ of the form,

$$\hat{I} = \frac{I}{\sqrt{I^2 + Q^2}} \tag{3.4}$$

$$\hat{Q} = \frac{Q}{\sqrt{I^2 + Q^2}} \tag{3.5}$$

been the input to the IQ modulator of Figure 3.1.

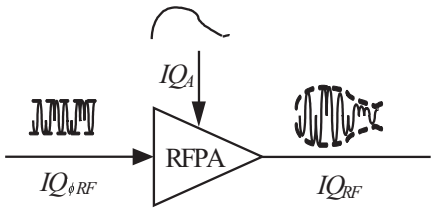


Figure 3.2: Diagram that illustrates polar modulation with an RFPA. The $IQ_{\Phi_{RF}}$ is the RF input to the PA while IQ_A is the supply voltage which changes with a bandwidth dictated by the envelope signal bandwidth. The RFPA operates as a time domain multiplier reconstructing the IQ_{RF} signal.

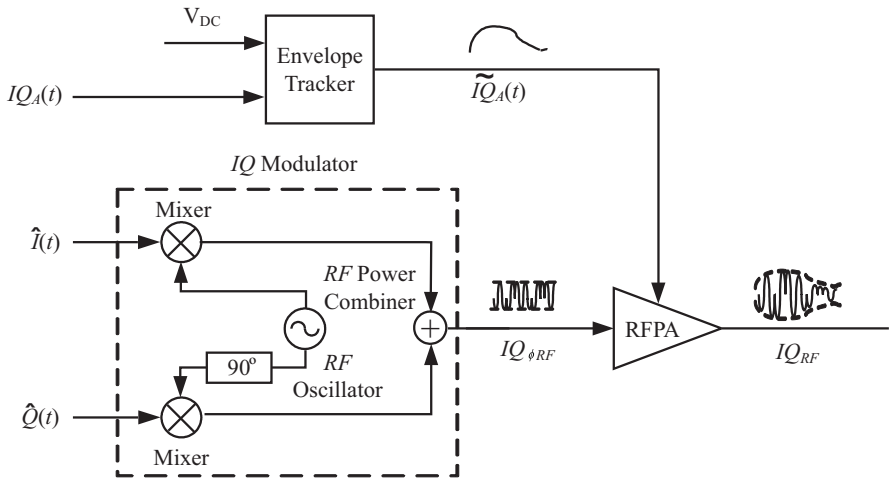


Figure 3.3: Diagram of a polar transmitter with baseband IQ_A, $\hat{I}$ and $\hat{Q}$ inputs. The envelope tracker has two inputs (DC supply and the reference IQ_A signal) and one output (low pass filtered $\widetilde{IQ}_A$). $\widetilde{IQ}_A$ is the tracked envelope signal that feeds the RFPA. Because envelope and biasing is provided by the tracker, the total efficiency depends on both the tracker and the RFPA.

As shown in Figure 3.2 supply modulating techniques, such as polar modulation and EER [3] implement the function of Equation 3.3 by operating the RFPA as a time domain multiplier that reconstructs the IQ_{RF} signal by utilizing the amplifier output power dependence to the supply voltage. Nothing is said in this diagram about what sort of RFPA is needed to perform this function and in practice people have used saturated Class-A, Class-AB or Class-E amplifiers for this role [6] - [17], [39] - [42]. Later in this chapter we will show that Class-E amplifiers are ideal for polar transmitters because the output voltage to a constant load is linearly proportional to the supply voltage.

Figure 3.3 shows a diagram of a polar transmitter. The envelope tracker supplies $\widetilde{IQ}_A$, a lowpass filtered version of IQ_A. Because $\widetilde{IQ}_A$ contains biasing and envelope variations, it handles similar power levels compared to the RFPA. The overall transmitter efficiency is given by,

$$\eta_{\text{Transmitter}} = \frac{P_{\text{OUT RF}}}{P_{\text{DC}}} \tag{3.6}$$

$$= \frac{P_{\text{ET}}}{P_{\text{DC}}} \cdot \frac{P_{\text{OUT RF}}}{P_{\text{ET}}} \tag{3.7}$$

$$= \eta_{\text{ET}} \cdot \eta_{\text{S}} \tag{3.8}$$

where P_{ET} and η_{ET} is the output power and the efficiency of the ET, while $P_{\text{OUT RF}}$ and η_{S} is the output power and the supply efficiency of the RFPA. From this equation we can conclude that it is not only important for the RFPA to be efficient, but to obtain a high overall transmitter efficiency, it is crucial that the envelope tracker is efficient and can provide the necessary envelope bandwidth.

3.2 Envelope Trackers

As was discussed in the previous section, the overall transmitter efficiency depends on the efficiency of the RFPA and the efficiency of the envelope tracker. One way to design ultra high-efficiency envelope trackers is with switch mode power supplies (SMPSs). SMPSs can achieve high efficiencies, are small, light, economic and have the capability to step-up or step-down voltages [43], [45]. However, for these converters losses increase with switching frequency and it is a challenge to design fast high-efficiency SMPSs. SMPSs can be assisted with linear amplifiers to cover larger bandwidths [43].

3.2.1 Switch-Mode Power Supplies

SMPSs can be implemented with transistors and diodes to step up or step down a supply voltage (V_{DC}). The output voltage depends on a reference signal converted usually to a duty cycle. There are several SMPSs configurations, such as Buck, boost, Buck-boost, and Ćuk converters. Each converter has its own properties;

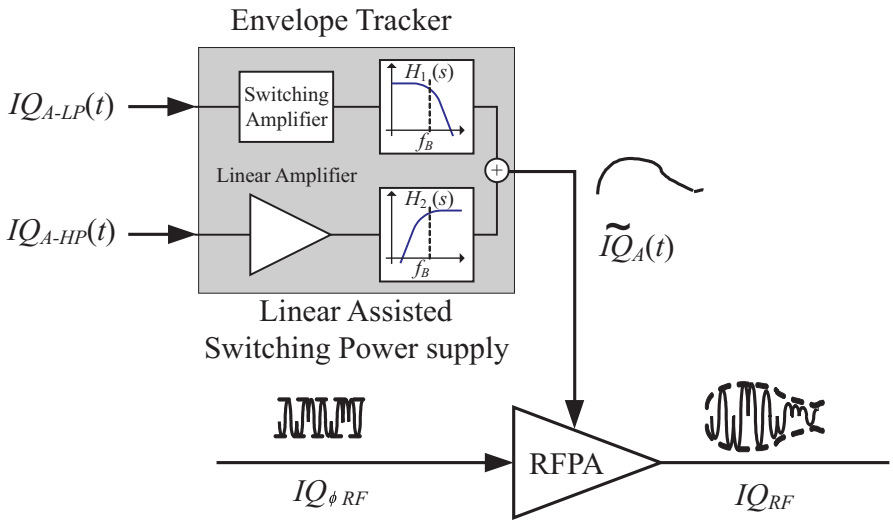


Figure 3.4: Diagram of a polar transmitter with the envelope tracker implemented with a linear assisted switching-power supply [14], [43], and [44]. The envelope signal IQ_A is band-separated into low (IQ_{A-LP}) and high (IQ_{A-HP}) frequency components. The low frequency component is supplied by a slow but ultra-efficient SMPSs, while the high frequency components are supplied by less efficient but fast linear amplifier.

for example, Buck converters can only step down the supplied voltage. To reduce switching harmonics, an SMPS is followed by a lowpass filter. The bandwidth of envelope signals such as WCDMA is in the order of 4 MHz [6]. In addition, the bandwidth provided by the tracker needs to take into account factors such as oversampling ratio. Because losses increase with frequency it is not possible to obtain high-efficiency with signal bandwidth exceeding the MHz range. However, linear amplifiers can be used to take care of the high frequency components, while the SMPS is responsible for supply the lower frequency envelope components.

3.2.2 Linear Assisted Switch-Mode Power Supplies

The envelope bandwidth of signals such as WCDMA is in the MHz range, but 85% of the envelope power is between DC and 300 kHz [6]. In such a system it makes sense to have an ultra efficient SMPSs to supply the power contained in the 300 kHz bandwidth while the remaining envelope spectrum is supplied by a

less efficient but high-bandwidth linear amplifier. In the case where the efficiency of the SMPSs is 90% and the efficiency of the linear amplifier is 30% the total envelope tracker efficiency is still on the order of 80%.

Figure 3.4 shows a diagram of a polar transmitter with the envelope tracker implemented with a linear assisted switching power supply [6], [14], [43], and [44], the envelope signal IQ_A, is assumed to have a bandwidth that might be on the order of couple of MHz is band-separated into low (IQ_{A-LP}) and high (IQ_{A-LP}) frequency components. The low frequency components are supplied by a slow ultra-efficient ($\tilde{9}0\%$) SMPSs, while the high frequency components are supplied by the linear amplifier. In [14] it is shown that depending on the signal statistics and the efficiency of the SMPSs and the linear amplifier, there is a band-separation frequency were efficiency is optimized.

When implementing this type of envelope tracker it is crucial to have a flat pass band response. For example, ripple, delay or amplitude unbalance between low and high frequency components will introduce distortion, which can be corrected by pre-distortion [46] - [49].

3.3 Class-E Power Amplifiers in Polar Transmitters

The class-E mode of operation lends itself well to the polar transmitter architecture. As shown in [30], for a 50% duty cycle of the switch drive, the voltage across the transistor is given by:

$$v_{\mathrm{DS}}(t) = \frac{I_{\mathrm{DS}}}{\omega_s \cdot C_{\mathrm{OUT}}}[\omega_s t - 1.86(\cos(\omega_s t - 32.5^\circ) - \cos(32.5^\circ))], \qquad (3.9)$$

where I_{DS} is the average drain current, C_{OUT} is the device nonlinear output capacitance, and f_s is the input signal frequency. If the DC supply voltage is provided

through an ideal RF choke, the average value of the switch voltage has to be equal to the DC drain supply voltage V_{DS}:

$$V_{\mathrm{DS}} = \frac{1}{T_s}\int_0^{T_s} v_{\mathrm{DS}}(t)dt = \frac{I_{\mathrm{DS}}}{\pi\omega_s C_{\mathrm{OUT}}} \tag{3.10}$$

By properly terminating the ideal class-E PA, the power delivered is

$$P_{OUT} = \frac{1}{2}R_{\mathrm{E}}I_{\mathrm{OUT}}^2 = \frac{1}{2}R_{\mathrm{E}}(1.86I_{\mathrm{DS}})^2 \tag{3.11}$$

where R_{E} is the real part of the optimal class-E load impedance, $Z_{\mathrm{E}} = R_{\mathrm{E}} + jX_{\mathrm{E}}$ and I_{OUT} is the magnitude of the output current i_{OUT}. From Equations 3.10 and 3.11 we obtain,

$$P_{\mathrm{OUT}} = \frac{1}{2}R_E(1.86 \cdot \pi \cdot \omega_s \cdot C_{\mathrm{OUT}})^2 V_{\mathrm{DS}}^2 \tag{3.12}$$

For a lossless output matching network, the output power is linearly proportional to V_{DS}^2. As a result, the output voltage of a class-E PA across a constant load can be linearly varied by varying the drain voltage:

$$V_{\mathrm{OUT}} = \pm\left(26 \cdot f_s \cdot C_{\mathrm{OUT}} \cdot \sqrt{R_{\mathrm{E}} \cdot R_{\mathrm{L}}}\right) V_{\mathrm{DS}} \tag{3.13}$$

In addition, the optimal efficiency and optimal load impedance are not affected by the bias variation, since the transistor current and voltage amplitudes only change with bias, but not their time-domain waveform shapes. The power can theoretically vary from zero to the maximal available power, but in practice the lowest power is limited by feedthrough, and the maximal power is constrained by the power handling of the device. In [13], and [12], the linearity of 10-GHz class-E PAs are examined and it is demonstrated that these highly saturated PAs can be linearized to some degree using polar modulation.

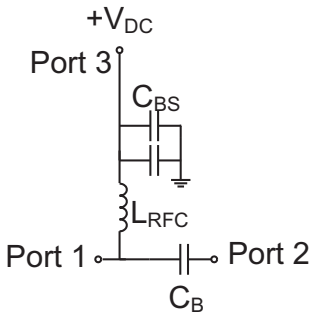


Figure 3.5: Diagram of a bias-tee with blocking capacitor (C_{B}), inductor (L_{RFC}), and shunt capacitors (C_{BS}) in the DC path. The basic function of the bias-tee is to diplex DC and RF signals.

3.3.1 Bias-Tee Design

Figure 3.5 shows the basic diagram of a bias-tee. The main purpose of the circuit is to diplex RF and DC signals. It is desired that the DC signal only flows from Port 3 to Port 1, while the RF signal only flows from Port 1 to Port 2. To deal with unstabilities and to ensure little V_{DC} variations it is a common practice to add a number of capacitors (C_{BS}) shunted in the DC path and to wind the inductor L_{RFC} in ferrite cores.

In polar transmitters the envelope of the signal is been fed through Port 3. Due to the large signal bandwidth, the bias-tee Port 3 to Port 1 path, needs to be re-design taking into account the expected frequency content and a lowpass filter approach is more appropriate. Figure 3.6 shows the measured S_{31} response for a bias-tee using an air core inductor and a ferrite. The bandwidth of the bias-tee implemented with an inductor with a ferrite is limited and will distort large bandwidth envelope signals when applying dynamic biasing.

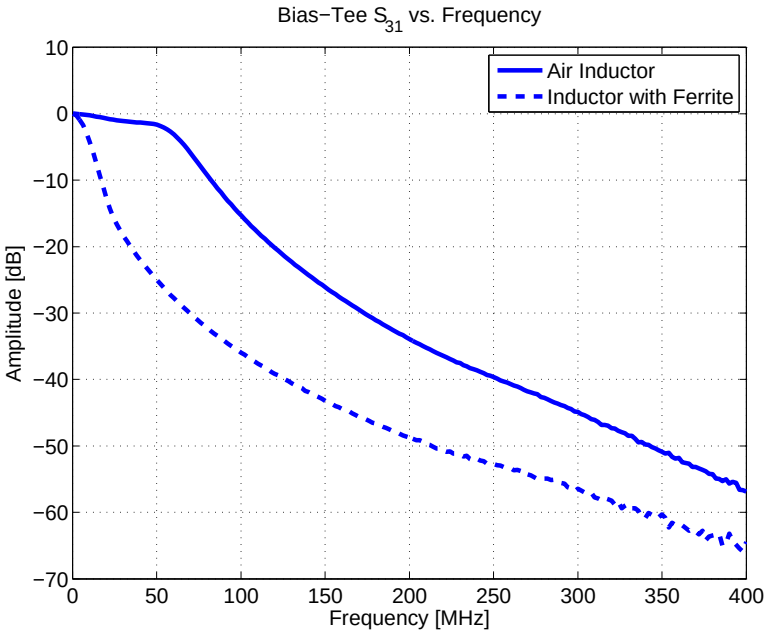


Figure 3.6: Measured S_{31} for bias-tee implemented with an air and ferrite core wound inductors. In polar transmitters the supplied voltage is intentionally varied to reproduce the signal envelope. Bias-tee bandwidth limitations will introduce distortion in the envelope signal.

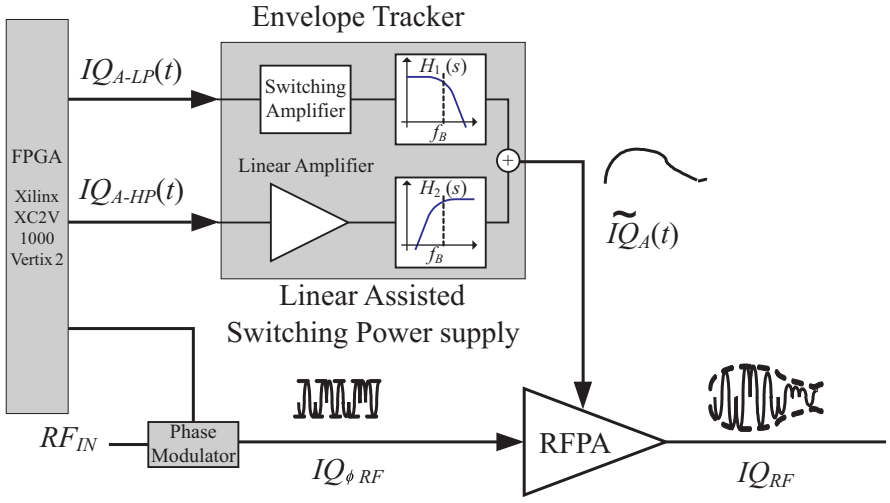


Figure 3.7: Block diagram of a polar system with FPGA digital control. The RFPA is a class-E 10-GHz MESFET amplifier [12]. The envelope signal is split into a low frequency component which controls a DC-DC converter and a high frequency component which provides additional envelope AC variations [14]. Phase variation is achieve with a digitally controlled phase shifter.

3.4 Example - Polar Two-Tone Architecture

In this section, the linearity of a polar transmitter implemented with a linear assisted switch-mode power supply as the envelope tracker and an ultra-nonlinear high-efficiency switched-mode class-E RFPA is examined [12]. The RF carrier is at 10 GHz, which is a higher frequency than most current commercial communication systems, but is a common frequency in other applications, such as radar. At carrier frequencies above 2 GHz, the circuit parasitics and device nonlinearities are more pronounced and difficult to model. The class-E X-band PA used in this study has been demonstrated in a two-stage efficient PA [30] and its linearity and EER operation were investigated in [13].

A diagram of the implemented system is shown in Figure 3.7. The digitally-controlled drain bias provides amplitude modulation of the output voltage through a ultra-efficient slow DC-DC converter in combination with a fast less efficient linear amplifier which provides the high frequency portion of the signal envelope. The signal is generated digitally and converted from IQ to polar form. The digital control of the bias allows allocation of the amplitude modulation between the slow and fast circuits in order to optimize efficiency for different modulated signals [43]. $IQ_{\Phi_{RF}}$ is generated from an 10-GHz RF source and a phase shifter.

3.4.1 Class-E PA Performance with a Single and Two-Tone Input

The class-E PA used throughout this work was designed using design equations as in [29] and load-pull characterization of a GaAs MESFET at 10 GHz, shown in Figure 3.8. The theoretical class-E impedance calculated from the output capacitance of this device is $24.7 + j28.4\,\Omega$. The maximum PAE of 59% at $27.2 + j31.4\,\Omega$ is obtained from load-pull measurements. P_{OUT}, gain, and η_{D} for the

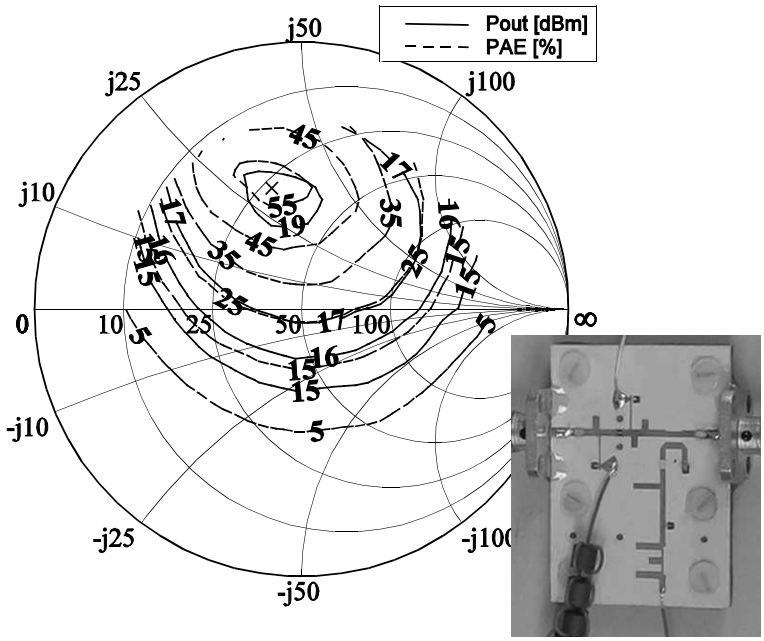
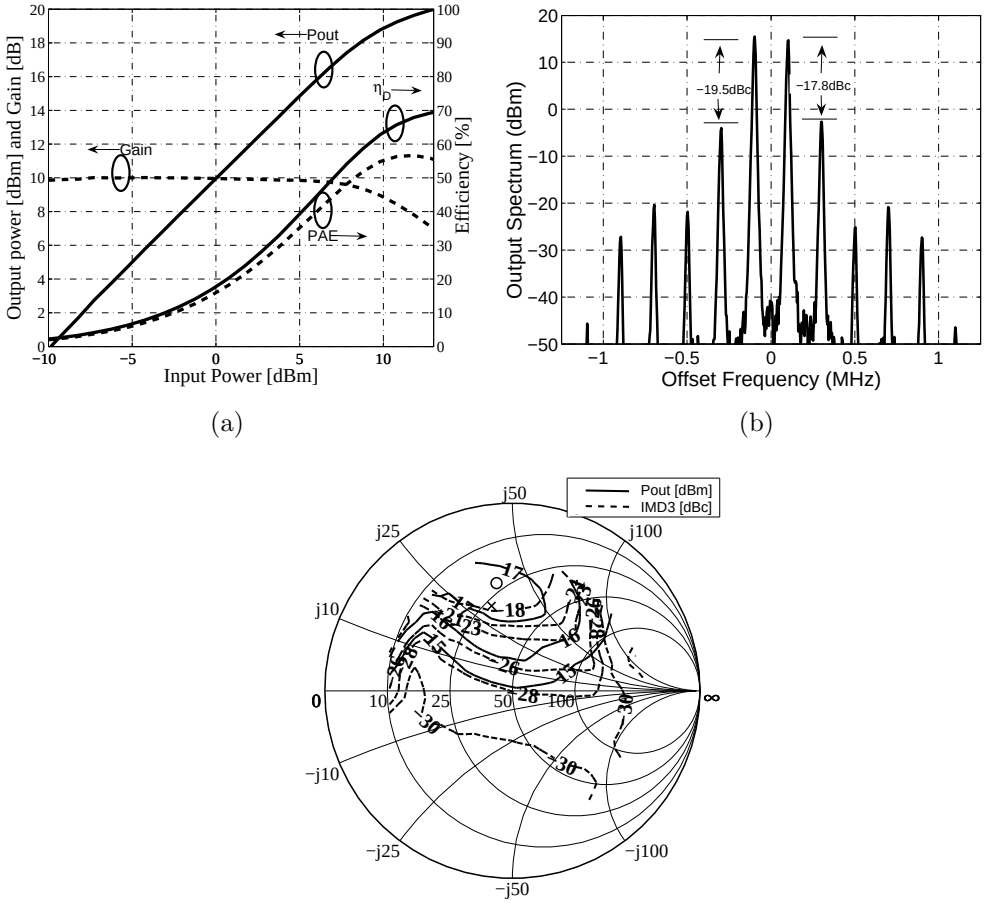


Figure 3.8: P_{out} (solid line) and PAE (dashed line) load-pull contours for MESFET AFM04P2 (Alpha industries). The class-E impedance ($27.2 + j31.4\,\Omega$) is indicated with '$\times$'. This amplifier was fabricated by Dr. Narisi Wang, formerly a student at CU.

PA are +19.9 dBm, 8.1 dB, and 64% respectively when the PA is compressed by 2.2 dB. The input impedance is matched to $8.2 + j27.3\,\Omega$.

Fig. 3.9(a) shows an input power sweep for the amplifier biased at 4.1 V and 10 mA. The output spectrum for a two-tone test when the tones are offset by 200 kHz and the input power is +11 dBm (optimum PAE) is shown in Figure 3.9(b). The 200 kHz bandwidth is chosen as an example since it corresponds to the bandwidth of an EDGE communication signal. Class-E PAs are highly nonlinear, this can be seen in the high upper and lower IMD3 levels of -19.5 dBc and -17.8 dBc, respectively. The PAE for the two-tone test with the same total input power dropped to 45% and the output power dropped to +17.5 dBm indicating a gain reduction.

To understand this degradation, load-pull measurements were taken for a two-tone test with the same 200 kHz offset. Figure 3.9(c) shows P_{OUT} (solid line)



(a) (b)

(c)

Figure 3.9: (a) Single tone power sweep for class-E PA at 10 GHz, (b) two-tone output spectrum for 200 kHz offset between tones (carrier frequency is 10 GHz), and (c) MESFET P_{OUT} and worst IMD3 load-pull contours. The Class-E impedance is indicated with an '×'; for this impedance PAE is 45% with +17.5 dBm of P_{OUT}. The optimumal PAE of 48% is obtained for $22 + j38\,\Omega$, 'o' with +17.5 dBm of P_{OUT}. Worst IMD3 and maximum P_{OUT} contours coincide.

and worst IMD3 contours (dashed-line) for the MESFET with +11dBm of input power. It is interesting to observe that there is an overlap between maximum output power and worst IMDs. The P_{OUT} and PAE for the class-E impedance are +17.5 dBm and 45% respectively. Optimum PAE (48%) impedance shifted to $22 + j38\,\Omega$ (indicated with a 'o') with same P_{OUT}.

3.4.2 Class-E Amplifier in a Polar Transmitter

Digital polar modulation was implemented using a Xilinx Virtex II FPGA to provide baseband and control signals. Digital-to-Analog Converters (DAC) are used to control a phase shifter responsible for modulating the RF carrier and also to send control signals to the linear portion of the envelope amplifier. The switching converter is also directly controlled by the FPGA. Time alignment of these three components is critical in achieving PA linearity.

The output power level of the envelope amplifier is greater than that of the RFPA, making it a significant factor in system efficiency. An efficient wideband envelope amplifier is realized by taking advantage of the high efficiency of a low-switching frequency converter and the broad bandwidth of a linear amplifier. The envelope command is filtered into high and low frequency components which are sent to the linear amplifier and switching converter respectively. This technique, referred to as band separation, has the capability to improve efficiency for various input signal types [14].

In a polar transmitter, the amplifier input power is held constant and output power variations are achieved by varying the supply voltage. As previously mentioned, in class-E the output voltage is nearly proportional to the supply voltage. Figure 3.10(a) shows how the amplifier parameters (P_{OUT}, Gain, η_{D}, and PAE) change as a function of supply voltage. Since, the RF input power is held constant throughout this test, it leads to negative gain and PAE, and drain efficiency higher

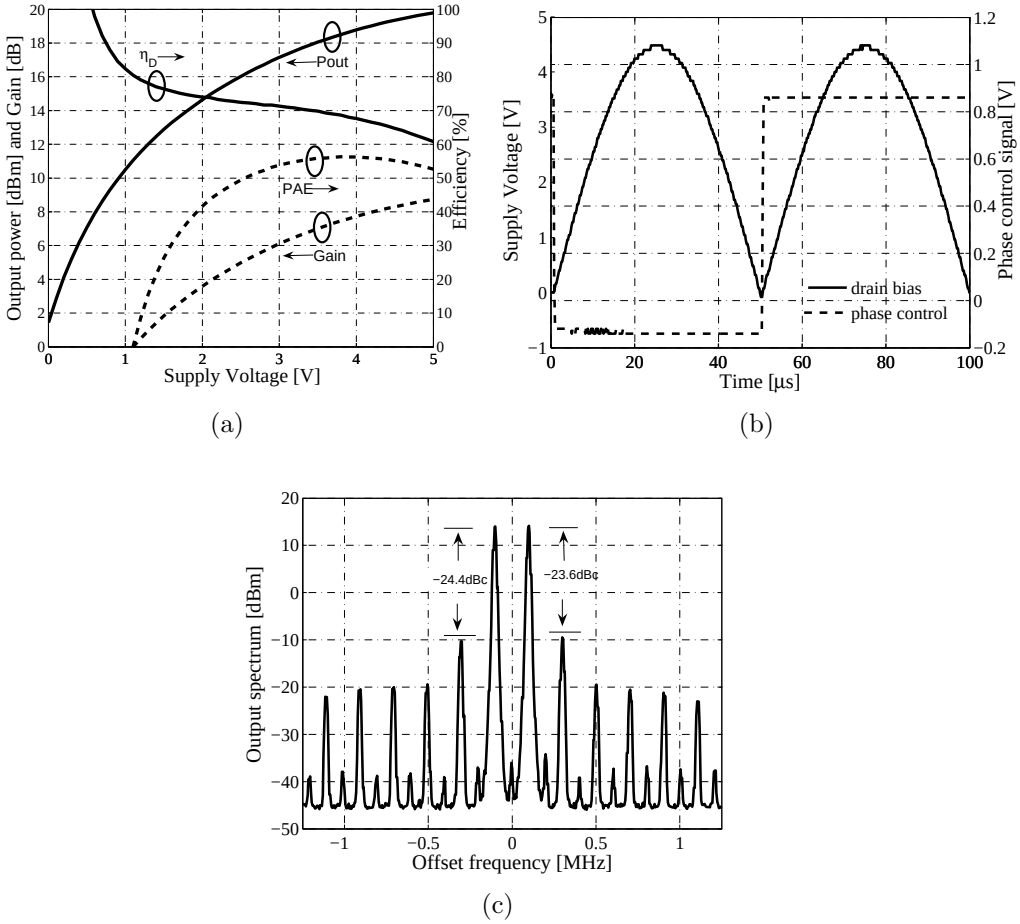


Figure 3.10: (a) Supply sweep for Class-E PA operated at 10-GHz, (b) envelope and phase control time domain signals for polar two-tone test, and (c) polar two-tone output frequency spectrum for 200 kHz offset between tones for a carrier frequency of 10 GHz.

than unity at low bias voltage. A maximal PAE of 56% is obtained for a supply voltage of 3.8 V. The corresponding η_{D} and P_{OUT} are 68.5% and +18.5 dBm respectively. The gain under these conditions is 7.46 dB. As bias voltage varies from 0 V to 5 V output power varies from +1.4 dBm to +18.5 dBm.

Polar system linearity measurement requires the two-tone signal to be split into amplitude and phase components, and fed to the envelope amplifier and phase modulator. Figure 3.10(b) shows the time domain envelope and phase control signals. For a polar two-tone test the envelope corresponds to a rectified

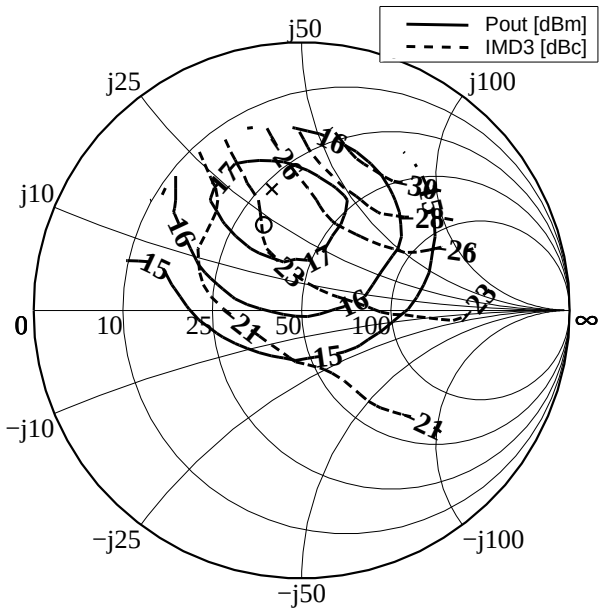


Figure 3.11: MESFET P_{OUT} and worst IMD3 polar load-pull contours. The class-E impedance is indicated with an '×', for this impedance, the η_{D} of the entire polar transmitter is 29.5% with P_{OUT} of +17.5 dBm. The optimal η_{D} of 30.5% is obtained for $31.3 + j22.7\,\Omega$, 'o' with +17.1 dBm of P_{OUT}. Worst IMD3 and maximum P_{OUT} contours do not coincide in this case.

sinewave and the phase control signal is a squarewave. The output spectrum for a polar two-tone test with tone offset of 200 kHz is shown in Figure 3.10(c). Upper and lower IMD measurements were -24.4 dBc and -23.6 dBc, significantly improved over the standard two-tone conditions class-E PA.

A load-pull was performed under polar two-tone excitation. P_{OUT} and worst IMD3 contours are shown in Fig. 3.11. Linearity improvements observed in the output frequency spectrum of Figure 3.10(c) are consistent with IMD measurements. There is a dramatic difference in IMD3 impedance as compared to the PA tested outside of the polar transmitter under standard two-tone conditions from Figure 3.9(b). In this case, the optimum IMD region does not coincide with maximum P_{OUT}. Therefore under polar modulation a different amplifier matching circuit should be designed for optimal linearity.

The P_{OUT} and η_{D} for the entire polar transmitter are +17.5 dBm and 29.5%

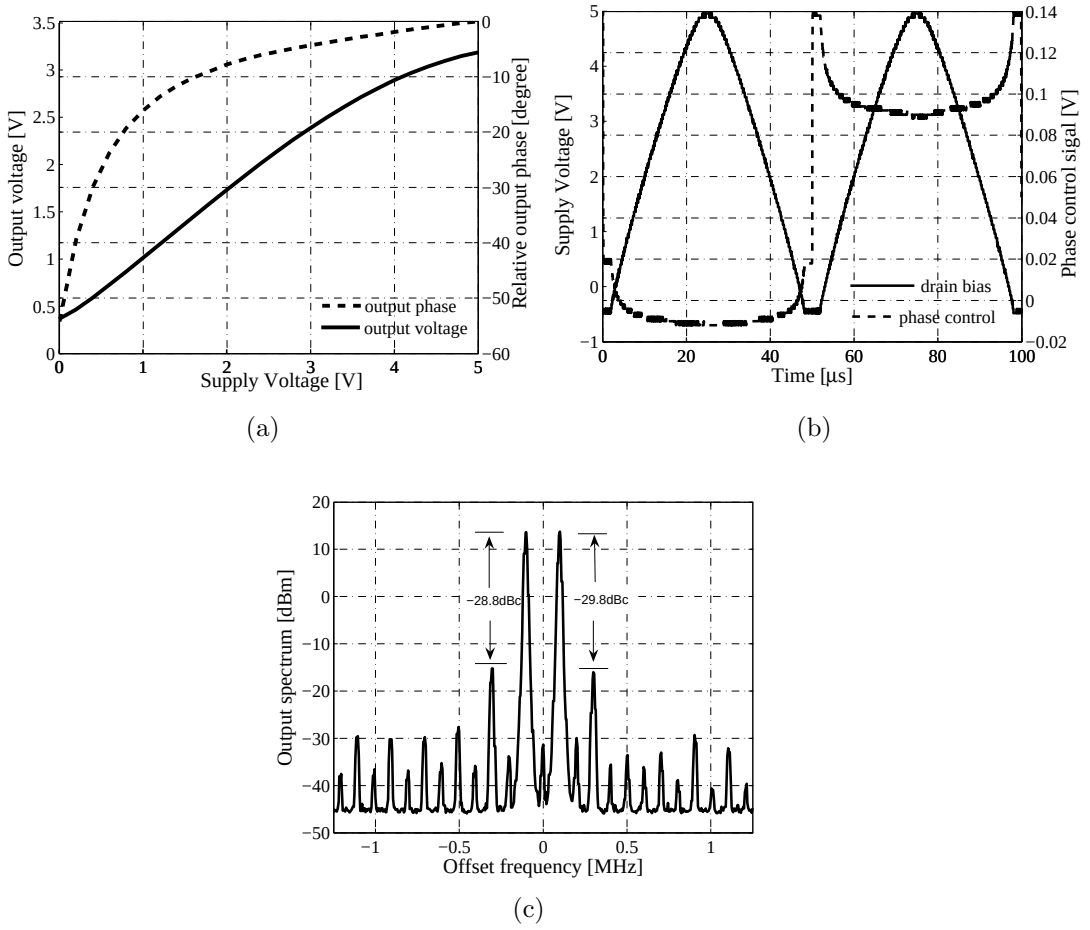


Figure 3.12: (a) Measured static AM-to-AM and AM-to-PM distortion for Class-E PA, (b) predistorted envelope and phase control time domain signals for polar two-tone test, and (c) polar two-tone output frequency spectrum with predistortion for 200 kHz offset between tones for a carrier frequency of 10 GHz [12].

respectively. Significant reduction in η_{D} was suffer because the spectral content of the two-tone envelope. The 200 kHz tones are too high in frequency for the high-efficiency DC-DC switching converter to track, limiting its contribution to only the DC component. Therefore, significant portion of the total envelope power is generated by the linear amplifier. Additional discussion is given in subsection 3.4.4. The maximal η_{D} of the entire polar loop is 30.5% with P_{OUT} of +17.1 dBm. The real and imaginary parts of the best-efficiency load impedance of $31.2+j22.7\Omega$ differ by around 30% from the single-tone load pull value.

3.4.3 Distortion and Predistortion

Figure 3.12(a) shows measured AM-to-AM and AM-to-PM distortion for polar class-E PA. The AM-to-AM distortion describes how the output voltage to a 50 Ω load changes as the supply voltage is varied. The static measurements show that there is significant phase distortion for voltages below 1 V. Other significant non-idealities are the feedthrough and the roll-off at high voltages.

Baseband predistortion was used to compensate for some of the polar system nonlinearities by distorting amplitude and phase information in a manner complimentary to the static AM-to-AM and AM-to-PM characteristics. Baseband distortion was accomplished using a lookup table (LUT) implemented in the FPGA. Figure 3.12(b) shows the predistorted baseband amplitude and phase control signals.

Figure 3.12(c) shows the obtained output spectrum for the predistorted polar two-tone test with 200 kHz spacing between tones. With predistortion the lower and upper IMD3 levels are reduced to -28.8 dBc and -29.8 dBc, for a 4.4 dB and 6.2 dB improvement, respectively. Table 3.1 shows the results for a two-tone test with tone spacing of 20 kHz, 200 kHz, 625 kHz and 1MHz offset between tones. It is interesting the dramatic improvement in two tone performance for 20 kHz case, reducing lower and upper IMD3 levels to -33.2 dBc and -32.9 dBc respectively. However, as the separation between tones increases effectiveness of the predistortion is degraded, suggesting other types of non-linearities are taking

Table 3.1: IMD Level for Polar Two-Tone Test with and without Predistortion

Δf kHz	IMD3_L dBc	IMD3_U dBc	IMD3_{Lpred} dBc	IMD3_{Upred} dBc
20	-22.5	-22.4	-33.2	-32.9
200	-24.4	-23.6	-28.8	-29.8
625	-24.2	-25.4	-27.1	-25.8
1000	-22.2	-25.5	-27.6	-23.2

place, such as memory effects. A more complex dynamic PA model which considers these effects is required to predistort wideband signals. Future work in this area includes the implementation of adaptive predistortion, predistortion of memory effects, and the elimination of feedthrough using RF drive power modulation.

3.4.4 Discussion

A 10-GHz high-efficiency class-E PA was characterized and tested in polar modulation under two-tone conditions. Linearity in polar modulation is significantly improved when compared to the linearity tested under standard two-tone conditions. Load-pull measurements suggest a region where linearity can be farther enhanced. Therefore, under polar modulation a different matching circuit should be designed for optimal linearity and efficiency.

The measured, not optimized, η_{D} for the entire polar class-E transmitter in two-tone test with 200 kHz offset between tones is 29.5%. In [14], it is shown that for an envelope signal with a known amplitude density distribution, an optimum band-separation frequency f_B can be found. Spectrally rich signals such as EDGE can benefit from the band-separation optimization technique because significant amount of power is concentrated at low frequency close to DC. For the case of EDGE signals, optimal band separation (0.88 ratio of envelope sent to the DC-DC converter and 0.12 to the linear amplifier) estimates efficiencies in the order of 72% for the linear-assisted switching converter and 50% for the entire transmitter.

3.5 Conclusion

It is shown in this chapter that polar modulation can be used to linearized high-efficiency power amplifiers. However, the overall transmitter efficiency depends on the efficiency, not only of the RFPA but the efficiency of the envelope tracker

as well. SMPSs can deliver ultra high-efficiencies, are small, light, economic and have the capability to step-up or step-down voltages. However, for these converters losses increase with switching frequency and it is a challenge to design fast high-efficiency SMPSs. With signal envelop bandwidths in the MHz region linear amplifiers can be used to assist SMPSs to achieve larger bandwidths. In envelope signals, most of the power is close to DC and even if linear amplifiers are not efficient, they need to deal with a fraction of the total power maintaining a high overall efficiency.

The measured data on the presented example of a 10-GHz polar transmitter shows that for high-efficiency class-E power amplifiers linearity in polar form is significantly improved when compared to the linearity under standard conditions. Under polar modulation, linearity is not only enhanced, but there is an output matching network were transmitters linearity is optimized.

Simple power managements techniques such as shutting down the PA when it is not needed can significantly improve the transmitter efficiency. However, power can be managed more efficiently by employing flexible or adaptive DC bias approaches such as providing a power supply for the PA that is capable to continually adapt the supplied voltage to achieve required output power variations [14].

The main objective of the work presented in this chapter is to develop a digitally-adaptive amplifier that can operate at high efficiency and linearity for different signal types. A portion of this work was done by Dr. Narisi Wang [35] & Dr. Vahid Yousefzadeh [43]. The specific contributions contained in this thesis are as follows:

- The repeatability of the 10-GHz amplifier characterization, and load pull measurements with single and two-tone (Cartesian and polar) excitation was verified;

- Proper design of bias circuitry for RFPAs in polar transmitters was investigated.

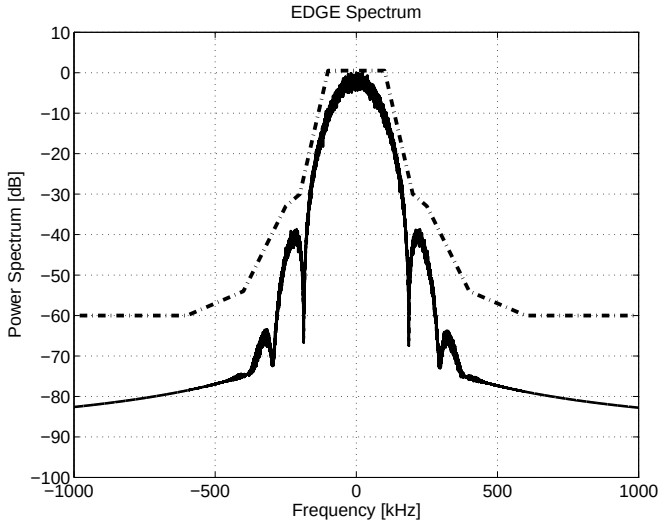
Chapter 4

A High-Efficiency Linear Polar Transmitter for EDGE

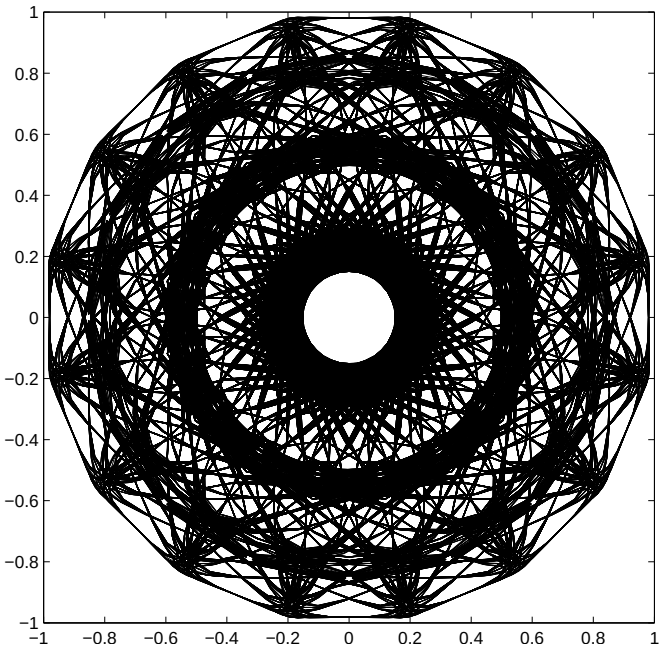
In the previous chapter, it was shown that high-efficiency power amplifiers can be linearized to some degree with the use of dynamic biasing techniques such as polar modulation. This chapter discusses how dynamic bias can be applied to the design of a high-efficiency linear polar transmitter for EDGE modulated signals [38] used in portable radios. Efficiency is especially relevant in portable equipment handsets that depend on battery power.

4.1 EDGE Modulation Scheme

EDGE stands for *E*nhanced *D*ata rates for the *G*SM *E*volution. It is considered to be a 2.5 G or 2.5 Generation modulation scheme and it is the most important transition from 2 G to 3 G for the GSM (*G*lobal *S*ystem for *M*obile communications) standard. Changing the modulation scheme from GMSK (GSM) to 8-PSK improves data rates from 270.833 kbps to 384 kbps over the same 200 kHz spectral bandwidth at one of the 3 career frequencies (900 MHz, 1800 MHz, and 1900 MHz). The EDGE spectrum is shown in Figure 4.1(a). The dashed-line corresponds to

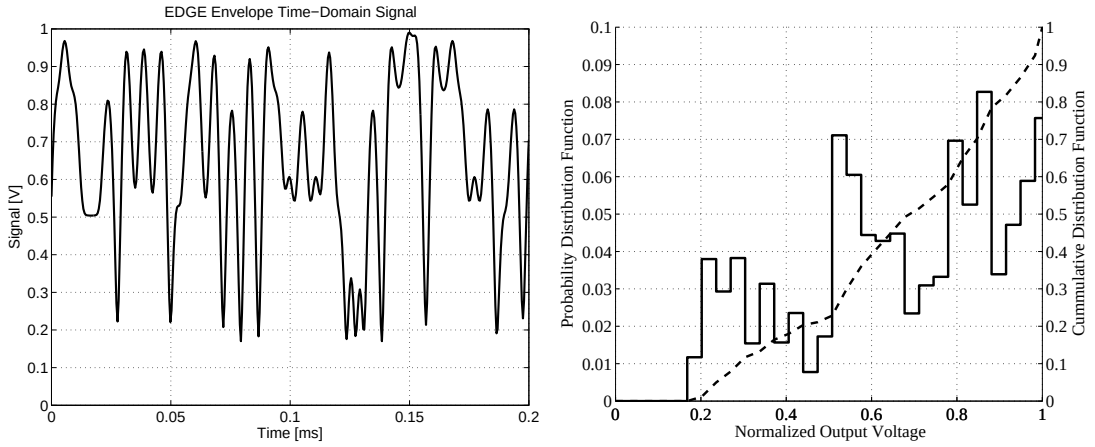


(a)



(b)

Figure 4.1: (a) EDGE frequency spectrum (solid-line) with the EDGE spectral mask (dashed-line). (b) IQ constellation of the EDGE modulation scheme; 8-PSK with $3\pi/8$ phase rotations and filtering. The phase rotations prevent the signal from passing through the origin.



(a) (b)

Figure 4.2: (a) 0.2 ms long sample of the normalized EDGE envelope. The envelope signal varies with time, but it does not have zero values. (b) Probability distribution function (solid-line) and cumulative distribution function (dashed-line) for the EDGE envelope.

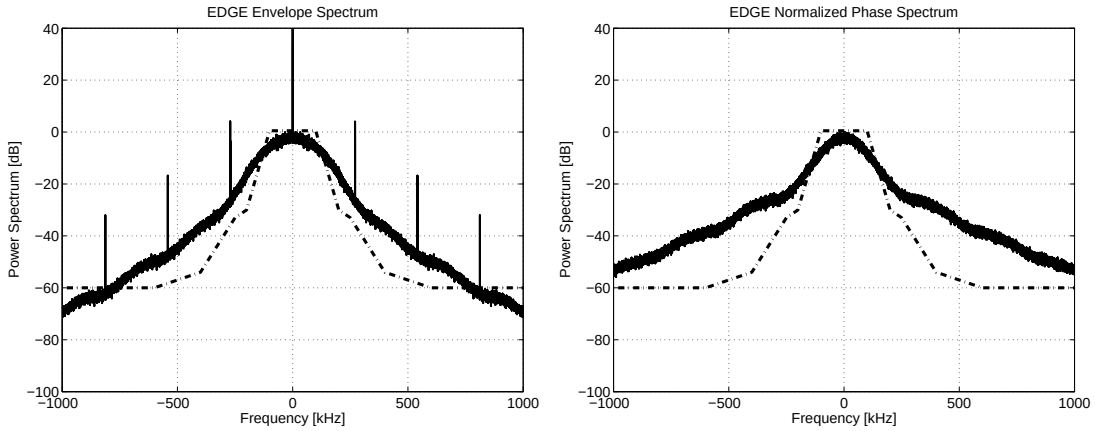
the EDGE spectral mask. It is desired for the EDGE signal to remain within the spectral mask limits to avoid adjacent channel interference. Distortions and unbalances throughout the system are usually displayed as spectral regrowth that commonly make the EDGE signal fall outside the spectral mask limits.

The EDGE constellation is shown in Figure 4.1(b). The $3\pi/8$ phase rotations prevent the signal from cross through the origin. Allowing envelope variations in the EDGE modulation scheme achieves higher data rates within the same GSM bandwidth. Figure 4.2(a) shows a normalized 0.2 ms long signal envelope sequence. The sequence does not cross through the origin, but varies with time. These envelope variations corresponds to a peak-to-average ratio (PAR) of 3.2 dB and they introduce linearity requirements. Figure 4.2(b) shows the calculated EDGE envelope statistics (probability distribution function (PDF) and cumulative distribution function (CDF). From the PDF the mean normalized value of the signal envelope can be calculated to be 0.65. The signal statistics can be used to optimize transmitter performance in terms of power conversion efficiency.

4.2 Polar EDGE

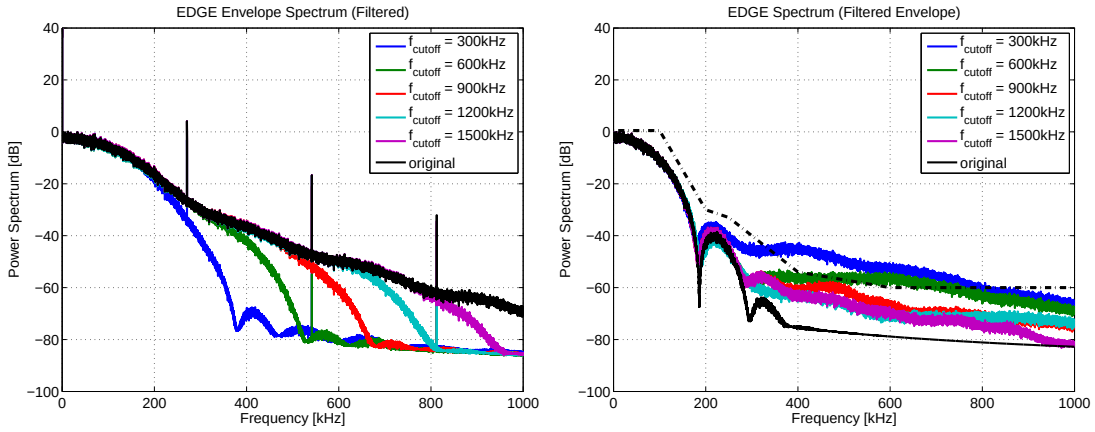
There are several characteristics that make EDGE suitable for polar modulation. For example, the $3\pi/8$ phase rotations prevent the signal envelope from passing through the origin. Also, its 3.2 dB PAR is low compared to 10 dB PA in WCDMA signals. Due to these reasons there has been a lot of effort into developing polar transmitters for EDGE. Companies such as Skyworks, TriQuint, Analog Devices, and Anadigics are starting to release their versions of EDGE polar transmitters giving higher emphasis towards linearity than efficiency [50] - [53]. In [50] is quoted the best number for overall transmitter efficiency in the order of 35% with +27 dBm of output power. This efficiency number is better than the one obtained with a linear amplifier which is in the order of 22% for the same output power level. Significant work has been done by the University of California, San Diego with best numbers for overall transmitter efficiency in the order of 43% with P_{OUT} = +20 dBm [54] - [56]. In these systems the envelope tracker is implemented with a linear-assisted switch-mode power supply.

As described in the previous chapter, in polar transmitters the complex baseband signal is separated into two components; the envelope and a normalized phase modulated signal. Figure 4.3 shows the baseband spectrum of these two components corresponding to EDGE modulation. It is important to notice the increase in spectral bandwidth of the amplitude and phase components compared to the original EDGE spectrum, this implies that the circuits in these paths need to support a bandwidth several times larger than the original signal. In the implemented system, the envelope tracker is implemented with solely a SMPS with a switching frequency of 4.33 MHz and it is followed with a 1.3 MHz Bessel lowpass filter. Details of the tracker are discussed in Section 4.3. The RFPA is a non-linear high-efficiency transmission line hybrid class-E PA with details in Section 4.4.



(a) (b)

Figure 4.3: (a) Envelope and (b) phase baseband spectra of an EDGE modulated signal compared to the total signal spectral mask (dashed-line). In polar transmitters the complex signal is divided into an envelope signal, and a normalized phase modulated signal, which are fed through the bias and input, respectively. It is important to consider the separate spectra of the envelope and phase when designing the polar transmitter circuits.



(a) (b)

Figure 4.4: (a) Envelope signal is lowpass filtered with different cutoff frequencies. Band-limiting the envelope spectrum results in spectral regrowth (b). From here we conclude that the cutoff frequency of the filter used in the envelope path should be larger 1200 kHz.

4.2.1 Bandwidth Limited Envelope

The design of efficient envelope trackers with large bandwidths is a challenge. Figure 4.4 shows the calculated effects of limiting the envelope bandwidth (Figure 4.4(a)) in the combined EDGE spectrum (Figure 4.4(b)). The envelope spectrum is lowpass filtered with cutoff frequencies of 300 kHz, 600 kHz, 900 kHz, 1200 kHz, and 1500 kHz. Figure 4.4(a) shows the envelope spectra for each of these cases compared to the original spectrum. As can be seen in Figure 4.4(b), the main effect of limiting the envelope spectral bandwidth is spectral regrowth in the combined signal. This same figure shows that to meet the spectral mask, the cutoff frequency of the filter should be higher than 1200 kHz. This figure illustrates the consequence of band limiting the envelope signal, however it is important to point out that the spectral response depends not only on the filter cutoff frequency, but also on additional parameters such as the order and the type of filter used.

4.2.2 EDGE Polar Transmitter

Figure 4.5 shows a block diagram of the EDGE polar transmitter. The transmitter has 3 baseband input signals and the RF signal that determines the carrier frequency. The 3 baseband input signals correspond to the envelope of the EDGE sequence $IQ_A(t)$, and the normalized $\hat{I}(t)$ and $\hat{Q}(t)$ signals which are quadrature phase parameters. Linearity is achieved when the RFPA performs the function of multiplying the amplitude and normalized phase signal in time domain, thus reconstructing the original signal. Time alignment between envelope and phase signals is therefore crucial for output signal fidelity.

To make the transmitter efficient, a high-efficiency envelope tracker and a high-efficiency RFPA are needed. As was discussed in the previous chapter, SMPS are suitable for implementing high-efficiency envelope trackers, while Class-E ampli-

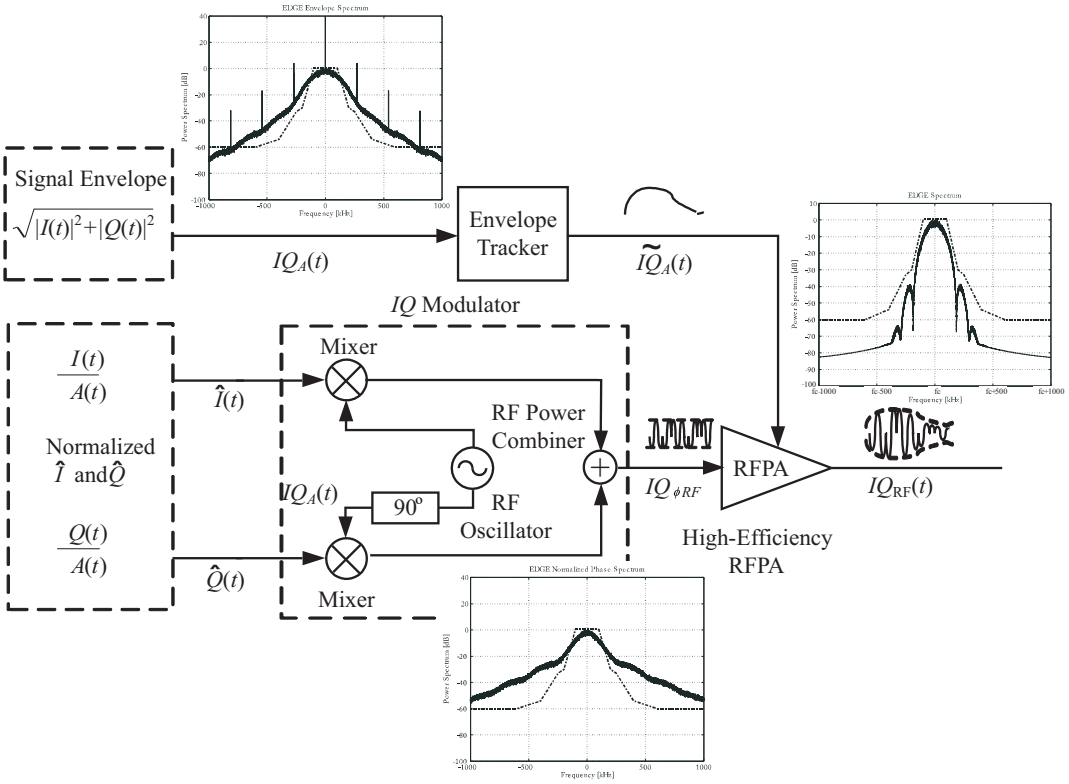


Figure 4.5: Block diagram of the EDGE polar transmitter. Three baseband signals are generated; the envelope $IQ_A(t)$, normalized $\hat{I}(t)$ and normalized $\hat{Q}(t)$. The RF output is the reconstructed signal $IQ_{\mathrm{RF}}(t)$.

fiers are ideal for the RFPA because the output voltage across a constant load is theoretically linearly proportional to the supply voltage. The next section discusses the designed envelope tracker and the RFPA.

4.3 High-Efficiency Envelope Tracker

The envelope tracker used in this work is implemented with a synchronous Buck SMPS (Figure 4.6) and the envelope variations are achieved with pulse width modulation. Deadtime (time when both transistors in Figure 4.6 are ON) control of the synchronous switches in SMPS is essential to enhance the tracker efficiency by eliminating the short circuit current and it is implemented with a digital counter-

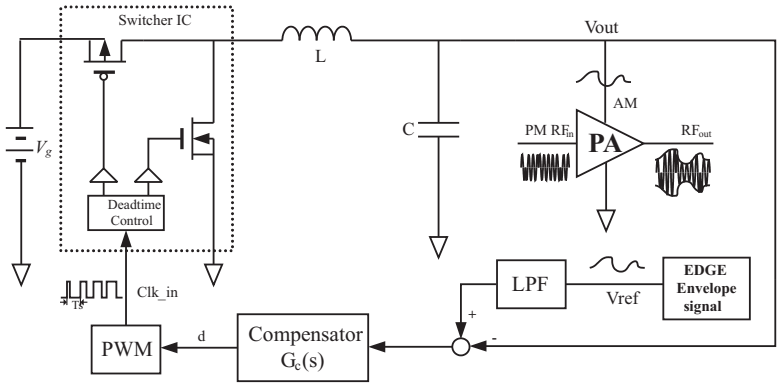


Figure 4.6: Schematic of the closed-loop envelope tracker. The tracker is implemented with a synchronous Buck switching converter. Envelope variations are achieved with pulse width modulation and deadtime control is used to enhance the tracker efficiency [16].

based adaptive scheme. Control is also required to produce a well regulated output voltage in the presence of variations in the input voltage, the load and/or element tolerances. The feedback loop around the power stage also achieves disturbance rejection and sensitivity reduction. The feedback loop also improves the tracking performance when compared to open loop operation. To minimize switching harmonics, the envelope tracker is followed by a 4^{th} order low pass Bessel filter with a cutoff frequency of 1300 kHz that keeps the 2^{nd} switching harmonic below -65 dBc, with a constant group delay of 259 ns [16]. This bandwidth is larger than the 1200 kHz found in the previous section.

Two factors were considered when choosing the switching frequency: signal bandwidth and switcher efficiency. The bandwidth of EDGE signals is 200 kHz, but the spectral requirements increase when the signal is converted to polar form as discussed in the previous section. The switching frequency was chosen to be 16 times higher than the EDGE standard transmission rate of 270.833 kHz. This corresponds to a switching frequency of 4.33 MHz. The tracker supply voltage is 3.6 V, which corresponds to the nominal voltage of a single-cell Li-Ion battery. The maximum output voltage of the tracker is 3.3 V. The switcher measured efficiency

is 79% [45]. For additional information about the switch-mode envelope tracker, the reader is referred to [16], [45].

In section 4.6, the performance of the transmitter with the switching supply from Figure 4.6 is compared to that with a linear amplifier envelope tracker such as the one presented in [17]. Although the power efficiency of a linear amplifier is not suitable, it can provide higher bandwidths and better dynamics than other analogous tracking systems. The linear amplifier is followed by a 4^{th} order lowpass Bessel filter with a cutoff frequency of 2.5 MHz and constant group delay of 140 ns.

4.4 High-Efficiency RFPAs

The transmitter efficiency depends not only on the efficiency of the envelope tracker, but on the efficiency of the RFPA as well. The steps to follow for the design of a high-efficiency RF power amplifier at a specified operating frequency and output power are:

(1) Choose mode of operation, suitable for the operating frequency. As was discussed in Chapter 2, there are several high-efficiency modes of operation, among them Class-E. The main advantage of the Class-E mode is that the output RF voltage to a constant load is linearly proportional to the supply,

$$V_{\text{OUT}} = \pm \left(26 \cdot f_S \cdot C_{\text{OUT}} \sqrt{R_{\text{E}} \cdot R_{\text{L}}}\right) \cdot V_{\text{DS}} \tag{4.1}$$

were R_{E} is the real part of the optimal impedance presented to the device for class-E switched mode operation, f_S is the operating frequency which is also the switching frequency, and C_{OUT} is the output capacitance of the device.

(2) Select the transistor. The main parameters of interest for class-E operation are the device internal output capacitance, the break down voltage and the

maximum output power capability of the device.

(3) In class-E the transistor is biased at cutoff and the RF input signal turns ON and OFF the device. It is important to determine the voltage range in which the transistor is going to operate. In class-E mode the voltage across the device might be higher than $3.56 \times V_{\mathrm{DS}}$. This mean that the maximum supply voltage needs to be limited to a maximum of $V_{\mathrm{DSS}}/3.56$, where V_{DSS} is the breakdown voltage of the device. Reducing the maximum supply voltage will limit the maximum RF output power of the device.

(4) Design input and output matching networks. For Class-E operation the harmonics should be terminated with a high impedance, in the transmission line version this is accomplished with stubs. The fundamental impedance should be terminated in a particular impedance that ensures soft switching. This impedance can be theoretically from the transistor output capacitance and the operating frequency [23],

$$Z_{\mathrm{E}} = \frac{0.28}{2\pi f_S C_{\mathrm{OUT}}} e^{j49^\circ} \tag{4.2}$$

The input needs to be matched to maximize gain, otherwise the η_{S} will be much larger than PAE.

4.4.1 Transistor Selection

Class-E is a switched mode of operation. Switching at RF frequencies is approximated by choosing a device with a low output capacitance relative to the operating frequency and a high f_T. The EDGE standard has 3 operating bands; 900 MHz, 1800 MHz, and 1900 MHz. For the 900 MHz band mobile transmitters operate around 880 MHz with output power of approximately +30 dBm. The transistor selected is the TGF-4240 from TriQuint. It is 2.4-mm HFET with and output

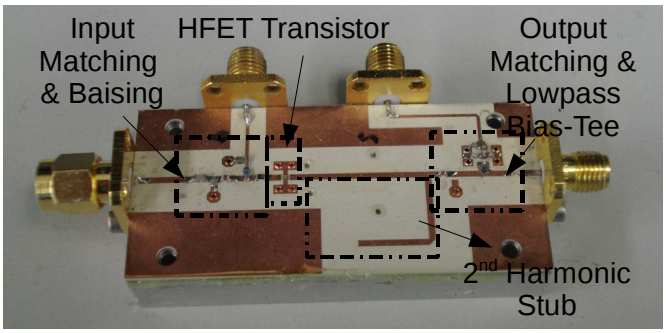


Figure 4.7: Photograph of the transmission line hybrid 880-MHz class-E power amplifier with integrated bias lines and DC blocking capacitors which also serve for impedance matching. A 10-Ω chip resistor in series with the gate terminal ensures stability of the PA.

capacitance of approximately 1 pF. The transistor is intended for operation at 8 GHz with over +30 dBm of output power and 10 dB of gain when operated from a 8 V supply [57]. Thus, at 880-MHz, it should be able to operate in Class-E.

4.4.2 RF Amplifier Design

This section details the design of the high-efficiency class-E PA for the polar EDGE transmitter, Figure 4.7. The design method combines transmission lines and lumped components for the implementation of the matching networks in order to keep loss low, but also reduce size. Transmission lines are used at the output to present a high impedance to the transistor second harmonic. The fundamental-frequency input and output matching circuits are implemented with lumped inductors and capacitors. The amplifier is build on a Rogers TMM6 0.635-mm thick substrate ($\epsilon_r = 6$). A 10-Ω series resistor is included in the gate of the transistor for stabilizing the PA at the operating frequency.

Using Equation 4.2 where the output capacitance for this particular device is estimated to be 1 pF based on measured small-signal S-parameters. Because the exact large-signal value of the output capacitance is not known, a source and load-pull measurement is performed around the initial estimate of Z_{E} to determine

Table 4.1: Load-pull for HFET Transistor at 880-MHz.

C_{OUT} (pF)	Z_E (Ω)	η_D (%)	PAE (%)	Gain (dB)	P_{OUT} (dBm)
0.5	66 + j77	49	41	8	+18
0.6	55 + j64	58	48	8.2	+18.2
0.7	47 + j55	55	47	8.7	+18.7
0.8	42 + j48	67	58	9.7	+19.7
0.9	37 + j43	62	55	9.6	+19.6
1.0	33 + j38	62	56	9.8	+19.8
1.1	30 + j35	62	56	10	+20

the optimum impedance. The only unknown in Equation 4.2 is C_{OUT}. Because there is uncertainty in the exact value of the output capacitance a load-pull was performed presenting to the device the calculated Class-E impedance from C_{OUT} in the range between 0.5 pF and 1.1 pF as shown in Table 4.1. Measurements are taken for V_{GS} = -2 V, V_{DS} = 3.5 V and +10 dBm of input power. A tradeoff analysis needs to be made in terms of gain, output power and efficiency for choosing the desired impedances. Since the main goal of the project is to improve linearity and efficiency, the output impedance of $42 + j48\,\Omega$ is chosen, corresponding to an output capacitance of 0.8 pF. The resulting PAE is 58% with a drain efficiency of 67%, a gain of 9.7 dB and an output power of +19.7 dBm.

The amplifier final design is biased at V_{DS} = 2.16 V taking into account the EDGE envelope mean of 0.65 and the maximum supply voltage from the SMPS of 3.3 V (0.65×3.3 V) and V_{GS} = -1.7 V, for I_{DS} = 72 mA. It was found that varying V_{GS} from -2 V to -1.7 V increased the gain and the output power with no degradation in efficiency. The input is matched to $15 + j35\Omega$ for an input return loss of -10 dB. Figure 4.8(a) shows the measured power sweep, which resulted in a choice for the input power of +7.6 dBm. If the transistor is compressed further, the drain efficiency will continue to increase but at the expense of gain and PAE. For this particular bias point, with +7.6 dBm of input power, the output power

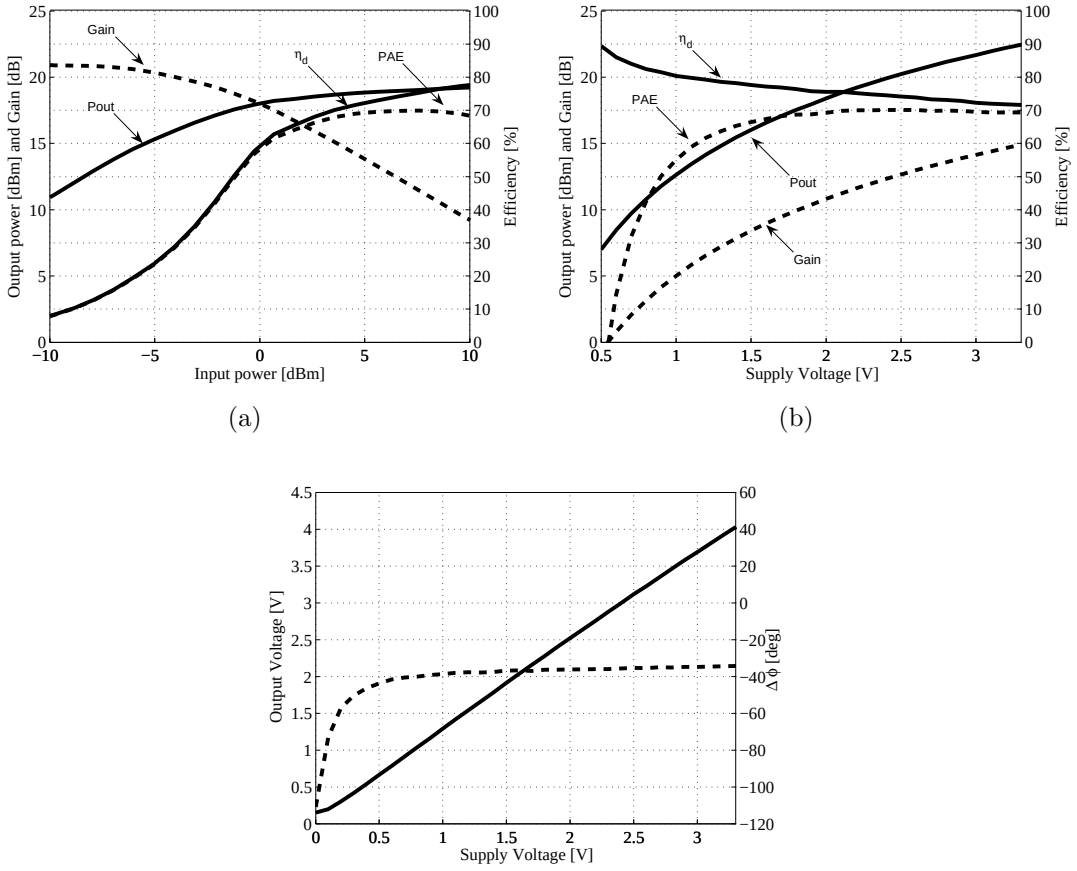


Figure 4.8: Measurements for EDGE 880-MHz class-E PA with $V_{GS} = -1.7\,\text{V}$. (a) Power sweep for $V_{DS} = 2.16\,\text{V}$, the maximal PAE is 70% with a drain efficiency of 75%, gain of 11.46 dB and output power of +19 dBm for input power of +7.6dBm. (b) Measured output power, gain, drain efficiency and PAE for supply sweep with input power of +7.6 dBm. (c) Measured AM-to-AM (solid line) and AM-to-PM conversion (dashed line).

is +19 dBm with a gain of 11.5 dB, drain efficiency of 75% and PAE of 70%.

Careful attention needs to be given to drain line design to avoid distortion and linear memory effects [58]. The drain line lowpass performance has to be designed to allow for supply modulation at the signal envelope bandwidth. The measured performance of the PA is shown in Figure 4.8: at 880 MHz, the PA gives +19 dBm output power at 3 V supply voltage with 70% power added efficiency and 11.5 dB gain.

4.4.3 RFPA Characterization

Figure 4.8(b) shows the results for the measured output power, gain and efficiencies for the class-E PA when V_{DS} is swept from 0.5 V to 3.3 V with V_{GS} = -1.7V and an input power of +7.6dBm. As can be observed from the figure, η_{D} is high throughout the entire supply voltage range, while the PAE is above 50% during a substantial part of the sweep, ensuring high-efficiency performance for this particular applications. Considering the EDGE statistics the mean values $\overline{\eta_{\mathrm{D}}}$, $\overline{\mathrm{PAE}}$ and $\overline{P_{\mathrm{OUT}}}$ are 76%, 65% and +19 dBm, respectively.

Figure 4.8(c) shows the AM-to-AM (solid line) and the AM-to-PM (dashed line) conversion. The AM-to-AM measurements show the output voltage variations produced to a 50-Ω load by sweeping the supply voltage for fixed input power. For a supply voltage of 0 V the output voltage is non-zero due to feedthrough. A linear relationship is observed in the range of interest (0.5 V to 3.3 V) and can be described by

$$V_{out} = 1.2V_{\mathrm{DS}} + 0.091\mathrm{V}. \tag{4.3}$$

The AM-to-PM conversion curve shows the phase offset produced by the amplifier as the supply is swept. As desired this value is almost constant throughout the range of interest. The measurement shows significant variations in phase for supply voltages below 0.5 V.

A summary of the measured PA properties is as follows:

- When the drain bias is swept from 0.5 V to 3.3 V, the output power varies from +7.01 dBm to +22.45 dBm giving an output power range of 15.44 dB.
- The drain efficiency, PAE and gain for maximal output power at $V_{\mathrm{DS}} = 3.3$ V are 71.6%, 69% and 14.9 dB, respectively.

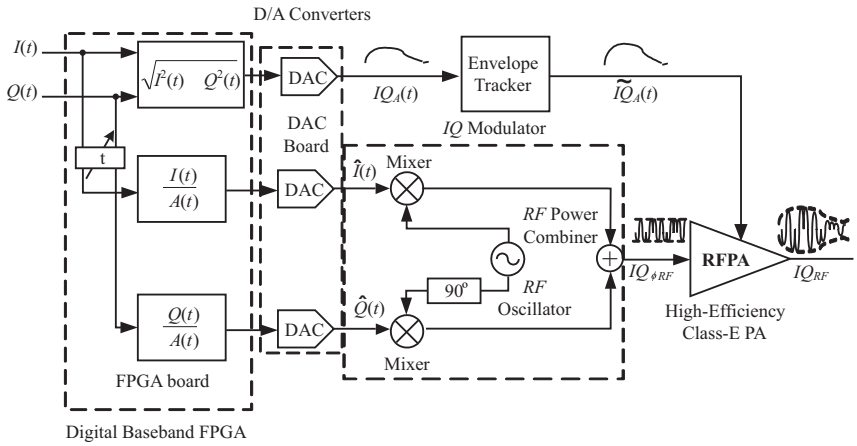


Figure 4.9: Block diagram of a polar transmitter. A random string of symbols is stored in the FPGA board as a look up table and transmitted at 2.17 MHz which corresponds to an over-sampling ratio of 8. The FPGA has three outputs; the amplitude of the complex signal, $IQ_A(t)$ which is the envelope tracker reference and normalized $\hat{I}(t)$ and $\hat{Q}(t)$ that are inputs to an are the input to an IQ modulator; the output is a constant amplitude phase modulated RF signal. Digital-to-analog converters are used at each output.Time alignment between amplitude and modulated phase path is crucial since both values determine each symbol.

- The maximal PAE is 70.2% obtained for a drain voltage of 2.6 V. At this bias point, the output power is +20.6 dBm, with a gain of 13 dB and a η_D of 74%.

- At a drain voltage of 0 V the output power is -4 dBm due to feed-through.

- Due to feed-through, drain efficiencies higher than 100% can be achieved since the input power is not considered in drain efficiency calculations.

- At high drain voltages, the drain efficiency and PAE exceed 70%. Signals with statistics that are weighted towards higher output powers are the ones that benefit from this technique.

4.5 EDGE Polar Transmitter Implementation

The diagram shown in Figure 4.9 is implemented with a Xilinx Virtex II FPGA and commercial oscillator, IQ modulator and DACs as shown in Figure 4.10. The oscillator is an Analog Devices ADF4360-7 and the IQ modulator is Texas Instruments TRF3701. For testing purposes an EDGE signal segment consisting of 256 pseudo random symbols is stored as a look up table in the FPGA and streamed out repeatedly. Given the standard EDGE transmission rate of 270.833 kHz and an oversample ratio of 8, the signals are streamed out of the FPGA at the rate of 2.17 MHz. The FPGA and baseband circuits were programmed and design by Dr. Xufeng Jiang.

Time synchronization between envelope and phase signals is crucial to minimize distortion, as discussed in [12]. For time alignment, it was found to be sufficient to compensate for the group delay τ produced by the lowpass Bessel filter. It was also found to be important to compensate for the DC offset introduced by the DACs in the I and Q channels. The implementation shown in Figure 4.10 allows all the required adjustments to be performed digitally.

4.6 System Performance

The system described in section 4.5 was implemented as shown in Figure 4.10. Figure 4.11 shows the measured output spectrum of the polar transmitter, with the switcher (blue) and the linear amplifier (red) as the envelope trackers. Because the linear amplifier bandwidth is larger than the SMPS it shows less spectral regrowth, however, the transmitter with the 79% SMPS also meets the EDGE spectral mask. It is important to emphasis that the high-efficiency RFPA was linearized with dynamic biasing without any pre-distortion. Adding pre-distortion to the system will farther enhance its linearity.

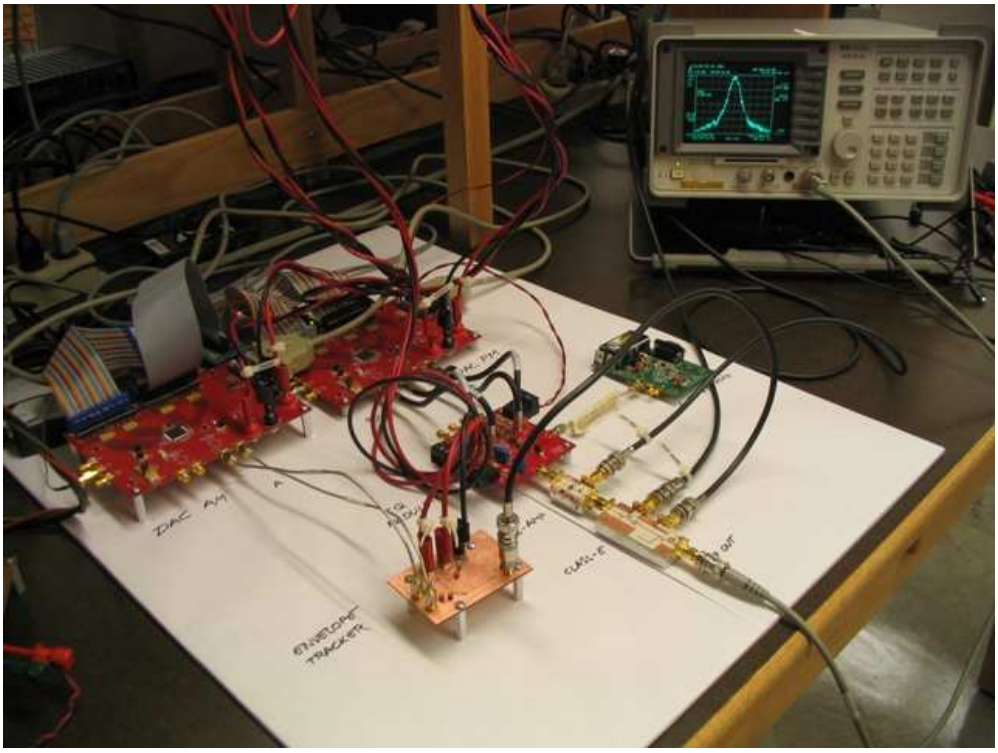


Figure 4.10: Photograph of the implemented setup. Baseband circuit design, selection and FPGA programming was performed by Dr. Xufeng Jiang.

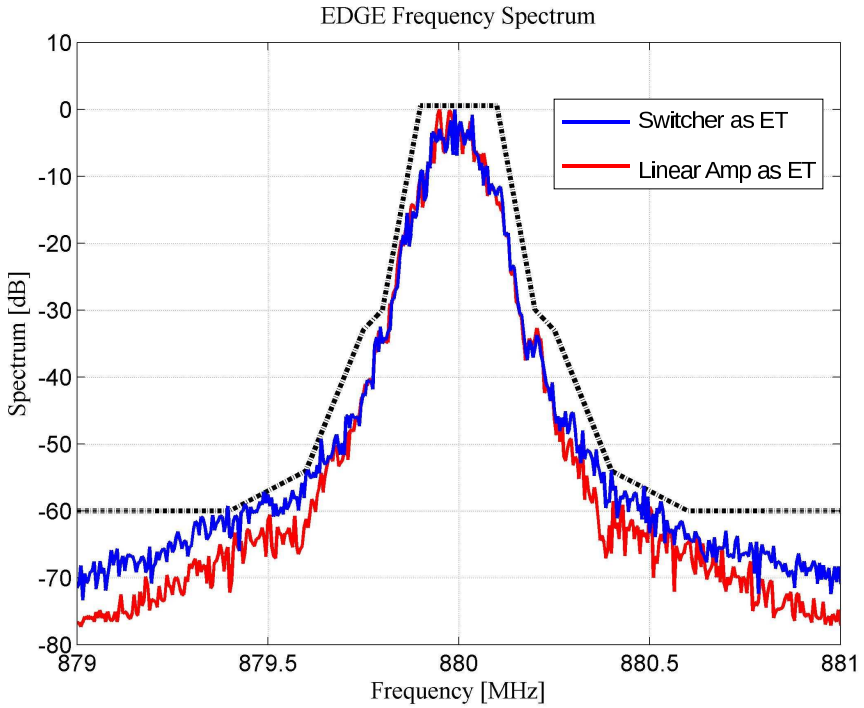


Figure 4.11: Measured output spectrum of the polar transmitter when the envelope tracker is the linear amplifier (red) and fast switching buck converter (blue). The dashed line indicates the EDGE spectral mask requirement.

The total transmitter efficiency taking into account the 79% efficiency SMPS and the 71% RFPA is 56% with an average RF output power of +20 dBm. The RFPA is able to deliver more than +30 dBm of output power at 8 V drain voltage, however it is desired to use a 3.6 V Li-Ion power battery as the DC power source of the system. This power source in combination with a Buck converter limits the maximum PA supply voltage to 3.3 V thus limiting the output power capabilities of the RFPA.

4.7 Summary

In conclusion, it is possible to linearize high-efficiency switched mode RFPAs to meet the EDGE spectral mask using a polar architecture, while maintaining high overall transmitter power consumption efficiency. This work demonstrates a 880-MHz 56% efficient polar transmitter for EDGE with +20 dBm of output power. The envelope tracker is a 79% efficient switch-mode buck converter and the RFPA is a 71% non-linear transmission line Class-E power amplifier. The transmitter meets the EDGE mask with two different envelope trackers, a less efficient linear amplifier with a 2.5 MHz bandwidth and a high-efficiency switch-mode power supply with a 1.3 MHz bandwidth.

The main objective of the work presented in this chapter is to described the details of the EDGE polar transmitter. The specific contributions contained in this thesis are as follows:

- Design and implementation of a transmission line hybrid Class-E power amplifier for the 880-MHz polar transmitter. The maximal PAE is 70% with η_{D} of 75% with $P_{\mathrm{OUT}} = +20\,\mathrm{dBm}$. The maximal P_{OUT} is +22.4 dBm with little degradation in PAE.

- The amplifier is linearized with polar modulation without the need of pre-

distortion and meets the EDGE spectral mask.

- The total transmitter efficiency is 56% with $P_{OUT} = +20\,\text{dBm}$ for EDGE signals. This is the highest efficiency reported for a EDGE polar transmitter to date. The closest work [56] is a parallel effort at the University of California, San Diego with a 44% efficient polar transmitter with the same output power.

Chapter 5

High-Efficiency UHF PA Design based on Load-pull

5.1 Introduction

RF amplifier design consists of biasing and impedance matching. These parameters are selected so that the PA performs a desired function at the desire frequency range, i.e. low-noise, maximum output power, linearity, or efficiency. Linear simulators are great tools for designing linear amplifiers. However, power amplifiers are driven with large signals and particularly in switch-mode operation display strong nonlinear behavior. The devices are driven into saturation and cutoff for a certain portion of the RF cycle and modeling these strong nonlinear effects is a difficult task, even if CAD models and tools are available [20]. Nonlinear device models often fail to accurately represent devices operating in class-E mode where the dynamic load line is close to the I-V axes.

Load-pull techniques can be modified for effective amplifier characterization in this mode of operation as shown in [34]. The load-pull technique consists of empirically presenting calibrated input and output impedances, RF excitation

and biasing conditions to the DUT and recording desired responses such as, input power, output power, gain, and power consumption. As long as the responses of interest can be measured, impedance contours that map the PA performance as a function of these controllable parameters can be created.

As an example, this method is used for designing a high-efficiency power amplifier at 370-MHz with a GaN HEMT on a SiC substrate prototype from RFMD, the RF3932. This transistor can deliver $P_{\mathrm{OUT}} = 60\,\mathrm{W}$ in Class-AB at 2 GHz and it is rated for 48 V operation with 14 dB of gain.

The steps for characterizing and designing a high-efficiency power amplifier are as follows:

(1) Select biasing conditions and characterize the transistor via load-pull;

(2) Design input and output matching networks and perform impedance verification;

(3) Repeat load pull to verify amplifier optimum operation; and

(4) Fine tune input and output matching networks until optimum PA performance is achieved.

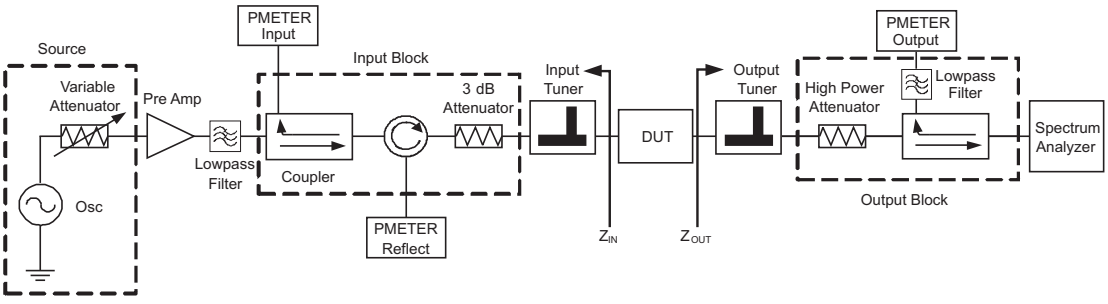


Figure 5.1: Setup for load-pull device characterization. The setup consists of a source, input and output blocks, the device under test (DUT), and impedance tuners.

5.2 Load-pull Setup and Calibration

Figure 5.1 shows a schematic of a load-pull setup. The setup consists of a source, input and output blocks, impedance tuners, and the device under test [59]. Load-pull characterization depends on carefully calibrating the input and output blocks, and the impedance tuners usually with a network analyzer. For device characterization the input and output blocks, as well as the tuners in the setup of Figure 5.1 are modeled with S-parameter matrices. Impedance tuners are calibrated creating look-up tables that map tuner position to S-parameters [59].

In this case, S-parameters do not take into account power dependent variations, such as thermal drift. The circulators/isolators and the attenuators might be sensitive to power or temperature. To reduce uncertainty it is important to use robust components that do not vary with power. A description of each of these elements is given next:

- **Source** - The source determines the operating frequency and the system input power.
- **Pre-Amplifier** - Usually, the source's output power is low compared to input power needed for amplifier testing, i.e. measuring compression. A linear pre-amplifier can be used to increase the available input power. Pre-amplifiers might generate harmonics and these should be lowpass filtered.
- **Input Block** - The input block consists of a coupler, a circulator/isolator and a 3 dB attenuator. The circulator/isolator ensures the coupler is terminated in 50 Ω. Also redirects the input reflected power to a load. A circulator or an isolator is used, depending on whether or not it is desired to measure reflected power. The 3 dB attenuator reduce out-of-band reflections produced by the the circulator/isolator. Out-of-band reflections might present impedances that drive the DUT into unstable regions causing oscillations.

- **Output Block** - The output block consists of a high-power attenuator, a coupler and a lowpass filter. The attenuator reduces P_{OUT} to a suitable level for RF instruments. For example, the maximum power handling of RF power sensors is usually +20 dBm, while the power handling of spectrum analyzers is usually +30 dBm. The attenuator is followed by a coupler to sample the output power. This signal is lowpass filtered to farther reduce harmonic levels. If it is desired to view the output spectral content, it should be through the direct path, because the coupled path is frequency dependent and will affect spectral measurements.

- **Impedance Tuners** - The impedance tuners transform a known impedance, usually a 50 Ω load, into a range of impedances. Some of the tuner important parameters are the maximum reflection coefficient ($|\Gamma_{\mathrm{max}}|$), impedance resolution and insertion loss. Impedance tuners can be manually or electrically controlled mechanical [59]- [61], based on MEMS, semiconductors [68] or active [62]. Active tuners inject a signal in a controllable manner mimicking a load. For additional information on tuners the reader is referred to [59] - [68].

5.2.1 Pre-matching Circuits

Impedance tuners can cover a set of points on a Smith Chart, referenced to an impedance constellation as shown in Figure 5.2(a). The constellation is centered around the tuner characteristic impedance, usually 50 Ω with points equally spaced radially around this value. The tuners are able to present impedances within a range in $|\Gamma|$ (from 0 to $|\Gamma_{\mathrm{max}}|$) with a particular density (number of constant $|\Gamma|$ and Δ phase).

Small impedances are needed to match high-power devices. In this case, pre-

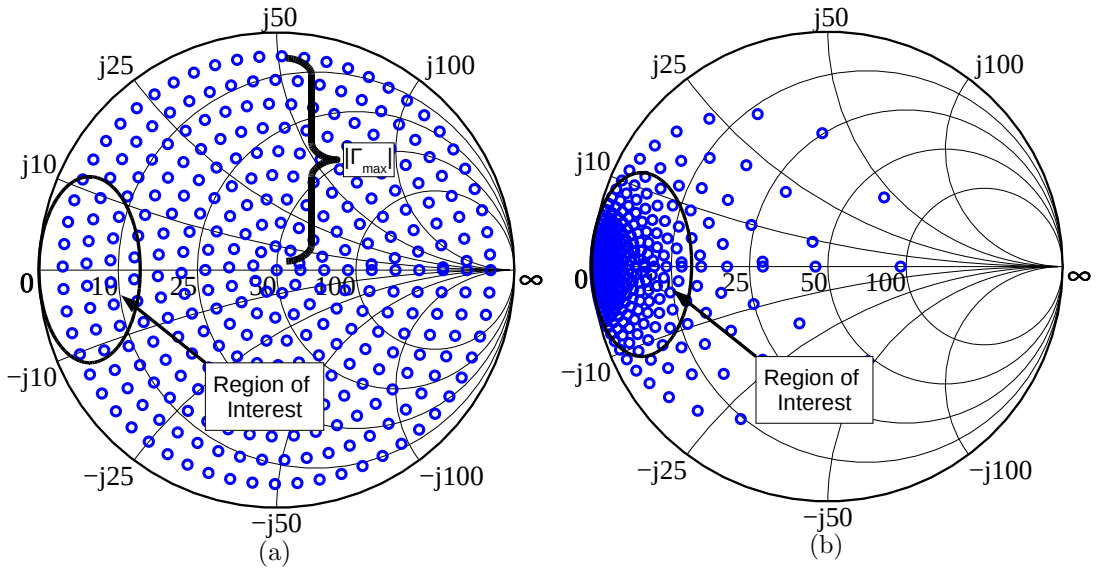
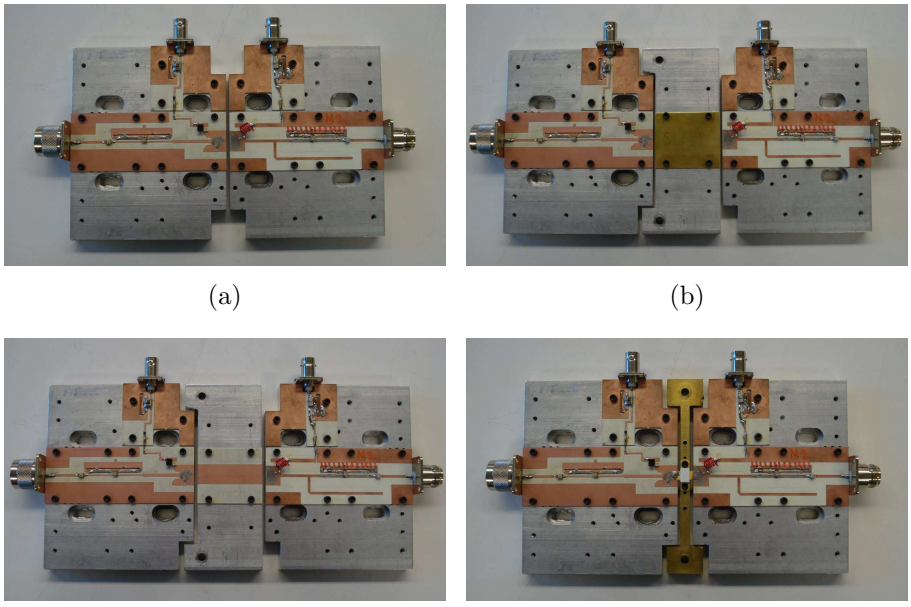


Figure 5.2: Typical constellation achieved by impedance tuners. (a) The points enclose the system characteristic impedance (usually 50 Ω). (b) Small impedances are necessary to match high-power devices. Pre-matching circuits can be used to shift the constellation to the region of interest, in this example 5 Ω.

matching circuits can be used to shift the constellation to a new impedance range as shown in Figure 5.2(b). In this example, the constellation is centered around 5 Ω.

For class-E mode characterization the pre-matching circuit not only re-centralizes the impedance constellation closer to the region of interest, but also terminates harmonics in an open circuit. For ideal Class-E operation, it is necessary to terminate all the transistor harmonics. However, reasonable performance can be achieved by terminating only the 2^{nd} harmonic. Terminating additional harmonics adds complexity and insertion loss for little enhancement in efficiency. Harmonic stubs are resonating structures and it is difficult to present the correct amplitude and phase for more than two harmonics simultaneously. Harmonic stubs also affect the fundamental frequency making multiple harmonic termination circuit design complex.



(a) (b)

(c) (d)

Figure 5.3: TRL fixture for transistor characterization in class-E mode. The input and output blocks transform the load-pull contours to a low impedance suitable for characterization. The output block includes an open stub for terminating the second harmonic with a high impedance. (a) TRL thru connection, (b) TRL reflect connection implemented with a short circuit, and (c) TRL line, and (d) input and output block fixtures with the DUT.

5.2.2 DUT Fixture Calibration

A modular mechanical fixture was designed to allow for pre-match circuit characterization and impedance verification. The fixture is shown in Figure 5.3. S-parameters of the pre-matching circuits are found using a TRL calibration algorithm requiring that the input and output pre-matches be:

- Connected together directly at the DUT plane (Figure 5.3(a));
- Terminated with high reflection (implemented in Figure 5.3(b) with a short circuit); and
- Connected together via a short length of transmission line with a known characteristic impedance (Figure 5.3(c)).

The modular nature of the mechanical fixture allows these configurations to be used easily and repeatably without fabricating additional calibration standards. Copper tape or solder is used to make microstrip connections between blocks. The modular fixture allows the use of passive lumped elements such as inductors and capacitors. Using the same fixture for calibration and testing eliminates element tolerance variations, reducing uncertainties.

5.2.3 Block Deembeding & Impedance Verification

The TRL algorithm returns two S-parameter matrices corresponding to the fixture input ($\mathbf{S}^{\mathrm{A}}$) and output blocks ($\mathbf{S}^{\mathrm{B}}$):

$$\mathbf{S}^{\mathrm{A}} = \begin{bmatrix} s_{11}^{\mathrm{A}} & s_{12}^{\mathrm{A}} \\ s_{21}^{\mathrm{A}} & s_{22}^{\mathrm{A}} \end{bmatrix} \tag{5.1}$$

and

$$\mathbf{S}^{\mathrm{B}} = \begin{bmatrix} s_{11}^{\mathrm{B}} & s_{12}^{\mathrm{B}} \\ s_{21}^{\mathrm{B}} & s_{22}^{\mathrm{B}} \end{bmatrix} \tag{5.2}$$

These matrices can be used to calculate parameters such as pre-matching impedances and insertion loss. For example, s_{22}^{A} corresponds to the central reflection coefficient presented to the DUT input port, while s_{11}^{B} corresponds to the central reflection coefficient presented to the DUT output port. The insertion loss (IL) quantifies how much power is dissipated in the matching block and is given by

$$\mathrm{IL}_{\mathrm{dB}} = 10 \log_{10} \frac{|s_{21}|^2}{1 - |s_{11}|^2} \tag{5.3}$$

The S-parameters obtained from the TRL algorithm can also be used to perform impedance verification. Once the optimum impedances have been identified

from load-pull measurements we would like to synthesize matching networks that present the targeted input ($s_{22}^{\text{A-Amp}}$) and output ($s_{11}^{\text{B-Amp}}$) reflection coefficients to the DUT, where $\mathbf{S}^{\text{A-Amp}}$ and $\mathbf{S}^{\text{B-Amp}}$ correspond to the S-parameter matrices of the input and output synthesized matching networks. For example, to perform impedance verification of the synthesized output matching network $\mathbf{S}^{\text{B-Amp}}$, the block can be connected directly following the calibrated block $\mathbf{S}^{\text{A}}$. The total S-parameters of these two cascaded blocks $\mathbf{S}^{\text{M}}$ can be measured using a network analyzer. Cascade matrices such as **ABCD** can be used to deembed the unknown output block $\mathbf{S}^{\text{B-Amp}}$ from the measured $\mathbf{S}^{\text{M}}$. The **ABCD** matrix can be obtain from the **S** matrix by [69]

$$\mathbf{ABCD} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{5.4}$$

$$= \begin{bmatrix} \frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{2s_{21}} & \frac{1}{Z_0}\frac{(1+s_{11})(1+s_{22})-s_{12}s_{21}}{2s_{21}} \\ Z_0\frac{(1-s_{11})(1-s_{22})-s_{12}s_{21}}{2s_{21}} & \frac{(1-s_{11})(1+s_{22})+s_{12}s_{21}}{2s_{21}} \end{bmatrix} \tag{5.5}$$

where Z_0 is the system impedance, usually 50-Ω. After transforming to **ABCD** matrices we obtain:

$$\mathbf{ABCD}^{\text{M}} = \mathbf{ABCD}^{\text{A}} \cdot \mathbf{ABCD}^{\text{B-Amp}} \tag{5.6}$$

Then the ABCD parameters of the unknown block $\mathbf{ABCD}^{\text{B-Amp}}$ can be easily obtained from,

$$\mathbf{ABCD}^{\text{B-Amp}} = [\mathbf{ABCD}^{\text{A}}]^{-1} \cdot \mathbf{ABCD}^{\text{M}} \tag{5.7}$$

ABCD matrices can be converted back to **S** with [69]

$$\mathbf{S} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \tag{5.8}$$

$$= \begin{bmatrix} \frac{A+B/Z_0-CZ_0-D}{A+B/Z_0+CZ_0+D} & \frac{2(AD-BC)}{A+B/Z_0+CZ_0+D} \\ \frac{2}{A+B/Z_0+CZ_0+D} & \frac{-A+B/Z_0-CZ_0+D}{A+B/Z_0+CZ_0+D} \end{bmatrix} \tag{5.9}$$

From the S-parameters the insertion loss of the output block can be calculated, as well as the output impedance presented to the device that is given by

$$Z_{\text{OUT}} = Z_0 \frac{1 + s_{11}^{\text{B}}}{1 - s_{11}^{\text{B}}} \tag{5.10}$$

The same procedure can used with the synthesized input block by connecting the unknown block $\mathbf{S}^{\text{A-Amp}}$ followed by the calibrated block $\mathbf{S}^{\text{B}}$ and measuring the combined S-parameters. After following a procedure similar to the one just described the input impedance presented to the device is calculated to be,

$$Z_{\text{IN}} = Z_0 \frac{1 + s_{22}^{\text{A}}}{1 - s_{22}^{\text{A}}} \tag{5.11}$$

This procedure can be iterated till the synthesized input and output matching networks match the identified optimum impedances.

5.2.4 Transistor Characterization

Transistor characterization begins with low supply voltage to avoid device damage due to voltage breakdown, power density, and instability. One convenient and unique property of class-E is that the optimal efficiency impedance does not change with changing supply voltage. High-efficiency impedance regions can be more safely identified at low voltage, and will not change considerably with increasing supply level.

Figure 5.4: Photograph of load-pull setup at dBm Engineering/Peak Devices facilities in Boulder, CO.

The input impedance is found using a low RF input power source pull. The objective of this test is to find a region of input impedances where the device is stable and has large gain. If the device remains unstable over the useful impedance region the input pre–match can be adjusted to stabilize the device. Parallel or series components such as capacitors or resistors can serve to suppress oscillations.

Since the load-pull technique relies on careful calibration, it is prone to errors in the absolute sense. The data should be used to determine optimum impedance regions and to observe trends in performance. A PA prototype design is required to determine the absolute performance of characterized devices.

5.3 Example with a RF3932 Prototype

The procedure described above was used for the characterization and design of a high-efficiency UHF power amplifier with a GaN HEMT on a SiC substrate. The transistor is a RF3932 prototype from RFMD capable of delivering 60 W of output power at 2 GHz in Class-AB mode. The transistor was characterized via Focus electro-mechanical tuners at the facilities of dBm Engineering/Peak Devices in Boulder, CO. A photograph of the setup is shown in Figure 5.4.

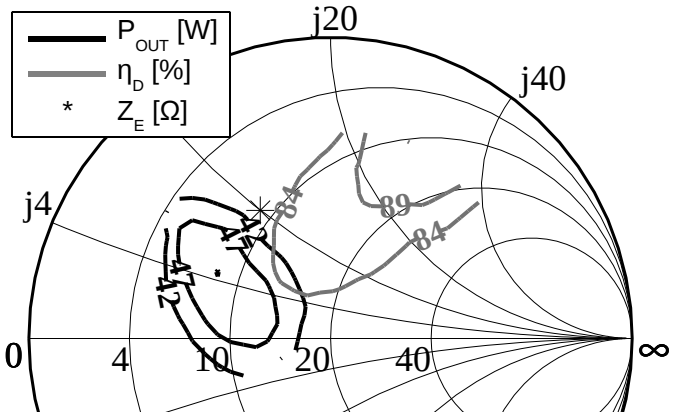


Figure 5.5: P_{OUT} (W) and η_{D} (%) load-pull contours for the RF3932 (GaN HEMT on a SiC substrate) biased at 28 V. Optimum P_{OUT} and η_{D} regions do not overlap. The figure also shows the optimal Class-E impedance ($9 + j10\,\Omega$) estimated from the device 9 pF output capacitance marked with '*'. The Smith charts is normalized to 20 Ω.

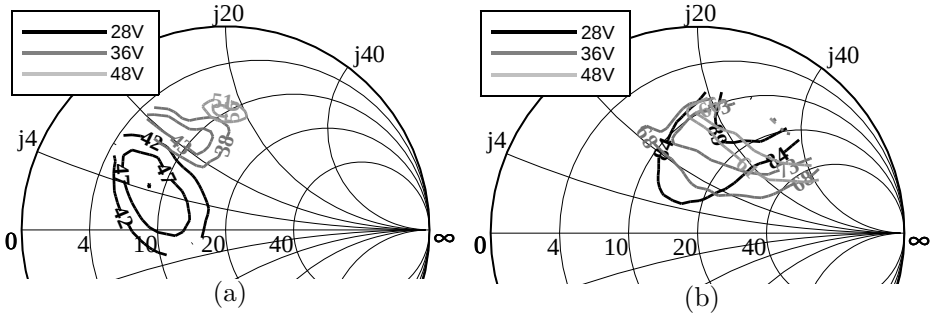


Figure 5.6: (a) P_{OUT} (W) and (b) η_{D} (%) contours when the transistor supply voltage is 28 V, 36 V and 48 V. The optimal output power impedance varies as a function of the supply voltage, while the high efficiency region remains constant. The Smith Charts are normalized to 20 Ω.

For this transistor at a frequency of 370-MHz the optimum P_{OUT} and η_{D} regions were close to 20-Ω and the Smith Chart is normalized to this value. Figure 5.5 shows measured P_{OUT} and η_{D} contours for a supply voltage of 28 V. The figure also shows the Class-E impedance predicted by the simple theoretical formulae, e.g. [23], with a 9 pF device output capacitance. From the figure it can be observed that the optimal output power and drain efficiency contours do not overlap. This means that a tradeoff analysis is necessary in order to choose the amplifier output impedance. Ultimately, the PA designer needs to deal with this analysis depending on the particular application. The next section discusses a proposed systematic optimization procedure based on a weighted Euclidean distance.

Similar measurements were taken for the device biased at 36 V and 48 V. The contours corresponding to optimal P_{OUT} are shown in Figure 5.6(a), while optimum η_{D} contours are shown in Figure 5.6(b). A trend can be observe in terms of optimum P_{OUT} as a function of supply voltage. As the supply voltage increases the imaginary part of the optimal impedance increases toward higher inductance values, while the real part remains approximately constant.

Figure 5.6(b) shows that the optimum η_{D} remains constant as the supply voltage is varied. This is consistent with Class-E theory. Assuming no varactor effect in the output capacitance the Class-E impedance should remain constant as a function of supply voltage, since the supply voltage only scales the amplitude of the voltage and current waveforms across the device but does not change their shape.

5.4 Optimum Amplifier Design

It can be seen from the examples in Figure 5.5 that a load impedance that optimizes power is not the same as the impedance that optimizes efficiency. For a

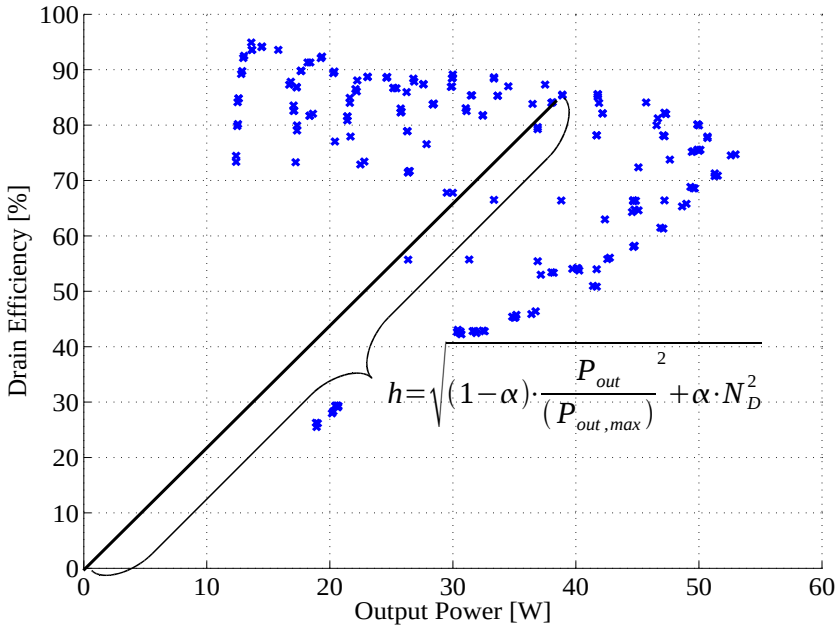


Figure 5.7: Drain efficiency values for specific output power are plotted as obtained by the load-pull measurement (Figure 5.5). The distance of each point to the origin is used a as metric for optimization.

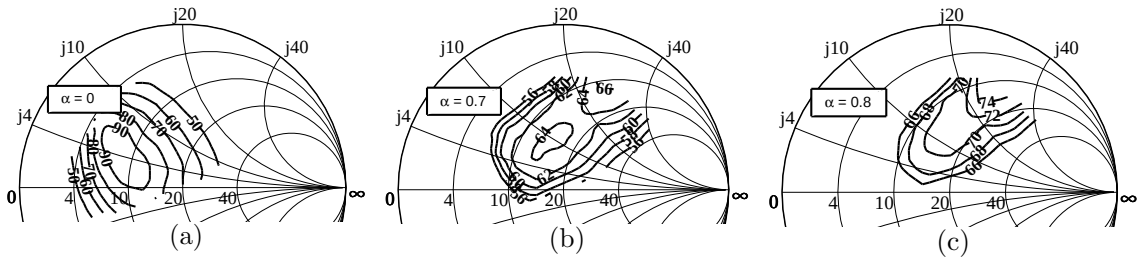


Figure 5.8: Load-pull contours in a normalized 20 Ω Smith Chart for different values of the parameter α in Equation 5.12. High values of h mean that the specific requirements for a specific tradeoff are matched for all the impedances on this contour; (a) show impedance contours for α=0, when power is optimize and efficiency is sacrificed, (b) α=0.7 gives more weighting to efficiency and (c) α=0.8 further maximizes efficiency.

particular PA design it would be useful to have a guideline of how much output power needs to be sacrificed to meet a particular efficiency specification. In this section we propose a simple method which allows a systematic approach to this tradeoff.

The method is outlined as follows:

- For each impedance the measured output power versus measured efficiency is plotted from load-pull data. An example is given in Figure 5.7;
- Given that the data deviates significantly from a straight line we defined the metric "h" as the weighted Euclidean distance from the origin;
- If defined in terms of output power and efficiency the metric is as follows;

$$h = \sqrt{(1-\alpha)\cdot\left(\frac{P_{\mathrm{OUT}}}{P_{\mathrm{OUT,\ max}}}\right)^2 + \alpha\cdot\eta_D^2} \tag{5.12}$$

- In the case when the output power is maximized without concern for efficiency, the parameter $\alpha = 0$;
- In the case when the efficiency is maximized without concern for output power sacrifice, the parameter $\alpha = 1$;
- Typically, however, there would be a tradeoff between these two parameters corresponding to different values of α between 0 and 1;
- Once α is chosen for a given design the load-pull data can be replotted to target the optimal impedance for a given tradeoff;

Examples are shown in Figure 5.8 for the load-pull data corresponding to Figure 5.5. Load-pull contours for different values of the parameter α in Equation 5.12 are chosen. High values of h mean that the specific requirements for a specific tradeoff are matched for all the impedances on this contour. For example α=0.7

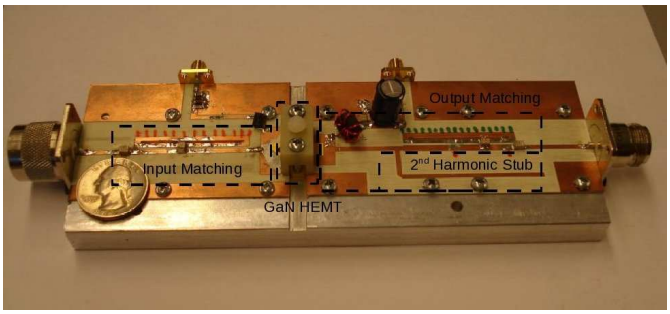


Figure 5.9: Photograph of the prototype amplifier. It is a high-efficiency power amplifier that uses a GaN HEMT on a SiC as the active device.

(Figure 5.8(b)) gives more weighting to efficiency than power. It seems that in this case the solution is not unique as there are two distinct contours that maximize the parameter h. This method can be extended to combine additional parameters in a slightly more complicated metric. For example, IMD level would be relevant for linearized Class-E PAs with envelope tracking [12]. In the presented design we choose $\alpha = 0.7$ and the resulting performance is presented in the next section.

Table 5.1: Measured Results for Class-E Amplifier

V_{DS}	Pin	Pout	Gain (dB)	η_D	PAE
28 V	+32 dBm	45 W	14 dB	87%	84%
35 V	+33 dBm	65 W	15 dB	85%	82%
48 V	+34 dBm	87 W	15 dB	71%	70%

5.5 Class-E Amplifier Performance

The measured power sweep for the $\alpha = 0.7$ amplifier is shown in Figure 5.10 for the 28 V supply voltage. The amplifier was designed using the measured load-pull data as a starting point for the output match and a similar source pull for the input match. The matching network were verified separately using the three block approach from Figure 5.3. The final impedances at the operating frequency are $Z_{\text{IN}} = 10.1 + j1\,\Omega$, and $Z_{\text{OUT}} = 12 + j6\,\Omega$. Table 5.1 shows a summary of

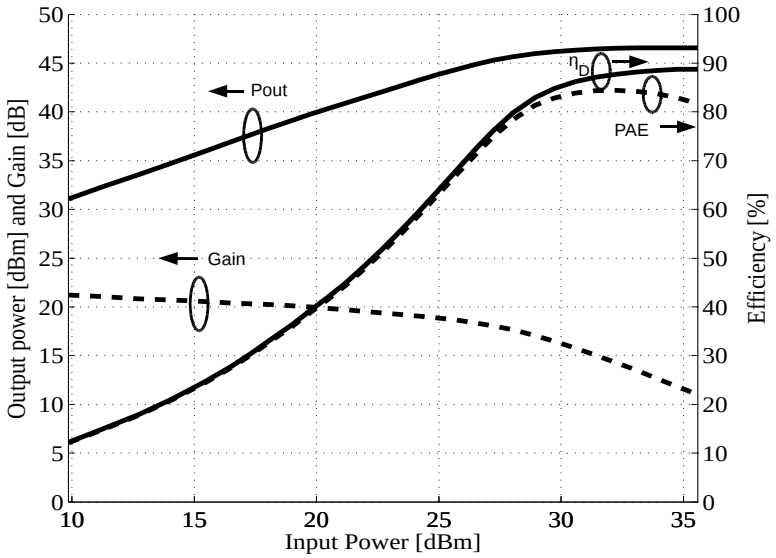


Figure 5.10: Power sweep of the Class-E mode 370-MHz Power Amplifier for a supply voltage of 28 V. The maximum PAE is 84% with a η_D of 87% with 45 W of P_{OUT}.

the measured PA performance at three different supply voltages (28 V, 35 V, and 48 V). As a trend it is observed that by increasing the supply voltage the amplifier is capable of producing additional output power at the expense of efficiency. For example, the output power increased from 45 W to 87 W by increasing the supply voltage from 28 V to 48 V. However, in this same range the η_D reduced from 87% to 71%. The supply voltage can be used as an additional dimension for optimization. It is important to remain within transistor limits to avoid permanently damaging the transistor.

5.6 Summary

The main objective of the work presented in this chapter is to layout the steps for designing high-efficiency transmission line hybrid class-E power amplifiers. Due to the highly nonlinear behavior of Class-E amplifiers, transistor characterization via load-pull techniques are more reliable than using nonlinear models. A RF3932 GaN HEMT on a SiC substrate prototype from RFMD is used to illus-

trate the steps for amplifier design. Load-pull data showed little overlap between optimum output power contours and optimum drain efficiency contours. An optimization procedure based on weighted Euclidean distance is developed as an objective method for optimum impedance selection. The implemented amplifier achieves $P_{\mathrm{OUT}} = 45\,\mathrm{W}$ with $\eta_{\mathrm{D}} = 87\%$ with $V_{\mathrm{DS}} = 28\,\mathrm{V}$ at $370\,\mathrm{MHz}$. Additional output power can be achieved by increasing the supply voltage at the expense of efficiency. The supply voltage can be an additional parameter for amplifier optimization.

Chapter 6

Technology Comparison of UHF Amplifiers

6.1 Introduction

State-of-the-art wide-bandgap semiconductor RF transistors are delivering record-breaking power levels in the UHF and lower microwave frequency range, with demonstrations of excellent amplifiers as reported in [6], [18], [70] - [73]. Wide-bandgap semiconductors have better intrinsic material properties than silicon, i.e. larger energy gap (support higher internal electric fields before breakdown), lower relative permittivity (lower capacitive loading), higher thermal conductivity (higher heat handling), and higher critical electric fields (higher RF power) [74]. High voltage operation and high power density with low parasitic reactance translate into robust devices that can withstand high-stress conditions typically associated with switch-mode operation. For example, in Class-E mode the peak voltage across the device can be more than 3.56 times higher than the supply voltage [26]. The supply voltage must then be limited by this factor ($V_{\mathrm{DSS}}/3.56$ where V_{DSS} is the absolute maximum drain-to-source voltage). Therefore, devices with high

breakdown voltage are ideal for this mode of operation.

In this work, the performance of wide-bandgap transistors (GaN HEMTs on a Si substrate, GaN HEMTs on a SiC substrate, and SiC MESFETs) is compared to standard Si LDMOS by designing UHF high-power high-efficiency transmission line Class-E power amplifiers. Load-pull techniques under Class-E conditions are used for device characterization. Finally, the power amplifiers are compared in terms of output power, gain, PAE and static distortion.

6.2 Transistor Technologies

The four different transistor technologies compared in this work are GaN HEMT on a Si substrate, GaN HEMT on a SiC substrate, SiC MESFET, and Si LDMOS. Today, the two main substrates used to grow GaN HEMTs are either Si or SiC. The main advantages of Si as a substrate for GaN is its low cost, and devices are commercially available in a variety of power levels ranging from 4 W to 180 W, with a promise of 200 V breakdown voltage [75]. SiC substrates are expensive, but the thermal conductivity is about 2.6 times higher than that of Si (4 W/°k-cm for SiC vs. 1.5 W/°k-cm for Si) [74]. Thermal conductivity is critical for high-power PAs because device performance degrades with temperature. For additional information on wide-bandgap transistors the reader is refered to [76]. The devices used in this work have no internal prematching and they are:

- *GaN HEMT on a Si substrate*

  Transistor used is the NPTB00050 from Nitronex. This transistor is able to deliver 50 W of output power with 11.5 dB of gain and 60% η_D at 3 GHz with a supply voltage of 28 V. The breakdown voltage is 100 V, the output capacitance is 9 pF and the threshold voltage is about -2.1 V.

- *GaN HEMT on a SiC substrate*

  Transistor used is a RF3932 prototype from RFMD. The transistor can deliver 60 W of peak power and it is rated for 48 V operation with 14 dB of gain in Class-AB. It has 9 pF of output capacitance and a threshold voltage of -4.2 V.

- *SiC MESFET*

  Transistor used is the CRF24060 from Cree. It is rated for operation up to 2.4 GHz with 13 dB of gain and 50 W of output power in Class-AB. It has a typical performance of 60 W of output power with 45% η_D at 1.5 GHz with a supply voltage of 48 V. The threshold voltage is -10 V and the output capacitance is approximately 11 pF.

- *Si LDMOS*

  The transistor used is the AGR09045E from Peak Devices/Agere. Its recommended operation is from 865 MHz to 895 MHz with 45 W of output power, and η_D of 59%. The breakdown voltage is 65 V and the threshold voltage is 3.5 V. The output capacitance is 23 pF.

Table 6.1 summarizes device parameters, i.e. drain-to-source breakdown voltage, output capacitance, $R_{ON\ DC}$, junction temperature and turn on threshold voltage.

Table 6.1: Summary of Transistor Properties

Part Number	V_{DSS}	C_{OUT}	$R_{ON\text{-}DC}$	T_J	V_{TH}
NPTB00050	100 V	9 pF	0.23 Ω	200°C	-2.1 V
RF3932	150 V	9 pF	0.32 Ω	250°C	-4.2 V
CRF24060	120 V	11 pF	0.46 Ω	250°C	-10 V
AGR09045E	65 V	23 pF	0.35 Ω	200°C	3.5 V

The breakdown voltage of wide-bandgap transistors is over 100 V, while standard Si LDMOS in only 65 V. Higher voltages lead to higher matching impedances. Also, in Class-E operation the drain-to-source voltage should be limited to at least 1/3.56 the breakdown voltage of the device to avoid permanently damaging the transistor. This might limit the maximum output power attainable in Class-E mode.

Matching impedances are not only affected by the supply voltage, but by the output capacitance as well [2]. The higher dielectric value of Si and its lower critical field (a larger number of fingers is needed to achieve desired P_{OUT} compared to GaN) results in an output capacitance more than twice that of wide-bandgap transistors. This parameter also limits the maximum frequency for Class-E operation.

Another important parameter for Class-E operation is the transistor R_{ON}. The R_{ON} limits the maximum efficiency attainable with these devices in Class-E mode. Table 6.1 shows the measured $R_{\mathrm{DC\,ON}}$ for each of the transistor technologies. The lower value was obtained with the GaN HEMT on a Si substrate (0.23 Ω) followed by the GaN HEMT on a SiC substrate (0.32 Ω), while the largest value was obtained with the SiC MESFET (0.46 Ω). The table also shows the maximum junction temperature and the threshold voltage.

6.3 Transistor Characterization in Class-E Mode

A transistor of each of the four different technologies was characterized with the procedure described in the previous chapter at an operating frequency of 370 MHz. The P_{OUT} and η_{D} load-pull contours for a supply voltage of 28 V when the device is in compression are shown in Figure 6.1. Closed contours for the Si LDMOS were not obtained due to voltage breakdown problems. The supply voltage of

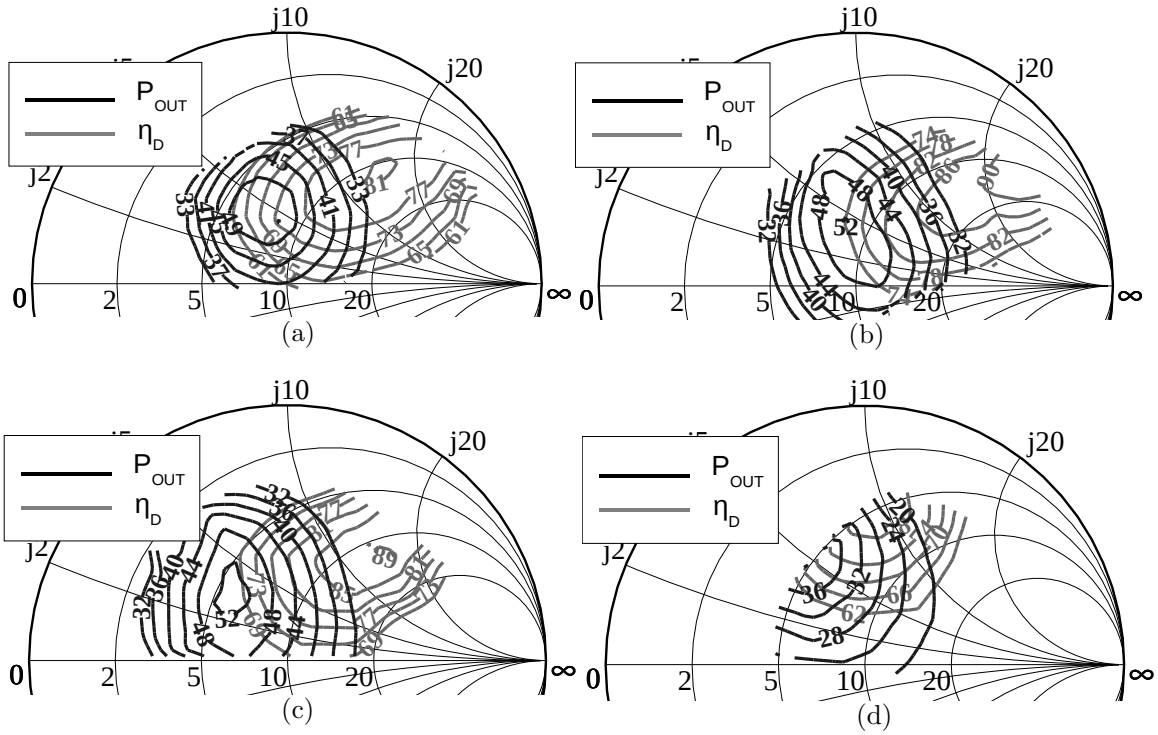


Figure 6.1: P_{OUT} and η_{D} load-pull contours for each of the four different transistor technologies at a supply voltage of 28 V in a 10-Ω Smith Chart. (a) GaN HEMT on a Si substrate, (b) GaN HEMT on a SiC substrate, (c) SiC MESFET, and (d) Si LDMOS. Notice that optimum P_{OUT} contours do not overlap with optimum η_{D} contours.

28 V exceeds the maximum allowed for Class-E mode which is 18 V (65 V/3.56).

In this set of data the main difference between wide-bandgap transistors and Si LDMOS is the value of the output capacitance. The output capacitance for the wide-bandgap transistors is between 9 pF to 11 pF, while for the Si LDMOS is 23 pF. It is interesting to observe the rotation of the optimal efficiency region as a function of output capacitance. If the intrinsic output capacitance keeps increasing, the transistor will no longer be operating in Class-E mode, but in Class-AB.

From Figure 6.1 we can observe that the optimal output power regions do not overlap with the optimal drain efficiency regions. Table 6.2 summarizes performance for each of the transistors in the optimum P_{OUT} and optimum η_{D}

Table 6.2: Optimum P_{OUT} and η_D Impedances from Load-pull Contours.

Part Number	Optimum P_{OUT}	Optimum η_D
NPTB00050	63 W, 68% @ 5+j7.5Ω	30 W, 84% @ 14+j22Ω
RF3932	53 W, 75% @ 8+j4.4Ω	14 W, 93% @ 11.8+j2.9Ω
CRF24060	53 W, 70% @ 6+j3.6Ω	20 W, 89% @ 13.5+j16Ω
AGR09045E	40 W, 74% @ 5.2+j5.6Ω	24 W, 82% @ 4+j9.3Ω

impedances. A tradeoff analysis as the one proposed in the previous chapter is necessary in order to choose the amplifier optimum output impedance.

6.4 Class-E Amplifier Performance

Amplifier prototypes were implemented with each of the transistor technologies. It is important to point out that in the remainder of this chapter, measured results for the PA prototypes are compared, whereas it might not be a direct comparison of transistor technologies.

The goals for these prototypes are to achieve $P_{OUT} > 40$ W with $\eta_D > 80\%$. The efficiency goal is much harder to meet. Increasing the supply voltage usually increases P_{OUT} at the expense of η_D. The supply voltages used for each of the prototypes are 28 V for the GaN HEMTs, 35 V for the SiC MESFET and 18 V for the Si LDMOS. The supply voltage for the Si LDMOS is limited to only 18 V because of transistor failure at higher levels. However, even for this low voltage the Si LDMOS was able to meet the specifications of 40 W and 80%. As for the SiC MESFET, the output matching gave significantly more weight to η_D with less P_{OUT} and the supply voltage had to be increased to 35 V to meet the power goal.

The amplifiers were tested while sweeping the input power, and sweeping the supply voltage. For the input power sweep, the supply voltage is held constant while P_{IN} increases until the amplifier starts to saturate and a peak is observed in the PAE. This results in an optimum P_{IN} for a given PAE. In the supply sweep,

Table 6.3: Prototypes Power Sweep Performance

Part Number	V_{DS}	P_{IN}	P_{OUT}	Gain	η_D	PAE
NPTB00050	28 V	+29 dBm	43 W	17.5 dB	83%	81%
RF3932	28 V	+32 dBm	45 W	14.6 dB	85%	82%
CRF24060	35 V	+31 dBm	40.5 W	15 dB	80%	78%
AGR09045E	18 V	+34 dBm	42.6 W	12.5 dB	80%	75%

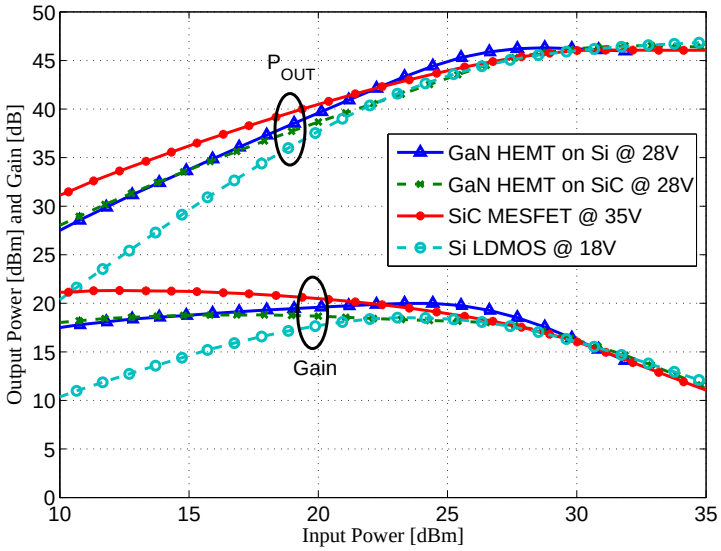
the amplifier P_{IN} is fixed to this optimum value while the supply voltage varies from 0 V up to a maximum supply voltage. For each of these sweeps parameters such as P_{OUT}, Gain, and PAE are recorded. Supply sweeps are important because these amplifiers are intended for polar transmitters. Also, for this application it is important to measure the amplifiers' AM-to-AM and AM-to-PM properties. Results for these sweeps are discussed next.

6.4.1 Input Power Sweep

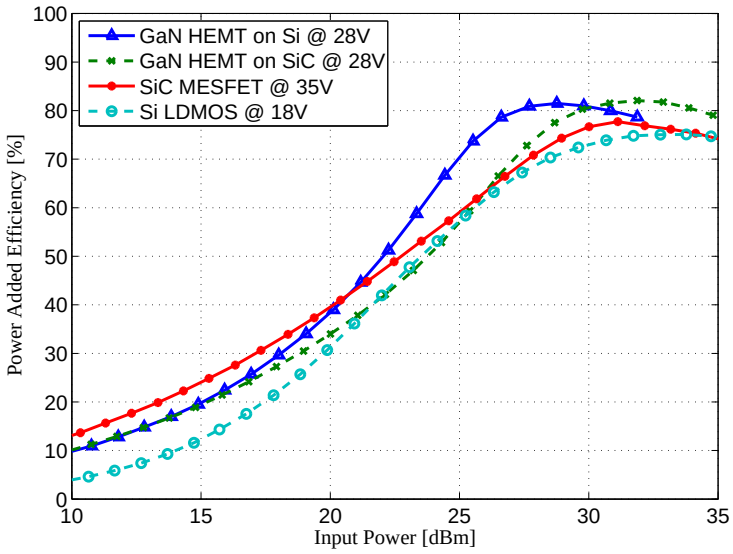
Figure 6.2 shows measured P_{OUT}, Gain and PAE as a function of P_{IN} for each of the amplifier prototypes. In terms of P_{OUT}, Figure 6.2(a) shows that each of the amplifiers is able to reach over 40 W (+46 dBm). This same figure shows that for these prototypes the saturated gain follows a similar path. It is important to point out the differences in supply voltage for each of the prototypes as discussed above (28 V for the GaN HEMTs, 35 V for the SiC MESFET and 18 V for Si LDMOS). Table 6.3 summarizes the performance of the four prototypes.

Figure 6.2(b) shows the measured PAE for each of the amplifiers. Some interesting plot properties are:

- PAE is above 80% for the GaN HEMTs amplifiers.
- The GaN HEMT on a Si substrate amplifier compresses with 3 dB less P_{IN} compared to the GaN HEMT on a SiC substrate amplifier, requiring less drive.



(a)



(b)

Figure 6.2: Input power sweep for each of the amplifier prototypes: GaN HEMT on a Si substrate biased at 28 V, GaN HEMT on a SiC substrate biased at 28 V, SiC MESFET biased at 35 V and Si LDMOS biased at 18 V. (a) P_{OUT} and Gain, and (b) PAE versus P_{IN}.

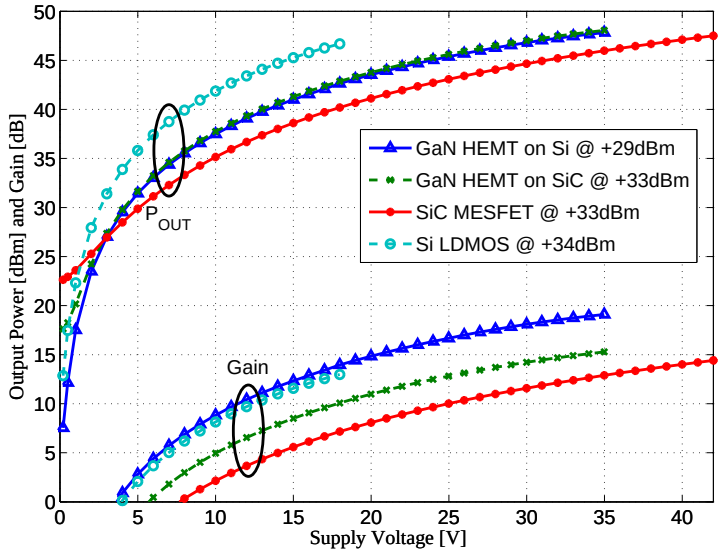
- All the amplifiers achieve more than 75% PAE.
- PAE achieved by the SiC MESFET is between the PAE acheived by the GaN HEMTs and the Si LDMOS.

6.4.2 Supply Voltage Sweep

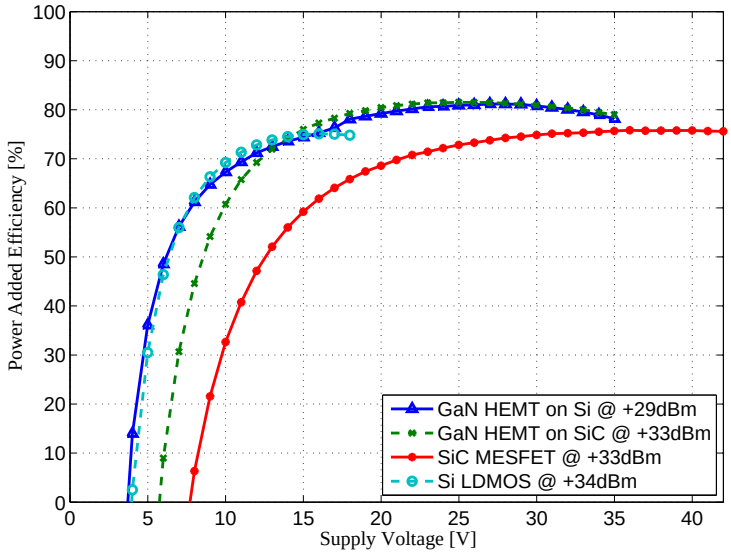
Figure 6.3 shows P_{OUT}, gain and PAE as a function of the supply voltage for each of the four amplifiers with dynamic biasing for linearization in mind. In this measurement, the input power is fixed to the one that gives optimum PAE in the input power sweep, while the supply voltage is swept from 0 V up to a maximum supply voltage. The maximum voltage is transistor dependent ($V_{\mathrm{DSS}}/3.56$).

Figure 6.3(a) shows P_{OUT} and gain. All the amplifiers reach P_{OUT} higher than the specified but not at the same supply voltage. The Si LDMOS prototype amplifier reaches the specified output power for lower supply volage than the other ones. The performance of the GaN HEMTs amplifiers is identical, while higher voltage is needed for the SiC MESFET amplifier. Additional P_{OUT} can be achieved at higher supply voltages, however it is important to consider the transistor breakdown voltage. The figure also shows the amplifier gain as a function of supply voltage. Below an amplifier-dependent supply voltage threshold, the gain is negative and the amplifier attenuates the input signal. The amplifiers with higher gain are the GaN HEMT on a Si substrate and the Si LDMOS. The amplifier implemented with the SiC MESFET has the lowest gain.

Figure 6.3(b) shows PAE as a function of supply voltage. Due to the PAE dependence upon the amplifier gain, the PAE is negative for voltages where P_{OUT} is lower than P_{IN}. In this plot we can observe the advantages of high gain and high breakdown voltage. These two conditions ensure high overall PAE. If the amplifier is used in a polar transmitter with a specified modulation scheme, the



(a)



(b)

Figure 6.3: Supply voltage sweep for each of the amplifier prototypes: GaN HEMT on a Si substrate with +29 dBm of P_{IN}, GaN HEMT on a SiC substrate with +33 dBm of P_{IN}, SiC MESFET with +33 dBm of P_{IN}, and Si LDMOS with +34 dBm of P_{IN}. (a) P_{OUT} and Gain, and (b) PAE versus supply voltage.

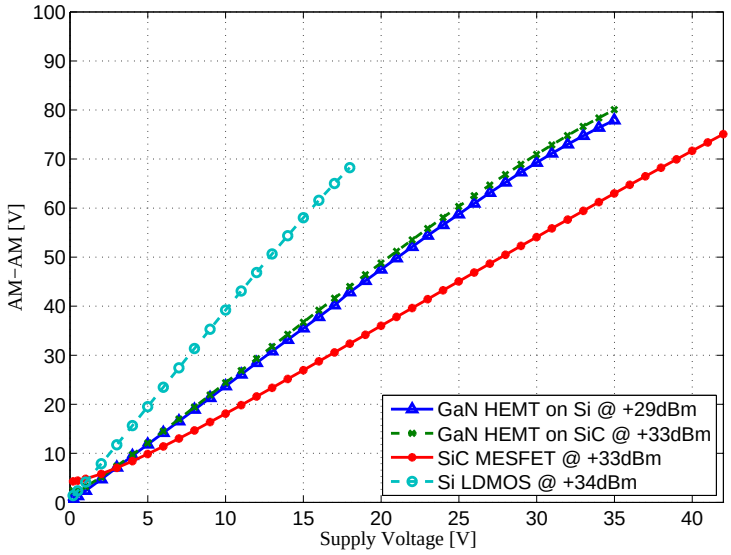
input power and the supply voltage range can be optimized in terms of power consumption efficiency.

6.4.3 AM-to-AM and AM-to-PM Distortion

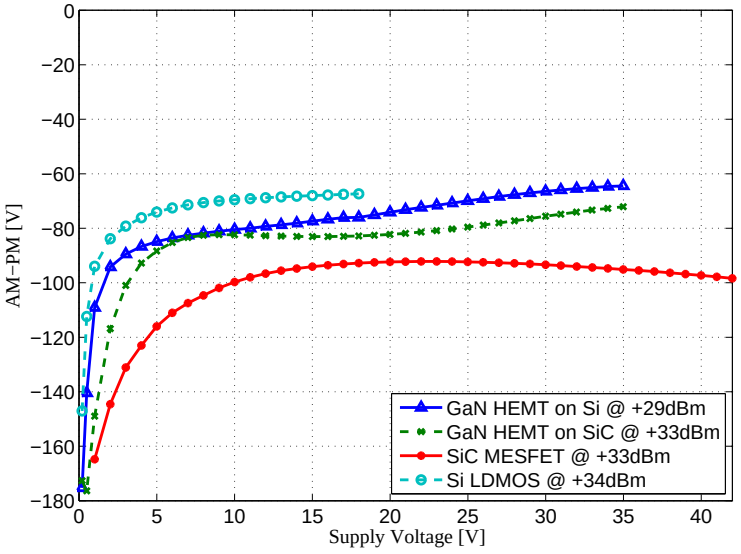
In polar transmitters the two main sources of distortion are AM-to-AM and AM-to-PM. The first describes how the supply voltage affects the RF output voltage across a constant load, and the second relates the supply voltage and the phase difference between the PA input and output RF signals. Figure 6.4 shows these two sources of distortion for each of the amplifier prototypes.

Figure 6.4(a) shows AM-to-AM curves and a linear relation can be observed. At low voltages AM–to–AM curves are limited due to feedthrough, related to the leakage from input to output due to the transistor internal capacitances at a supply voltage of 0 V. At the other end, the amplifier is limited by either saturation or breakdown voltage. A third interesting parameter is the slope, which is higher for Si LDMOS, followed by GaN HEMTs, while the smallest slope corresponds to the SiC MESFET. The slope of the AM-to-AM line depends on impedance matching. We can observe that in order to achieve the output power requirements with the Si LDMOS transistor, the impedance matching was agressive towards achieving the power at a low voltage (18 V). For the SiC MESFET, significant weight was given to efficiency. As a consequence, a higher voltage was needed to achieve the desired P_{OUT} specification, therefore a smaller slope. The GaN HEMTs were matched at some point in between.

The AM-to-PM characteristics for each of the amplifiers is plotted in Figure 6.4(b). The AM-to-PM distortion is characterized by an abrupt knee at lower voltages. This distortion should be corrected with predistortion because it has significant effects on ACPR and EVM in polar transmitters. GaN HEMT on a Si substrate shows the smallest knee voltage, followed by the Si LDMOS. The SiC



(a)



(b)

Figure 6.4: (a) AM–to–AM and (b) AM–to–PM for each of the amplifier prototypes: GaN HEMT on Si with +29 dBm of P_{IN}, GaN HEMT on SiC with +33 dBm of P_{IN}, SiC MESFET with +33 dBm of P_{IN}, and Si LDMOS with +34 dBm of P_{IN}. The feedthrough values for the prototypes (GaN HEMT on a Si substrate, GaN HEMT on a SiC substrate, SiC MESFET and Si LDMOS) are 0.75 V, 2.4 V, 4.28 V and 1.39 V (respectively).

MESFET amplifier has the largest knee. Ideally, it is desired that this response is constant. We can observe from the figure that the overall shape is amplifier dependent.

6.5 Discussion of Results

In this work, high-efficiency UHF power amplifiers were designed with four different transistor technologies; GaN HEMT on a Si substrate (NPTB00050 from Nitronex), GaN HEMT on a SiC substrate (RF3932 prototype from RFMD), SiC MESFET (CRF24060 for CREE), and Si LDMOS (AGR09045E from Peak Devices/Agere). These transistors have similar output power capabilities. Specifications such as breakdown voltage, output capacitance, and $R_{\mathrm{ON\,DC}}$ were given for each of these transistors.

A modular fixture that allows TRL calibration and impedance verification was designed and the transistors were characterized with a load-pull measurement system under Class-E conditions. The P_{OUT} and η_{D} load-pull contours showed that for wide–bandgap transistors used at UHF there is a significant tradeoff between P_{OUT} and η_{D} since the contours do not overlap. A simple optimization procedure, based on a weighted Euclidean distance was applied in order to deal with this tradeoff.

Transmission line Class-E amplifier prototypes were implemented for each of the transistor technologies. These prototypes had the specification of achieving more than 40 W of P_{OUT} with over 80% η_{D}. Input power and supply sweeps characterized performance of each amplifier prototype. The prototypes were also characterized in terms AM-to-AM and AM-to-PM, due to potential use in polar transmitters. Following is a brief summary of the overall technology performance.

- *GaN HEMT on a Si substrate*

The particular Nitronex transistor used in this work, has lower $R_{\mathrm{ON\,DC}}$ compared to the other technologies and a low output capacitance of approximately 9 pF. The prototype built with this transistor seems to have good overall performance. It had the largest gain and best properties for polar transmitters; regarding AM-to-AM characteristics it had the the lowest feedthrough and regarding AM-to-PM the lowest knee voltage, and a relatively flat response.

- *GaN HEMT on a SiC substrate*

  The overall performance of the RFMD GaN HEMT on a SiC substrate was comparable to that of the GaN HEMT on a Si substrate, with the advantage of a higher breakdown voltage. The main advantages of a higher breakdown voltage is that the implemented matching network can be weighted more towards optimum efficiency, because more output power can be obtained at a larger supply voltage.

- *SiC MESFET*

  Due to the larger R_{ON} resistance of the CREE SiC MESFET transistor compared to the tested GaN HEMTs, the amplifier prototype impedance matching network gave a lot of weight towards optimizing efficiency. The supply voltage needed to be increased to 35 V in order to achieve performance comparable to the other prototypes. Tests showed high output power with little degradation in efficiency for voltages above 42 V (70 W of P_{OUT} with 77% η_{D} with a supply voltage of 47 V).

- *Si LDMOS*

  The AGR09045E Peak Devices/Agere LDMOS has the largest output capacitance (23 pF) and lowest breakdown voltage (65 V) compared to the

other technologies. Its overall performance was comparable to the other technologies, although the low breakdown voltage played a significant role in its limitation.

6.6 Summary

The main objective of the work presented in this chapter is to assess the benefits of wide-bandgap transistors compared to standard Si LDMOS at UHF by designing high-efficiency power amplifiers. Si LDMOS has been the technology of choice at UHF, and wide-bandgap transistors have been designed to target the GHz range. The low cost of Si LDMOS compared to new wide-bandgap transistor and its reliable performance are dominant factors to keep Si LDMOS as the technology of choice. However, wide-bandgap transistor also demonstrate excellent performance at UHF with the advantage of higher breakdown voltage, and lower output capacitance leading to higher output matching impedances and additional flexibility in amplifier design. For example, the output matching design can give higher weight towards improving efficiency, since higher output power can usually be achieved by increasing the supply voltage. The specific contributions contained in this thesis are as follows:

- Design and implementation of high-efficiency power amplifiers at UHF with new wide-bandgap technologies; GaN HEMT on a Si substrate, GaN HEMT on a SiC substrate, and SiC MESFET.

- Performance comparison of amplifiers implemented with wide-bandgap transistors to an amplifier implemented with standard Si LDMOS.

Chapter 7

Discussion & Future Work

7.1 Discussion

The topic of this thesis is efficiency optimization in UHF and microwave power amplifiers used in communications systems. In order to eventually obtain an amplifier architecture in which efficiency and linearity can be optimized for a given signal, some choices have to be made. For example, a specific class of single-ended transistor operation for the RFPA can be chosen to enable straightforward dynamic biasing. The choice of class-E with its soft-switching properties is also appropriate for hybrid circuit implementation for which some tolerance for component values is advantageous. At the beginning of this work, it was an open question as to what type of transistor works best in this switched-mode of operation. In addition to well known devices such as MESFETs and Si LDMOS, new emerging technologies such as GaN HEMTs and SiC MESFETs needed to be considered.

After choosing the type of PA, which is not commonly used in commercial products, amplifiers over a wide frequency range were implemented. 60 W single device amplifiers with over 80% efficiency at 370 MHz were designed in pure class-E

mode, while it was shown that at higher frequencies the devices operate in a sub-optimal, slightly degraded class-E mode. Nevertheless, the results demonstrated for EDGE signals at 880-MHz and the results at 10 GHz are highest reported in the literature.

In order to linearize the PAs with minimal added complexity and minimal sacrifice in efficiency, a choice was made for the linearization technique which matches the class-E operation. This polar architecture was then demonstrated at 880-MHz and 10-GHz with some of the best reported simultaneous linearity and efficiency as demonstrated by spectral mask measurements and reduction in IMD level.

The results of this work open up numerous possibilities for future research as it will be discussed in the next section. On the power amplifier side, modified modes of operation, with different harmonic terminations are likely to give improved performance especially for higher powers and at lower microwave frequencies. As semiconductor technologies improve, more power will be available from single GaN transistors with higher supply voltages and the technique developed in this thesis can be directly applied to this future devices. For even higher power levels, low loss combining techniques need to be investigated.

In terms of linearization for communication transmitters the trend of increasing bandwidth and spectral efficiency will demand new integrated solutions such as possibly combinations of polar, outphasing and predistortion.

The specific contributions contained in this thesis are as follows:

- The repeatability of the 10-GHz amplifier characterization, and load-pull measurements with single and two-tone (Cartesian and polar) excitation was verified, as well as an investigation of proper design of bias circuitry for RFPAs in polar transmitters [12], [17].

- Design and implementation of a transmission line hybrid Class-E power amplifier for the 880-MHz polar transmitter. The maximal PAE is 70% with η_D of 75% with $P_{OUT} = +20\,\text{dBm}$. The maximal P_{OUT} is $+22.4\,\text{dBm}$ with little degradation in PAE [15].

- The amplifier is linearized with an efficient envelope tracker [16].

- The total transmitter efficiency is 56% with $P_{OUT} = +20\,\text{dBm}$ for EDGE signals. This is the highest efficiency reported for a EDGE polar transmitter that meets the EDGE mask [17]. The closest work [56] is a parallel effort at the University of California, San Diego with a 44% efficient polar transmitter with the same output power.

- Development of an optimization procedure based on weighted Euclidean distance an objective method for optimum impedance selection [18]. This contribution will be very useful for future designs, and thus more examples are given in Section 7.2.

- Implementation of a UHF high-efficiency amplifier implemented with a GaN HEMT on a SiC substrate that achieves $P_{OUT} = 45\,\text{W}$ with $\eta_D = 87\%$ with $V_{DS} = 28\,\text{V}$ at $370\,\text{MHz}$ [18]. These PAs were design using a commercial Focus load-pull system. Some of the active devices are in the experimental stage and the manufacturer provided no specs. Another in-house developed active load-pull technique could prove useful in the future, and some results developed for the work in this thesis is described in Section 7.4.

- Design and implementation of high-efficiency power amplifiers at UHF with new wide-bandgap technologies; GaN HEMT on a Si substrate, GaN HEMT on a SiC substrate, and SiC MESFET [19].

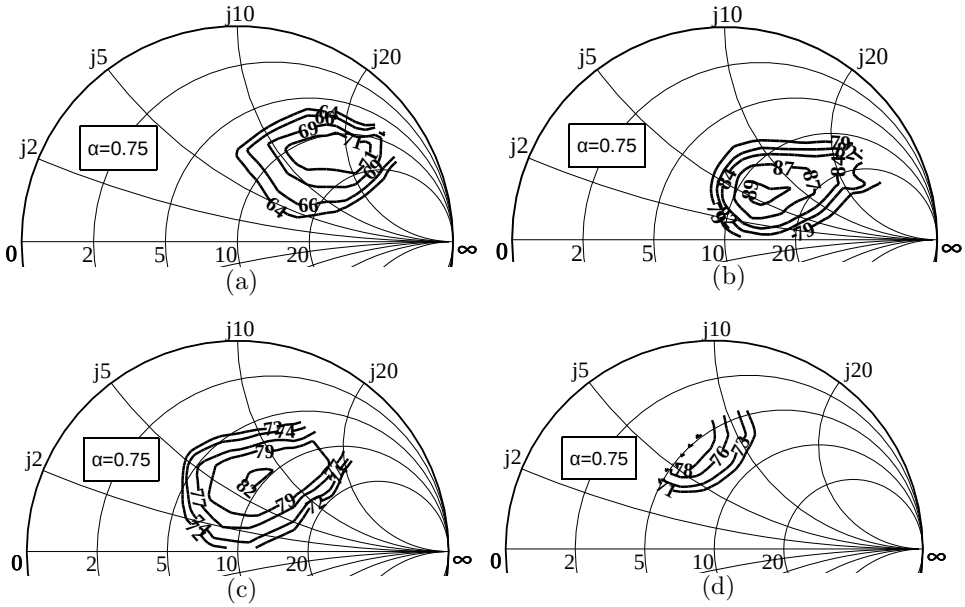


Figure 7.1: Load-pull contours for the parameter $h_{\alpha=0.75}$ of Equation 5.12 for each of the four different technologies and a supply voltage of 28 V. (a) GaN HEMT on a Si substrate, (b) GaN HEMT on a SiC substrate, (c) SiC MESFET, and (d) Si LDMOS. Notice that optimum h depends significantly upon technology.

- Performance comparison of amplifiers implemented with wide-bandgap transistors to an amplifier implemented with standard Si LDMOS [19].

7.2 Additional Optimization Examples

Section 5.4 introduces a proposed method for the design of optimal power amplifiers. Amplifier design consists of biasing and impedance matching. Load-pull techniques allows transistors to be characterized under different input and output impedance terminations. In cases as the one discussed in Chapter 5 impedance selection is non-trivial as different impedances provide desired functionality such as maximal output power or maximal efficiency. Additional contours can be obtained from load-pull in terms of measurable quantities such as additive phase noise or IMD level. The amount of data increases if parameters such as supply

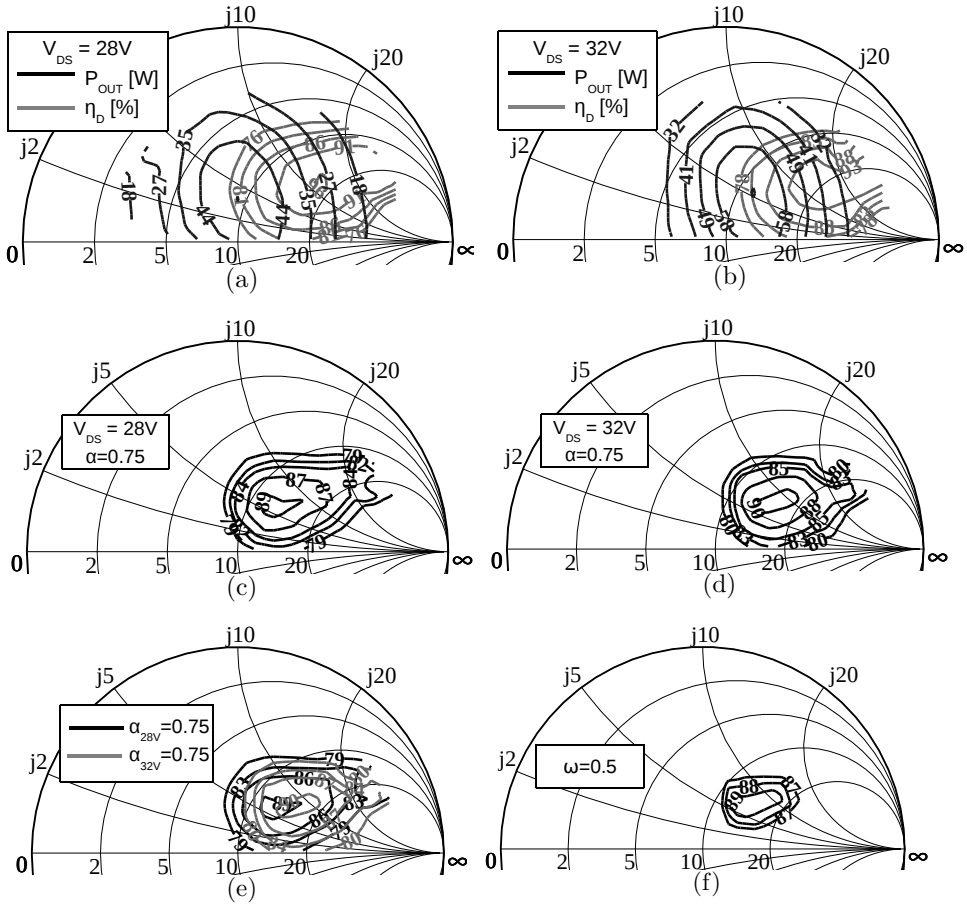


Figure 7.2: P_{OUT} and η_{D} load-pull contours for the RF3932 for a supply voltage of (a) 28 V, and (b) 32 V. (c) h for an $\alpha = 0.75$ and a supply voltage of 28 V, and (d) 32 V. (d) h for an $\alpha = 0.75$ and supply voltages of 28 V and 32 V, and (e) farther combined h contours (h_ω) for an $\omega = 0.5$.

voltage are also taken into account. Due to the large quantity of information it is a difficult task to objectively select optimal impedances even if a very specific application is in mind. It is in this sense that a method just as the one described in Section 5.4 is important.

Figure 7.1 shows additional examples of optimized contours. In this case for an $\alpha = 0.75$ in Equation 5.12 is chosen for each of the transistors characterized in Chapter 6. As can be seen from the figure the optimal impedance depends significantly upon technology.

This technique also allows for additional optimization by combining for example voltage dependence. By defining:

$$h_\omega = \sqrt{(1-\omega)\cdot h_{V1}^2 + \omega \cdot h_{V2}^2} \tag{7.1}$$

an overall optimal result that combines h_α contours for specified voltages is obtained. Figure 7.2 shows a sequence of contours that combine P_{OUT} and η_{D} for two different voltages, 28 V and 32 V for the RF3932. It is interesting to observe how the data from Figures 7.2 (a) and (b) is simplified to the one shown in Figure 7.2(e). This optimization procedure allows for the consideration of voltage dependent effects when designing amplifiers with dynamic biasing. The weighting coefficients can potentially be the envelope PDF of the modulation scheme to be used.

7.3 Class-F Transistor Characterization

The procedure described in Section 5.2 was used for transistor characterization in Class-F mode. In Class-F the 2$^{\mathrm{nd}}$ harmonic is terminated with a short circuit, while the 3$^{\mathrm{rd}}$ harmonic is terminated with an open stub as shown in Figure 7.3. The wide-bandgap transistors were characterized under these conditions for a supply voltage of 28 V. The P_{OUT} and η_{D} load-pull contours are shown in Figure 7.4. It is important to notice the difference in impedances compared to Class-E. This means that harmonic terminations affect the necessary impedances for optimal output power or efficiency at the fundamental frequency. Table 7.1 summarizes the measured data. It was observed that the tradeoff between $\mathrm{P_{OUT}}$ and η_{D} is not as severe as in Class-E. Due to time constraints Class-F prototypes were not implemented.

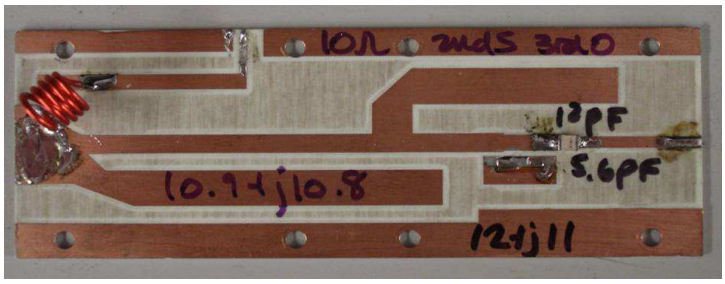


Figure 7.3: Output matching network for Class-F operation. For Class-F transistor characterization the 2nd harmonic is terminated with a short circuit, while the 3rd harmonic is terminated with an open stub.

Table 7.1: Class-F Optimum P_{OUT} and η_D.

Part Number	Optimum P_{OUT}	Optimum η_D
NPTB00050	50 W, 77% @ 11.2-j3.6Ω	40 W, 86% @ 13+j0.4Ω
RF3932	42 W, 67% @ 8.6-j4.7Ω	30 W, 75% @ 19-j5Ω
CRF24060	54 W, 66% @ 6.8-j5.9Ω	37 W, 76% @ 15-j1.9Ω

7.4 Active Load-pull

The procedure for amplifier design via load-pull is as followed:

(1) Select transistor to be used.

(2) Select mode of operation, i.e. Class-A, Class-AB, Class-E, Class-E, etc...

(3) Characterize transistor in the desired mode of operation at the correct biasing conditions.

(4) Synthesize and verify input and output matching networks.

(5) Test prototype.

(6) Load-pull the prototype to ensure it is delivering optimum performance.

In this work, the transistor were characterized in dBm Engineering/Peak Devices/TriQuint facilities in Boulder, CO and it was impractical to repeat load-pull for every designed prototype. An active load-pull system was implemented to

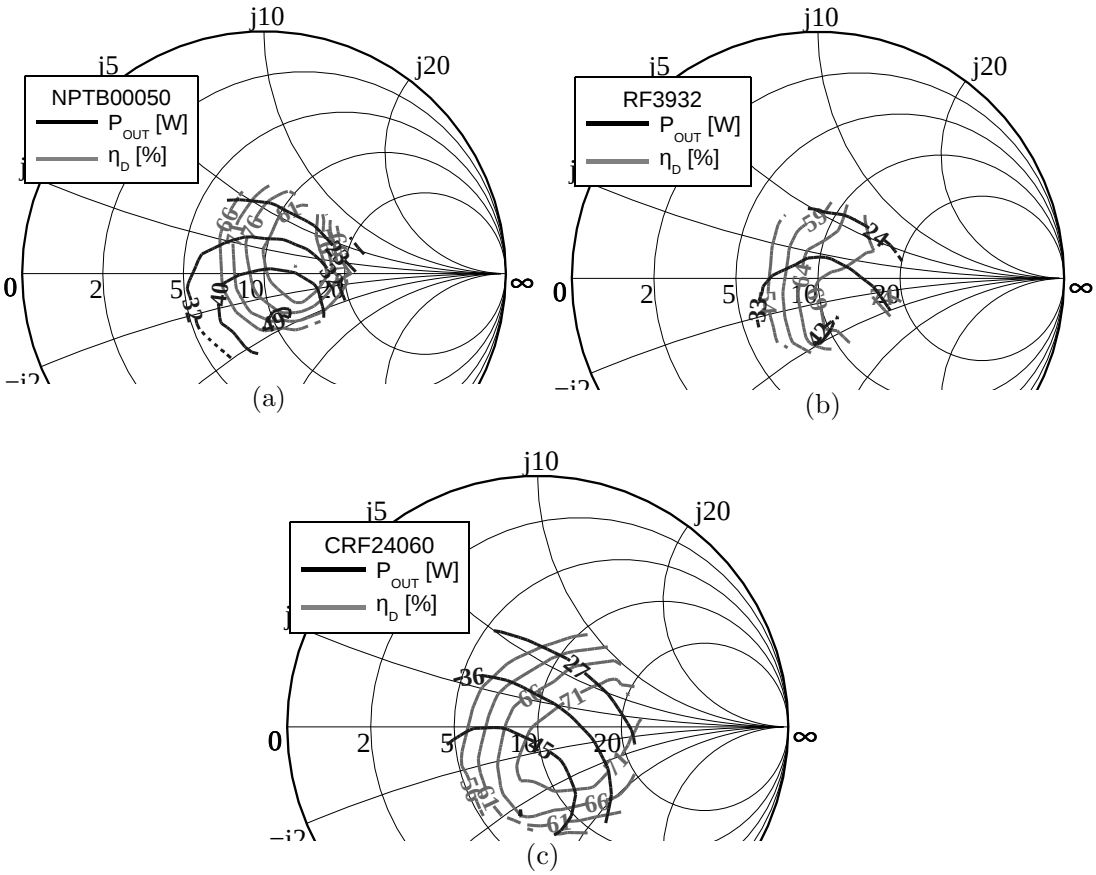


Figure 7.4: P_{OUT} and η_{D} load-pull contours for three different transistor technologies for a supply voltage of 28 V and Class-F terminations.(a) GaN HEMT on a Si substrate, (b) GaN HEMT on a SiC substrate, and (c) SiC MESFET.

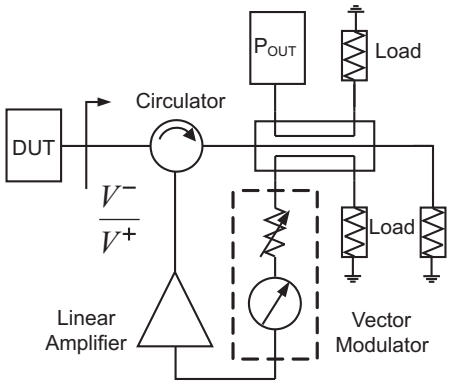
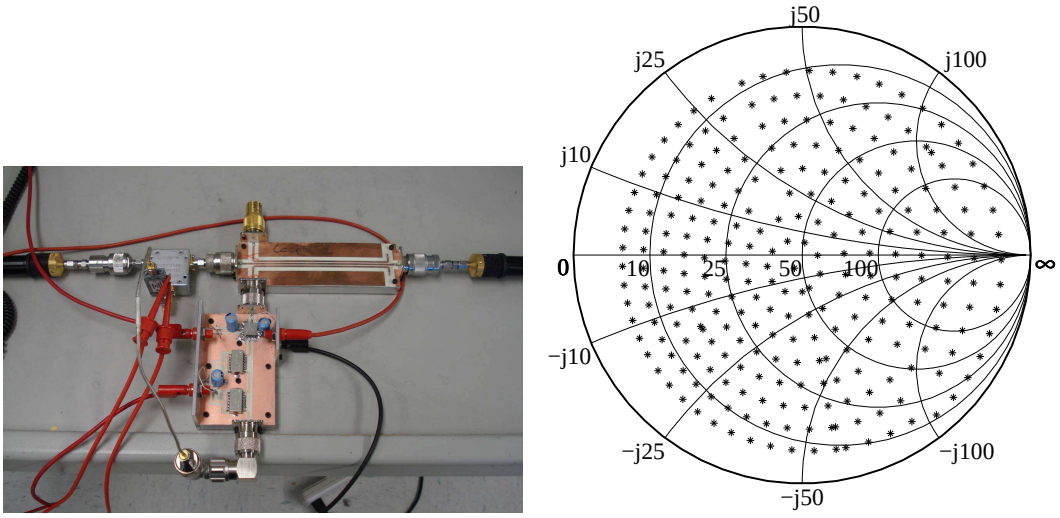


Figure 7.5: Diagram of an active load-pull setup. The DUT delivers power to the circulator. A sample of the power is coupled and controlled via a vector modulator before been amplified and injected back to the DUT via the circulator. Control of the amplitude and the phase of the injected wave mimics different Γ presented to the DUT.

perform this last task. A diagram of the active load-pull setup is shown in Figure 7.5. The DUT delivers power to the circulator. A sample of the power is coupled and controlled via a vector modulator before been amplified and injected back to the DUT, again via the circulator. Control of the amplitude and the phase of the injected wave mimics different Γ presented to the DUT. This particular setup can be calibrated because it only depends on the input wave. Some of the system details and assumptions are as follows:

- Circulator can handle the power level; output of the DUT plus the injected power.
- Circulator insertion loss does not vary with power or temperature.
- Infinite circulator isolation.
- The amplifier is linear with a constant phase as a function of input power.
- For a Γ=1, the linear amplifier is injecting the same amount of power than the one been generated by the DUT. This can be a problem when characterizing high-power devices.



(a) (b)

Figure 7.6: (a) Photograph of an implemented active load. The vector modulator is implemented with the RVA-2500 attenuator and two JSPHS-446 phase shifters (180°) from Minicircuits. (b) Measure active load contours.

- Γ can be larger than 1.
- For Γ=0.7 the active load injects half of the DUT output power.
- The system is calibrated with small-signal S-parameters in a network analyzer. The accuracy of the calibration is compromised as the DUT output power increases and as Γ increases.

Several active loads were implemented and one of them is shown in Figure 7.6(a). The vector modulator is implemented with the RVA-2500 attenuator and two JSPHS-446 phase shifters (180°) from Minicircuits. The active load contours are shown in Figure 7.6(b). The procedure for characterizing amplifiers via the active load-pull is as follows:

- Active load is characterized with small-signal in a network analyzer. The calibration is saved as a look-up-table to present desired impedance to the DUT.

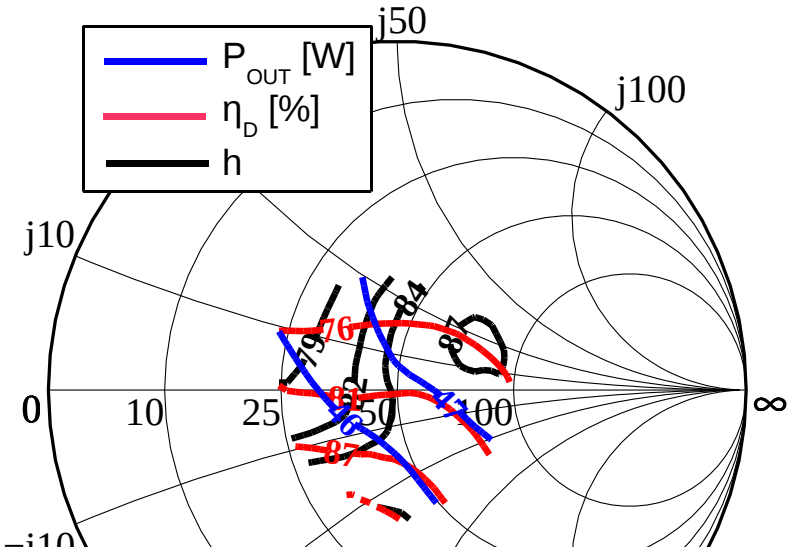


Figure 7.7: P_{OUT}, η_{D}, and $h_{\alpha=0.7}$ contours for the NPTB00050 measured with the active load for a supply voltage of 28 V.

- The calibrated impedances are presented to the DUT and performance is recorded.

Figure 7.7 shows P_{OUT}, η_{D}, and $h_{\alpha=0.7}$ contours in a 50 Ω for the NPTB00050 measured with the active load for a supply voltage of 28 V. Some of the problems encountered in the system are measurement of efficiencies higher than 100%, no linear amplifier with over 100 W output power was available at the time, and the large-signal behavior is approximated with small-signal S parameters. The system accuracy can improve with measurement of the forward and reverse waves. This can be accomplished via a coupler placed between the DUT and the circulator. A circuit that can compare amplitude and phase of these waves is also necessary. A circuit that can achieve this is the AD8302 from Analog Devices [77].

7.5 Future Work

Some of the topics that need to be address in the design of high-efficiency power amplifiers for linear transmitters are:

- How to deal with larger bandwidths in systems that implement dynamic biasing for signals such as WCDMA or signals that have not yet been developed but that the envelope exceeds the MHz range?
- How does predistortion can be used to improve linearity in polar systems?
- How does wide-bandgap transistors scale with power and frequency?
- How to efficiently combine several high-efficiency power amplifiers without significantly degrading performance?
- How to minimize package parasitic effects that limit higher frequency performance?
- How to maintain high-efficiency over broad bandwidths?

7.5.1 Outphased Assisted Polar Transmitter

A way to deal with the bandwidth and high PAR of signals such as WCDMA is with a system that combines outphasing and dynamic biasing. We are calling this system the Outphased Assisted Polar Transmitter. What is intended with this system is to combine the strength of polar transmitters with the strength of the outphasing architecture.

A summary of the properties of the outphasing architecture:

- Can deal with feedthrough;
- Sensitive to phase and amplitude unbalances;

- Needs 2 synchronized IQ channels;
- Needs 2 RFPAs;
- In constant load combiners the outphased power is dissipated. Can it be harvested?
- "Chireix" combiners can be used to efficiently combined the signals;
- Combiners losses cannot be avoided.

A summary of dynamic biasing is as follows:

- Scales the supply voltage to the desired output power;
- Problems due to feedthrough;
- Sensitive to time-alignment between envelope and phase;
- Only one IQ channel that needs to be synchronized with the envelope;
- Only one RFPA is needed;
- Performance depends on the bandwidth and the efficiency of the envelope tracker.

Outphasing can assist a polar transmitter by providing the bandwidth that the envelope tracker cannot supply; similar to the linear assisted envelope tracker. However, an advantage of combining techniques is that the system is redundant; only outphasing or only polar. The hybrid system can deal with feedthrough, and techniques such as optimal band-separation can be applied making the transmitter highly adaptable. The system implementation can be described as:

(1) Decomposed the amplitude and phase modulated signal into two components; amplitude and phase;

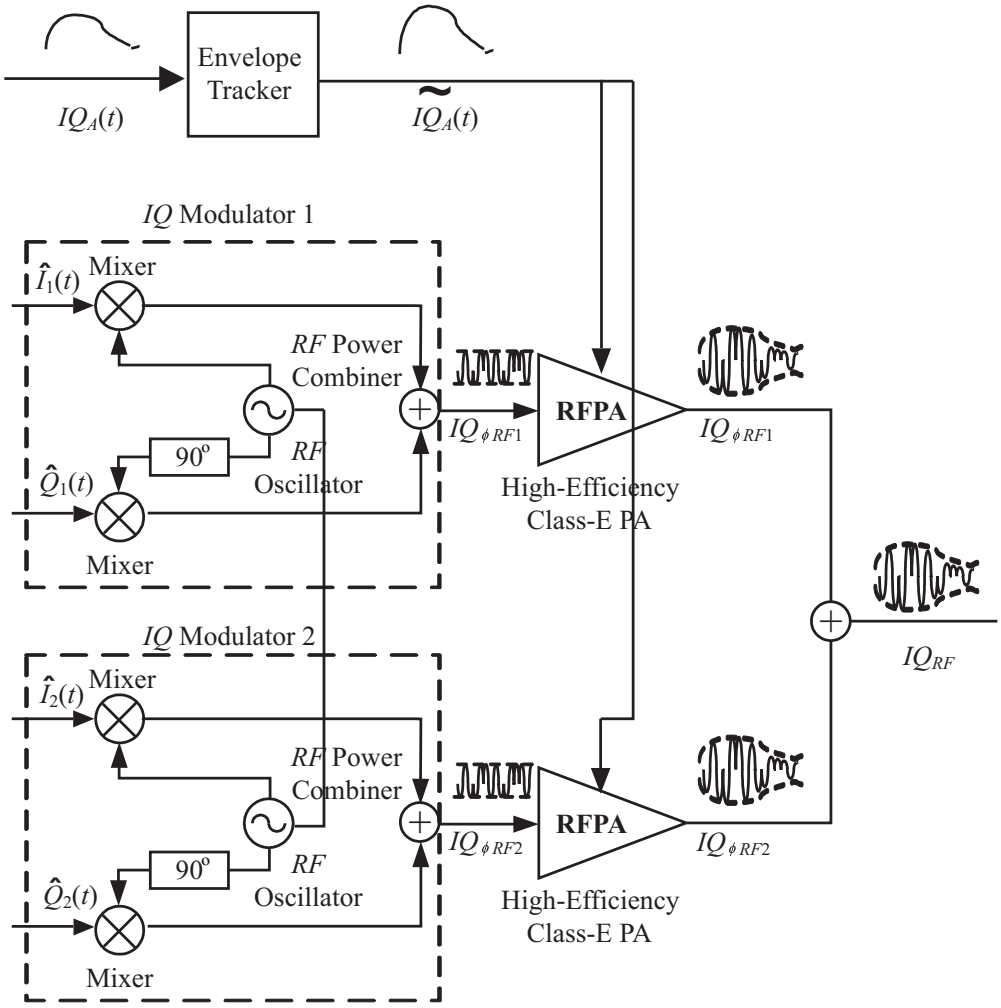


Figure 7.8: Diagram of the outphased assisted polar transmitter. The system combines the advantages of outphasing with the advantages of a polar transmitter making it highly adaptable.

(2) Lowpass filter the envelope with the bandwidth that the envelope tracker can supply;

(3) Recombine highpass envelope to the phase signal;

(4) Apply outphasing techniques to the remainder of the signal.

A diagram of such as system is shown in Figure 7.8. The system combines the advantages of outphasing architecture with the advantages of a polar transmitter making it highly adaptable. Mathematically the system is describes as follows,

$$IQ_{\mathrm{RF}} = IQ_{\mathrm{A}} \cdot IQ_{\phi} \tag{7.2}$$

where

$$IQ_{\phi} = e^{j\angle IQ_{\mathrm{RF}}} \tag{7.3}$$

$$IQ_{\mathrm{A}} = |IQ_{\mathrm{RF}}| \tag{7.4}$$

The envelope signal is decomposed into lowpass and highpass frequency components,

$$IQ_{\mathrm{A}} = IQ_{\mathrm{A\ LP}} + IQ_{\mathrm{A\ HP}} \tag{7.5}$$

The original signal can now be expressed as,

$$IQ_{\mathrm{RF}} = (IQ_{\mathrm{A\ LP}} + IQ_{\mathrm{A\ HP}}) \cdot IQ_{\phi} \tag{7.6}$$

$$= IQ_{\mathrm{A\ LP}} \cdot IQ_{\phi} + IQ_{\mathrm{A\ HP}} \cdot IQ_{\phi} \tag{7.7}$$

Because dynamic biasing can only multiply,

$$IQ_{\mathrm{RF}} = IQ_{\mathrm{A\ LP}} \left(IQ_{\phi} + IQ_{\phi} \cdot \frac{IQ_{\mathrm{A\ HP}}}{IQ_{\mathrm{A\ LP}}} \right) \tag{7.8}$$

and the outphasing component is then,

$$IQ_{\mathrm{outphasing}} = IQ_{\phi} \left(1 + \frac{IQ_{\mathrm{A\ HP}}}{IQ_{\mathrm{A\ LP}}} \right) \tag{7.9}$$

Because dynamic biasing can only multiply, there is a low frequency component ($IQ_{\mathrm{A\ LP}}$) in Equation 7.9. However as the tracking bandwidth of the envelope tracker increases the $\mathrm{IQ_{A\ HP}}/\mathrm{IQ_{A\ LP}}$ component goes to zero.

7.6 Summary

Digital modulation techniques used in wireless communications with radio frequency (RF) carriers can increase channel capacity, improve transmission quality, enhance security, and provide services not possible with analog modulation [1]. Improving spectral efficiency by allowing the envelope of the RF signal to vary with time can enhance channel capacity. Envelope variations require RFPA linearity. The power conversion efficiency of RFPAs operating in linear modes is limited to less than 25% for signals with high envelope variations. Poor conversion efficiency leads to significant dissipated power, and shortens the lifetime of battery operated equipment.

Polar transmitters can be used to linearize RFPAs to meet the spectral mask for signals such as EDGE without the use of pre-distortion. In these systems the baseband signal that contains, both amplitude and phase modulation is divided into two signals; one that contains just the amplitude modulation and one that contains the phase modulation with constant amplitude. The phase modulated signal is the RF input to an RFPA, while the envelope is supplied by an envelope tracker. The RFPA is able to reconstruct the signal due to its output voltage dependence to the supply voltage.

To maintain a high-overall efficiency it is necessary to use a high-efficiency envelope tracker and a high-efficiency RFPA. Switch-mode power supplies are suitable for envelope trackers, because they can achieve high-efficiencies, are small, light, economic and have the capability to step-up or step-down voltages. However, for these converters losses increase with switching frequency and it is a challenge to design fast high-efficiency SMPSs. SMPSs can be assisted with linear amplifiers to cover larger bandwidths. The class-E mode of operation lends itself well to the polar transmitter architecture because the output voltage across a constant load can be linearly varied by varying the supply voltage. A 56% efficient linear polar

transmitter with +20dBm of output power was designed and implemented for the EDGE modulation scheme. This is the highest efficiency reported to date for a polar EDGE transmitter.

The work presented in this thesis illustrates the design, implementation and performance of transmission line class-E power amplifiers at UHF and microwave frequencies. 60-W single device amplifiers with over 80% efficiency at 370 MHz were designed with transistor technologies such as GaN HEMTs, and SiC MESFETs. As these transistor technologies continue to mature with more power at higher frequencies, the techniques illustrated in this thesis can be directly applied to these future devices. For even higher power levels, low loss combining techniques need to be investigated.

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