A Fully Monolithically Integrated 4.6 GHz DC-DC Converter

Ignacio Ramos, Zoya Popović
Department of Electrical, Computer, and Energy Engineering
University of Colorado, Boulder, CO, 80309-0425
Email: ignacio.ramos@colorado.edu, zoya.popovic@colorado.edu

***Abstract*—This paper presents the design and measurement of a proof-of-concept fully monolithically integrated DC-DC converter operating at 4.6 GHz. The converter is designed in Qorvo's 0.15 μm GaN on SiC process and has a total area of 2.5 mm × 3.8 mm. The distributed class-E^2 converter does not use any external inductors or other lumped elements. The maximum efficiency achieved by the converter is 48 % at 0.6 W output power. The converter can also operate in self-synchronous mode without rectifier gate drive, albeit with a drop in performance.**

***Index Terms*—DC-DC converters, high efficiency power amplifiers, rectifiers, MMIC, integrated circuits, power supply on a chip (PwrSoC).**

I. Introduction

THE realization of an integrated power supply on a chip (PwrSoC), has been a research area of interest for a number of different applications [1]. Recently, there is an interest in increasing the frequency of converter operation in order to reduce the value and size of the passive components [2], [3]. Magnetics tend to be the biggest impediment for the integration of power supplies. Hence, the reduction or elimination of bulky magnetic components can lead to reduced size or even monolithic integration of power supplies [4].

In [5], a CMOS integrated converter switching at 233 MHz achieves 82 % efficiency at an output power of 0.55 W. The converter uses off-chip air-core inductors and covers an area of 1.28 mm x 0.990 mm. In [6], an integrated resonant boost converter designed using switches fabricated in a 50 V integrated power process and discrete components is demonstrated. The converter operates at 50 MHz with an efficiency better than 74 % at an output power of 17 W. More recently, a buck converter integrated with its drive circuitry was implemented on a 2.3 mm x 2.3 mm GaN chip in [7]. This converter switches at 100 MHz and achieved a maximum efficiency of 90 % at 9 W but requires a 47 nH off-chip inductor. More research related to the use of GaN in the development of high-frequency DC-DC converters has been shown in [8], [9], where class-E^2 converters operating at 780 MHz and approximately 1 GHz were demonstrated with efficiencies around 70 % and output powers around 10 W. However, these converters are not integrated and are approximately 5.6 cm × 6 cm in size and 3 mm thick.

In this paper, the design and characterization of a fully integrated class E^2 DC-DC converter is presented. The converter is implemented in Qorvo's 0.15 μm GaN on SiC process, operates at 4.6 GHz with an output power of approximately 1 W, and is a proof-of-concept demonstration of a fully monolithically integrated DC-DC converter. The MMIC is shown in Fig. 1.

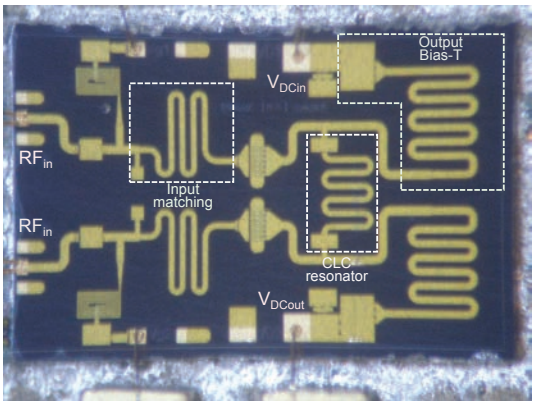

Fig. 1. Photograph of the monolithically integrated class-E^2 DC-DC converter. The total area of the die is 2.5 mm × 3.8 mm.

II. Design of Integrated Converter

The design of the converter is based on the topology presented in [10], which is a PA (inverter) reactively coupled to a synchronous rectifier. A switching frequency of approximately 4.6 GHz is chosen based on die size as well as voltage constraints imposed by the process. The typical characteristics of the process are I_{max}=1.15 A/mm, $g_{m,max}$= 380mS/mm, and 3.5 V pinch-off at V_{ds}=10 V. The breakdown voltage exceeds 50 V at I_{gd}=1 mA/mm. A non-linear model developed by Modelithics was used to extract the output capacitance of the transistors. The size of the transistors for both inverter and rectifier is 100 μm in gate width, with twelve gate fingers each. The intrinsic capacitances are estimated to be C_{gs}=1.4 pF, C_{ds}=0.36 pF, and C_{gd}=0.09 pF. The equivalent output capacitance of the transistor is therefore equal to 0.420 pF. The simulated I-V curves of the 12x100μm transistor are shown in Fig. 2. The slope of the red line is used to estimate the ON resistance $R_{ON} \approx 0.3\,\Omega$. As previously mentioned, the switching frequency has to be high enough for the distributed circuit to fit in a 2.5 mm x 3.8 mm die size but low enough to approximate class-E waveforms at the intrinsic drain of the transistor. An initial frequency range between 4.5-5 GHz was chosen as a starting point for the design. Using C_{ds}= 0.36 pF and 4.5 GHz, according to well known class-E theory the impedance that needs to be presented to the transistor for a class-E PA is approximately 19 + j21.14 Ω. For a class-E^2 converter, the reactances of the PA and the rectifier add as shown in [11], therefore the impedance to be presented to the transistor becomes 19 + j42 Ω.

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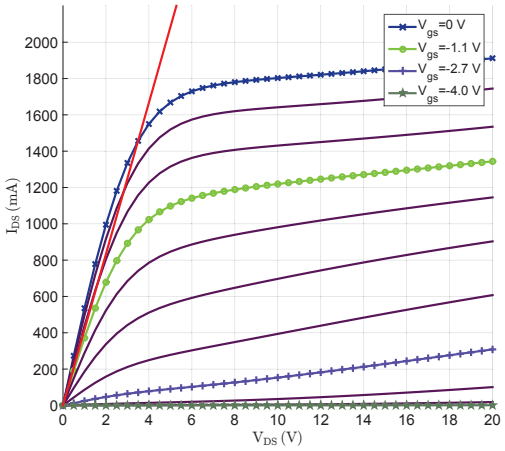

Fig. 2. Simulated I-V curves for the 12x100 μm transistor device used in the design of the distributed converter. The red line is used to estimate R_{ON}.

Because of the distributed nature of the circuit, it proves difficult to terminate both the 2nd and the 3rd harmonic simultaneously in an open circuit, thus priority is given to the termination of the 2nd harmonic. The two bias networks at the output are implemented with a meandered 48 μm line and a 24 pF shunt capacitor to ground, and are also part of the output matching network. The CLC resonator from [9] is implemented by a meandered line and two 5.7 pF capacitors. The bias-T and the resonator are used to approximately terminate the 2nd harmonic in an open circuit and to present the previously calculated impedance. The input matching network consists of a spiral inductor and a 30 pF capacitor shunt to ground for the bias-T, and a meandered transmission line with a 2.3 pF capacitor shunt to ground for appropriate matching.

III. Measurements with Synchronous Rectifier

The die from Fig. 1 is soldered to a 40-mil thick CuMo carrier plate. The RF inputs for both the power amplifier and the rectifier are connected to 50-Ω lines on an alumina substrate and bounded with two 1-mil gold bond wires each. The carrier plate is then inserted into an aluminum fixture that also serves as a heat sink for the circuit. The 50-Ω launchers that make contact with the lines are shown in Fig. 3. The DC gate and drain pads are connected with bondwires to a shunt 1000 pF capacitor, which is in turn connected through a bondwire to more accessible DC pads.

The converter is characterized using the setup shown in Fig. 4. The PA is biased at different quiescent currents for input voltages ranging from 5-20 V. The rectifier is biased at pinched-off with V_{gs}= -4.0 V. The DC load used for testing is a BK Precision 8500 electronic DC load in constant voltage mode. The output voltage is set by the electronic load and is swept from 1-15 V. All the measurements are performed with an input power of P_{in}= 22 dBm for both the PA and the rectifier. The phase of the signal driving the rectifier gate is

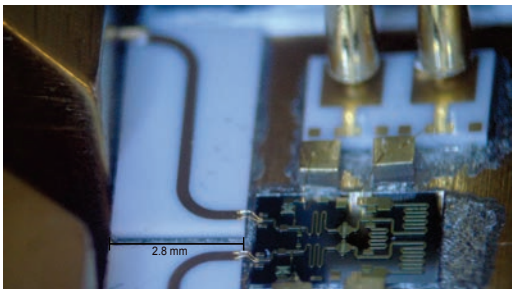

Fig. 3. Photograph of the fixture used to measure the class-E^2 MMIC. The two RF inputs are connected to the alumina lines via two bondwires. The center pin of the launchers is settled on the alumina line. The gate and drain DC pads are connected to a 1000 pF capacitor shunt to ground and then connected to DC pads for external pins (two cylinder on top) to make contact with.

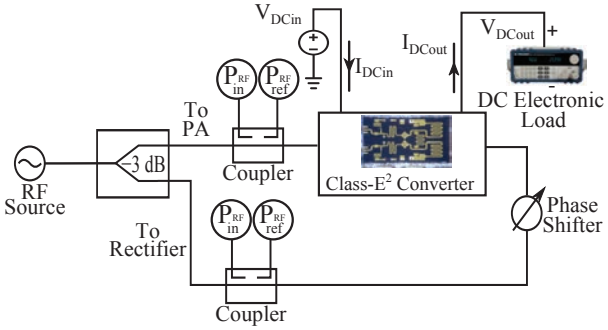

Fig. 4. Setup used to characterize the monolithically integrated class-E^2 converter. The RF source is split in two signals, one is driving the PA and the other one drives the rectifier. The incident and reflected power of the driving signal is measured using two couplers. The phase of the signal driving the rectifier is adjusted for synchronours operation. The output voltage is enforced by the electronic load.

adjusted until synchronous operation is achieved. Fig. 5 shows a summary of the performance of the converter. Output power and efficiency are plotted as a function of output voltage for different input voltages. The converter operates with output power proportional to input voltage as previously shown in [10]. Highest efficiency is achieved at lower input voltages with a a maximum of 48 % at an output power of 0.68 W. The maximum rectified power is 1.3 W for an input voltage of 18 V. The efficiency of the converter plotted in Fig. 5 is defined as

$$\eta_{DC} = \frac{V_{DCout} I_{DCout}}{V_{DCin} I_{DCin}} \quad (1)$$

IV. Self-synchronous operation

Eliminating both RF inputs is desirable, and operation in both self-synchronous mode and oscillating self-synchronous mode is demonstrated in [10] for a hybrid circuit. According to the analysis in [10], an impedance approximately equivalent to

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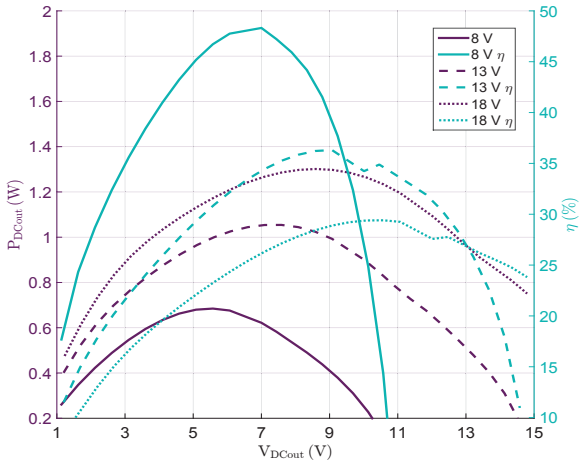

Fig. 5. Measured results of the integrated converter. Efficiency (cyan) is shown in the right y-axis and output power (purple) is shown in the left y-axis; both are plotted as a function of output voltage for an input voltage of 8, 13 and 18 V.

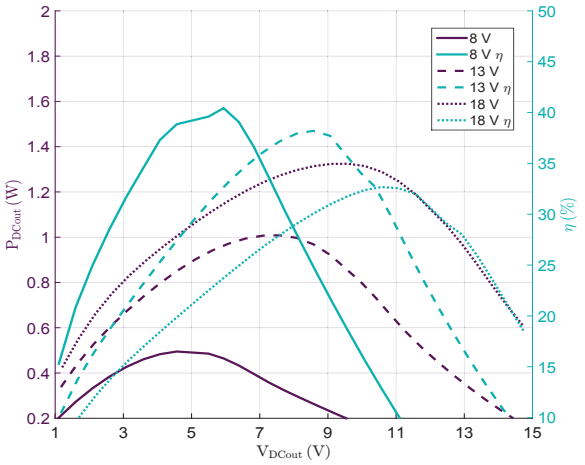

Fig. 6. Measured output power and efficiency of the integrated converter with the rectifier running self-synchronously. Efficiency (cyan) is shown in the right y-axis and output power (purple) is shown in the left y-axis; both are plotted as a function of output voltage for input voltages of 8, 13 and 18 V.

$$L_g = \frac{1}{(C_{gs} + C_{gd})\omega_s^2} = \frac{1}{(1.4\,\text{pF} + .088\,\text{pF})(2\pi 4.6\,\text{GHz})^2} = 0.8\,\text{nH} \quad (2)$$

has to be presented to the input of the transistor. However, due to matching to a 50 Ω connector, the alumina lines and the launchers used in the measurement of the MMIC converter, the impedances that can be presented to the transistor are limited to a small area on the Smith chart. After performing a manual load pull at the gate port of the rectifier, the converter is operated running the rectifier self-synchronously. Fig. 6 shows the measured results of the converter without a drive signal at the rectifier gate. The performance of the converter running self-synchronously undergoes a drop in both efficiency and output power. The performance degradation is likely due to the inability to reach the optimal value of the equivalent inductance from (2) externally.

V. Conclusion

A proof-of-concept fully integrated GaN MMIC DC-DC Converter switching at 4.6 GHz is demonstrated for the first time. The circuit uses two GaN HEMTs, one for the inverter (PA) and one for a synchronous rectifier. The 3.8 mm × 2.6 mm chip has two RF 50-Ω inputs, a DC input and a DC output, and does not require any external elements. By connecting an external RF tuner to the rectifier gate input, it is demonstrated that the converter can also operate in self-synchronous mode with a single RF input, but with lower efficiency. The efficiency can be increased in this mode of operation by including the appropriate impedance in the rectifier gate on-chip. The maximum end-to-end efficiency is 48 % and can be increased in this particular process by lowering the frequency of operation. It should be noted that the nonlinear device models do not accurately (or at all) predict device behavior for the dynamic load line in the 3rd quadrant of the IV characteristics, making the design only an approximate process since only the inverter (PA) can be simulated. Experiments are under way to demonstrate self-oscillating performance with no RF inputs, as well as investigation of possible methods to control the output voltage such as frequency modulation and pulsed RF operation.

Acknowledgment

This work was funded in part by the Office of Naval Research under the Defense Advanced Research Projects Agency (DARPA) Microscale Power Conversion (MPC) Program (N00014-11-1-0931), and in part by the Advanced Research Projects Agency-Energy (ARPAE), U.S. Department of Energy (DE-AR0000216). The authors would like to thank the sundown saloon and Avery brewery in Boulder CO for providing a prime environment for the

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