Monolithic Multilevel GaN Converter for Envelope Tracking in RF Power Amplifiers

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***Abstract*—This paper presents a monolithic multilevel converter realized in a depletion-mode GaN process and intended to operate as a drain supply modulator (DSM) for high efficiency radio-frequency (RF) power amplifiers (PAs). The custom prototype chip includes a four-level power stage with on-chip integrated gate drivers and damping networks designed to mitigate effects of parasitics during output voltage level transitions. An optimization algorithm is described to maximize the drain supply system efficiency using the level voltages and a minimum switching interval as optimization variables. The monolithic multilevel chip is used to construct a four-level converter prototype. Experimental results are presented for tracking 8 MHz sine-wave and 10 MHz LTE envelope signals. The converter output voltage exhibits fast and well damped level-to-level transients. For the 10 MHz LTE envelope signal, the converter achieves greater than 97.3% power stage efficiency at 3.5 W average output power level.**

I. Introduction

Modern radio-frequency (RF) communications systems require power amplifiers (PAs) to process signals with high bandwidth and high peak-to-average power ratio (PAPR), which adversely affects PA efficiency. Efficiency improvement techniques include approaches based on drain supply modulation (DSM) or envelope tracking (ET) [1], [2]. DSM-based systems improve the efficiency of RF transmitters by dynamically adjusting the drain supply voltage of the PA in response to the RF envelope signal. Drain supply modulators (DSMs), also referred to as envelope amplifiers, can be realized using linear power amplifiers (LPAs) [3], [4], single-phase or multi-phase switched-mode pulse-width modulated (PWM) converters [5]–[9], switched-mode assisted LPAs [10], or multilevel converters [11]–[13]. Switched-mode PWM DSMs operate at switching frequencies significantly higher than the RF envelope signal bandwidth and can offer the highest system efficiency, but are bandwidth-limited due to switching losses. A multilevel converter outputs discrete voltage levels, which are dynamically selected to be close in magnitude but always higher than the RF envelope, as shown in the simplified block diagram of Fig. 1. As a result, a multilevel converter can operate at frequencies comparable to or lower than the RF envelope signal bandwidth, and have potentials to offer better efficiency trade-offs in wide-bandwidth systems. Challenges in multilevel DSMs are associated with hard-switched transitions, which result in switching losses, and undesirable ringing due to parasitic capacitances and inductances in the path between the dc input supplies and the PA drain supply node. The objectives of this paper are to introduce a monolithic GaN multilevel converter realized as a custom chip in a high-performance depletion-mode GaN process, and to show how integration and design of the on-chip and off-chip interconnect networks result in high-frequency switching capabilities and mitigation of parasitic effects. Furthermore, an algorithm is proposed to optimize the level voltages and the minimum switching interval of a multilevel converter based on the envelope signal, in order to maximize the drain supply system efficiency. The paper is organized as follows. The multilevel converter circuit is described in Section II. The converter loss modeling and system efficiency are addressed in Section III. The system optimization algorithm is presented in Section IV. Experimental results for the prototype monolithic GaN multilevel converter are shown in Section V, while Section VI concludes the paper.

II. Monolithic GaN Four-Level Converter

A schematic of the GaN four-level converter chip is shown in Fig. 2. The power stage comprises four switches (transistors

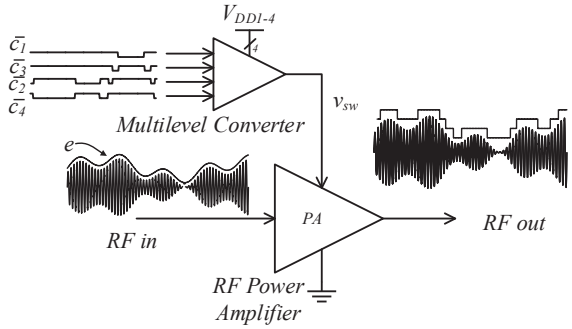

Figure 1: RF power amplifier with a multilevel converter used as an envelope-tracking drain supply modulator (DSM).

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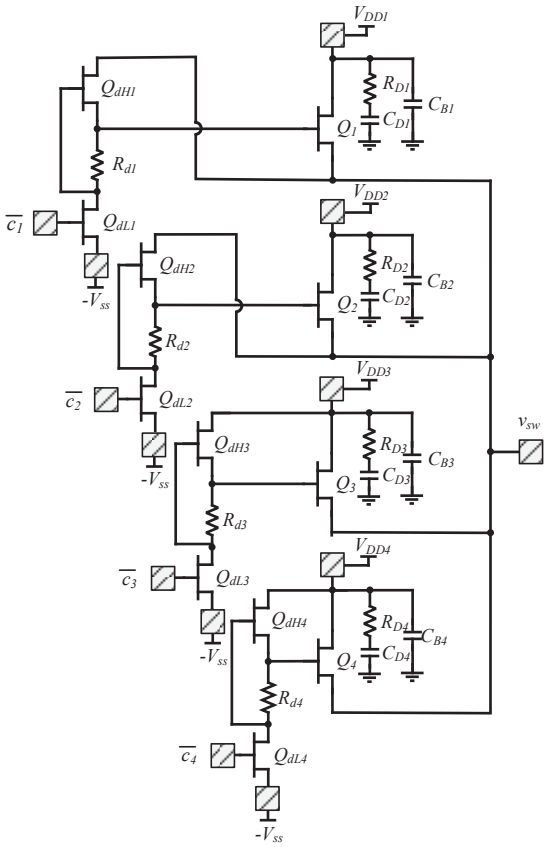


Figure 2: Circuit diagram of the monolithic GaN four-level converter with integrated gate drivers and damping networks.

Q_1 to Q_4), each connecting one of the four dc supply voltages V_{DDn} to the output node v_{sw}. The depletion-mode GaN process and the transistor gate-drivers are as described in [14]. For each power-stage transistor, the gate-drive stage is based on an active pull-up configuration comprising two transistors Q_{dH}, Q_{dL} and a resistor R_d. The inverting gate-driver circuit operates as follows: when the input control signal c_n is logic low, the corresponding power stage transistor Q_n is turned on, and when c_n is logic high, Q_n is turned off. The drains of the top two gate-driver transistors (Q_{dH1} and Q_{dH2}) are connected to the output switching node, following the modified active pull-up approach [14], while the bottom two gate-driver transistors (Q_{dH3} and Q_{dH4}) have their drains connected to their respective supply rails, corresponding to conventional active pull-up drivers [14]. This hybrid gate drive scheme reduces the overall quiescent power consumption. To better explain this, assume that the input dc supply voltage levels are arranged so that

$$V_{DD1} > V_{DD2} > V_{DD3} > V_{DD4}\,, \tag{1}$$

and also assume that the average output voltage is between levels V_{DD3} and V_{DD2},

$$V_{DD2} > v_{sw,avg} > V_{DD3}\,. \tag{2}$$

The drains of the top two gate-driver transistors Q_{dH1} and Q_{dH2}, corresponding to the voltage levels greater than the output average, are connected to the output voltage node v_{sw} in order to reduce the quiescent power consumption in the gate-drivers in level 1 and level 2. On the other hand, the drains of the bottom two gate-driver transistors Q_{dH3} and Q_{dH4} are connected to the respective dc supply voltages V_{DD3} and V_{DD4} to reduce the quiescent power consumption because these voltage levels are on average lower than the output voltage.

The converter generates up to four levels of output voltage v_{sw}, each uniquely corresponding to the on-state of one of the power-stage transistors. The switching of the four transistors is time-interleaved with appropriate dead times. Hence, only one of the power stage transistors is on at any time. Idealized time-aligned waveforms of the control inputs, output voltage levels and an RF envelope signal are shown in Fig. 3. The output voltage of the converter v_{sw}(t) is always higher than the RF envelope signal, in order to preserve linearity of the RFPA. One may note that the output voltage includes hard-switching level transitions which result in switching losses, and are prone to undesirable ringing due to parasitic capacitances and inductances in the path between the dc supply voltages and the output. To mitigate these effects, an on-chip damping circuitry, consisting of a resistor R_{Dn} and a capacitor C_{Dn} is connected to the drain of each transistor in parallel with a supply decoupling capacitor C_{Bn}.

An equivalent circuit in the on-state of one of the switches ($n = 1 - 4$) is shown in Fig. 4, including the dc power supply voltage (V_{DDn}), the damping circuit (R_{Dn} and C_{Dn}), the bypass capacitor (C_{Bn}), and the power-stage transistor on-resistance (R_{dsn}). The PA that loads the multilevel converter is modeled by its equivalent resistance (R_{PA}) in parallel with the drain decoupling capacitance C_{sw}.

After a level-to-level transition, the output voltage of the

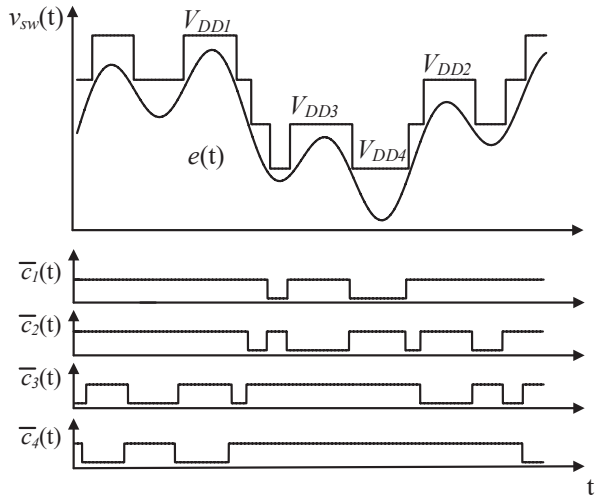


Figure 3: Idealized multilevel converter output voltage v_{sw}(t) and the controls signals c_1(t) to c_4(t) for an envelope signal e(t).

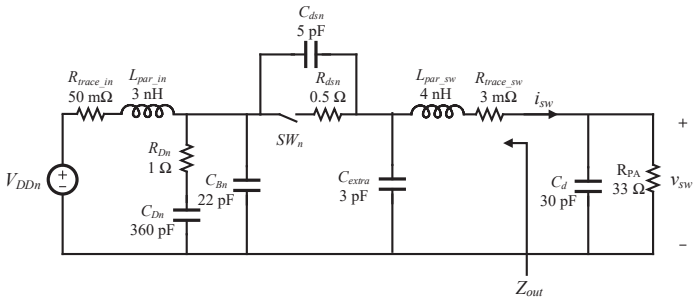
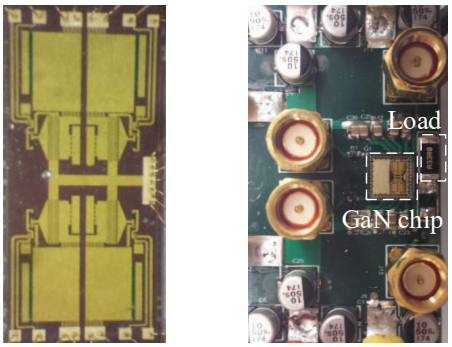


Figure 4: An equivalent circuit model of one stage in the multilevel converter, including on-chip damping and decoupling components, and off-chip parasitics.



(a) (b)

Figure 5: (a) GaN four-level converter die photograph 2.6mm × 5.4mm, and (b) photograph of the four-level converter prototype, with the GaN converter chip in a 7mm × 7mm QFN package.

converter is given by:

$$v_{sw} = V_{DDn} - (R_{trace\_in} + R_{dsn} + R_{trace\_sw})i_{sw}\,. \quad (3)$$

The majority of the voltage drop and the corresponding conduction loss are associated with the switch on-resistance R_{dsn}. To prevent distortions arising from the v_{sw} transitions and the high-frequency content in the RF envelope signal, it is necessary to damp and filter the switching transitions and to ensure that the output impedance of the multilevel converter be sufficiently low. The output impedance can be derived from the equivalent circuit shown in Fig. 4. The bypass capacitor C_{Bn} is relatively large, lowering the converter's output impedance. However, the bypass capacitor tends to resonate with the parasitic inductances present in the converter circuit. To mitigate this issue, the bypass capacitor and the damping circuit are integrated with the power stage transistors on the same die. A photograph of the prototype chip die is shown in Fig. 5(a). The bypass capacitor and damping circuit are placed very close to the power switch transistors to minimize interconnect inductances. For effective damping, the value of the damping circuit capacitor needs to be larger than the bypass capacitor C_{Bn} [15]. The magnitude of the multilevel output impedance

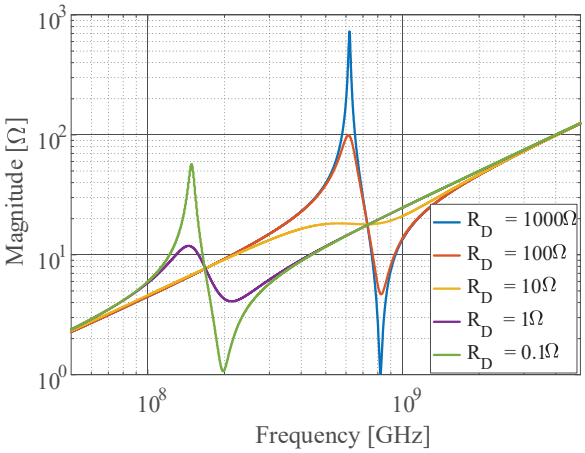


Figure 6: Magnitude of the multilevel converter output impedance $||Z_{out}||$ for different damping resistances R_D.

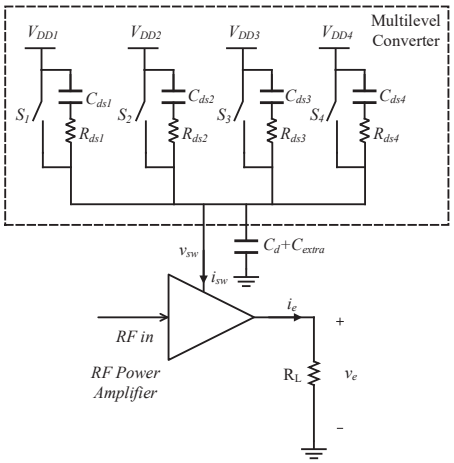


Figure 7: A circuit model used for the multilevel converter loss modeling.

$||Z_{out}||$ (in Fig. 4) is shown for different damping resistances R_D. The chip includes $R_D = 1\ \Omega$ that provides adequate damping of the resonances in a wide range of frequencies.

III. Loss Modeling and System Efficiency

In an ideal envelope-tracking system, the RFPA is designed to operate close to saturation, with supply voltage very close to the minimum required to reproduce the required RF envelope without distortion [1], [2]. In a system with a multi-level converter, the PA supply voltage is higher than the ideal minimum, which means that the PA operates further away from saturation. As a result, PA losses are higher compared to the PA in an ideal ET system. On the other hand, since the levels do not necessarily need to be switched very often, the switching losses in the multilevel converter can be much reduced, and the multilevel converter efficiency can be significantly higher compared to an ET supply that would be required to continuously track a high-bandwidth signal envelope. Hence, there is an optimum selection of the switching pattern in a multilevel converter to maximize the drain supply efficiency

for a given RF signal envelope. Loss modeling and system efficiency considerations are presented in this section, as an introduction to a system efficiency optimization approach described in Section IV.

A. Multilevel converter loss modeling

A loss model for the multilevel converter is developed with reference to Fig. 7. Each stage of the multilevel converter is modeled as an ideal switch S_n in series with the switch on resistance $R_{ds,n}$, with a transistor output capacitance C_{dsn} connected in parallel. Expressions for power losses are derived considering an RF signal segment over a time interval T.

The conduction loss is given by:

$$P_{cond} = \frac{1}{T}\int_0^T R_{ds} i_{sw}(t)^2 dt\,, \tag{4}$$

where $i_{sw}(t)$ equals the drain supply current for the RFPA. In general, $i_{sw}(t)$ depends on the RF signal characteristics and the RFPA design details.

The switching loss associate with hard-switching transitions that involve charging and discharging of capacitances connected to output v_{sw} can be expressed as:

$$P_{sw} = \frac{\sum_1^m \frac{1}{2} C_{sw} \Delta V_{sw,m}^2}{T}\,, \tag{5}$$

where m is the total number of level transitions over the signal segment interval T, $\Delta v_{sw,m} = V_{sw,m} - V_{sw,m-1}$ is the voltage difference between two levels at each transition, and C_{sw} is the total output-node capacitance,

$$C_{sw} = C_d + C_{extra} + \sum_{n=1}^{4} C_{dsn}\,, \tag{6}$$

where C_d is the PA drain decoupling capacitor, C_{dsn} is the output capacitance of each power stage transistor, and C_{extra} is the total package and PCB parasitic capacitance [6].

Gate driver losses are estimated following the approach described in [14]. The loss associated with charging and discharging the gate of the power stage device Q_n is

$$P_{d,\mathrm{Q_n}} = C_{gs,\mathrm{n}} V_g^2 \ \frac{m_n}{T}\,, \tag{7}$$

where m_n is the total number of switching events of stage n, $C_{gs,\mathrm{Q1}}$ is the charge-equivalent gate-to-source capacitance of Q_n, and V_g is the gate-drive voltage swing (5 V). The driver transistor $Q_{dH,n}$ is hard switching, and the loss associated with its equivalent output capacitance differs for the two types of gate drivers in the multilevel converter. For the two top levels (level 1 and level 2), the loss is given by

$$P_{d,\mathrm{Q_{dL}}} = \frac{1}{T}\int_0^T C_{ds,dL}(V_{ss} + v_{sw})^2 \ dt\,, \tag{8}$$

and for the two bottom levels (level 3 and level 4), the loss is

$$P_{d,\mathrm{Q_{dL}}} = C_{ds,dL}(V_{ss} + V_{DDn})^2 \ \frac{m_n}{T}\,. \tag{9}$$

Referring to Fig. 2, the low-side driver transistor $Q_{dL,n}$ is operating either fully off, fully on, or in the active region, conducting bias current $I_{Q_{dH}}$. The switching loss associated with Q_{dL} is given by

$$P_{d,\mathrm{Q_{dH}}} = \underbrace{C_{gs,dH}(I_{Q_{dH}} R_d)^2 \ \frac{m_n}{T}}_{C\text{gs loss}} + \underbrace{C_{ds,dL} V_g^2 \ \frac{m_n}{T}}_{C\text{ds loss}} + \underbrace{\frac{2}{3} I_{Q_{dH}} V_g t_0 \frac{m_n}{T}}_{\text{transition loss}}\,, \tag{10}$$

where $t_0 = 200$ ps and is the transition time it takes for the transistor to move from the active region into fully on, or fully off region during a switching event. $I_{Q_{dH}} = 6$ mA is the gate driver DC bias current. Quiescent power loss for the two top gate drivers (level 1 and level 2) is given by:

$$P_{d,\mathrm{cond}} = \frac{1}{T}\int_0^T (v_{sw}(t) + V_{ss})\, I_{QdH} \ dt\,, \tag{11}$$

while for the lower gate drivers (Level 3, and level 4) the quiescent power consumption is expressed as:

$$P_{d,\mathrm{cond}} = (V_{DDn} + V_{ss})\, I_{QdH} \frac{T_{cond}}{T}\,, \tag{12}$$

where T_{cond} is the total time the gate driver transistor Q_{dL} is on (the corresponding power stage transistor Q_n is off). The total gate driver loss is given by:

$$P_d = \sum_{n=1}^{4} P_{d,\mathrm{Q_n}} + P_{d,\mathrm{Q_{dHn}}} + P_{d,\mathrm{Q_{dLn}}} + P_{d,\mathrm{condn}}\,, \tag{13}$$

and the overall multilevel converter efficiency can be found as:

$$\eta_{multilevel} = \frac{P_{sw}}{P_{sw} + (P_{cond} + P_{sw} + P_d)}\,, \tag{14}$$

where P_{sw} is the converter average output power, i.e. the power delivered to the PA,

$$P_{sw} = \frac{1}{T}\int_0^T v_{sw} i_{sw} \ dt\,. \tag{15}$$

B. System efficiency

The overall system efficiency η can be defined as a product of three efficiencies,

$$\eta = \eta_{multilevel} \times \eta_{ov} \times \eta_{PA}\,, \tag{16}$$

where $\eta_{multilevel}$ can be calculated as in (14), while the "over-voltage" efficiency η_{ov} corresponds to the power losses associated with the fact that the drain supply voltage v_{sw} produced by the multilevel converter must be greater than the ideally minimum voltage v_e required by the PA to produce the output RF signal without distortion. Finally, the RFPA efficiency η_{PA} depends on the RFPA design details, which is outside the scope of this paper.

The over-voltage efficiency can be found as a ratio of the idealized PA output power

$$P_e = \frac{1}{T}\int_0^T v_e \ i_{sw} \ dt\,, \tag{17}$$

and the output power P_{sw} of the multilevel converter,

$$\eta_{ov} = \frac{P_e}{P_{sw}} \,. \tag{18}$$

Note that η_{ov} depends on how far the multilevel output voltage v_{sw} is from the minimum supply voltage v_e required by the PA. For a given RFPA, and a given signal, the multilevel system efficiency optimization amounts to maximizing the drain supply efficiency η_{dsm} defined as the product of the multilevel converter efficiency, and the over-voltage efficiency,

$$\eta_{dsm} = \eta_{multilevel} \times \eta_{ov} \,. \tag{19}$$

IV. Multilevel System Optimization

The drain supply efficiency η_{dsm} defined by (19) can be maximized for any given envelope signal by selecting the optimum voltage levels V_{DDn}, and a switching pattern between the levels. The voltage levels and the switching pattern must meet the requirement that at any point in time

$$v_{sw} \geq v_e(t) + \Delta V \,, \tag{20}$$

where $v_e(t)$ is the minimum supply voltage required by the PA, and ΔV provides a safety margin. For a given signal, i.e. for a given $v_e(t)$ waveform, an appropriate switching pattern can be constructed by choosing the minimum level $v_{sw} = V_{DDn}$ that meets (20) over a switching time interval T_{sw}. The time interval T_{sw} represents the minimum switching interval for the multilevel converter. The voltage levels and the minimum switching interval T_{sw} are directly related to the system efficiency. For instance, increasing the number of output voltage levels and decreasing T_{sw} degrades the efficiency $\eta_{multilevel}$ of the multilevel converter while improving the over-voltage efficiency η_{ov}. This represents a trade-off, and hence an opportunity to optimize the number and magnitude of the output voltage levels and T_{sw} to maximize the overall drain supply system efficiency η_{dsm}.

A simple optimization procedure is described here where the voltage levels V_{DDn} and T_{sw} comprise a set of optimization variables to be determined in order to maximize the drain supply efficiency η_{dsm} for a signal given over a time segment T. One may note that efficiency calculation depends not only on the envelope signal $v_e(t)$ characteristics, but also on the drain supply current $i_{sw}(t)$ taken by the PA. The drain supply current, in turn, depends on the PA design details. In the optimization examples considered in this paper, it is assumed that the PA presents a resistive load R_{PA} at the drain, and $i_{sw} = v_e/R_{PA}$. Furthermore, the optimization is performed for the four-level converter prototype.

Given $v_e(t)$ over a signal segment interval T, the highest voltage level V_{DD1} (referring to Fig. 2) is set to meet the requirement (20)

$$V_{DD1} = v_{e,max} + \Delta V \,, \tag{21}$$

where $v_{e,max}$ represents the maximum of $v_e(t)$, and $\Delta V = 1\ V$ provides a margin to ensure the PA's output signal fidelity. Then, voltage levels V_{DD2}, V_{DD3}, V_{DD4} and the minimum switching interval T_{sw} are swept in nested loops and used to calculate the drain supply system efficiency (19). An exhaustive search for the optimization variables that maximize η_{dsm} is performed, with increments being $\Delta v = 1$ V for voltage levels, and $\Delta T_{sw} = 5$ ns for the minimum switching time T_{sw}. In the loops, the voltage levels are constrained to always meet (1) and (20).

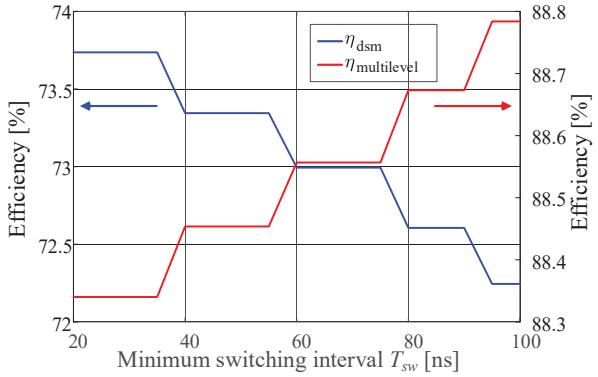


Figure 8: Drain supply system efficiency η_{dsm} and multilevel converter efficiency $\eta_{multilevel}$ as functions of the minimum switching interval T_{sw} for a 10 MHz LTE signal.

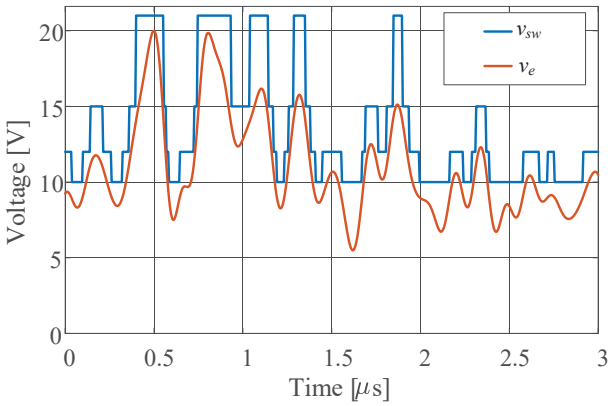
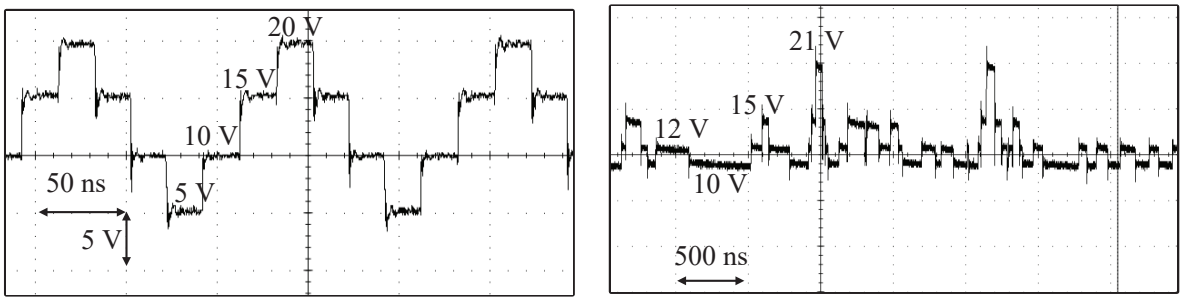


Figure 9: The output voltage $v_{sw}(t)$ of the multilevel converter optimized for a 10 MHz LTE envelope signal $v_e(t)$.

As an example, Fig. 8 shows the resulting optimized efficiencies as functions of the minimum switching interval T_{sw} for a 10 MHz LTE signal. It is shown how the multilevel converter efficiency increases as T_{sw} is increased, as expected. However, higher T_{sw} results in reduced over-voltage and overall drain supply efficiencies. As a result, the best drain supply system efficiency is obtained as T_{sw} is reduced. However, as T_{sw} of the multilevel converter is reduced below 37 ns no further improvements can be observed due to the fact that the number of voltage levels is limited to 4, and there are no further changes in the resulting v_{sw} waveform. Fig. 9 shows the converter output voltage v_{sw} overlaid with the 10 MHz LTE signal for the optimized voltage levels and $T_{sw} = 5$ ns.

Table I: Optimization results for different envelope signals.

Envelope	T_{sw}	$f_{sw,avg}$	V_{DD1}	V_{DD2}	V_{DD3}	V_{DD4}	$V_{e,max}$	$V_{e,min}$	$\eta_{multilevel}$	η_{ov}	η_{dsm}
10 MHz LTE	35 ns	9.65 MHz	21 V	15 V	12 V	10 V	20 V	4.9 V	88.2%	83.3%	73.5%
20 MHz LTE	25 ns	18.30 MHz	21 V	15 V	12 V	10 V	20 V	4.9 V	88.2%	82.8%	73.0%



(a) (b)

Figure 10: The output voltage v_{sw} of the multilevel converter prototype for (a) 8 MHz sine-wave envelope signal and (b) 10 MHz LTE envelope signal.

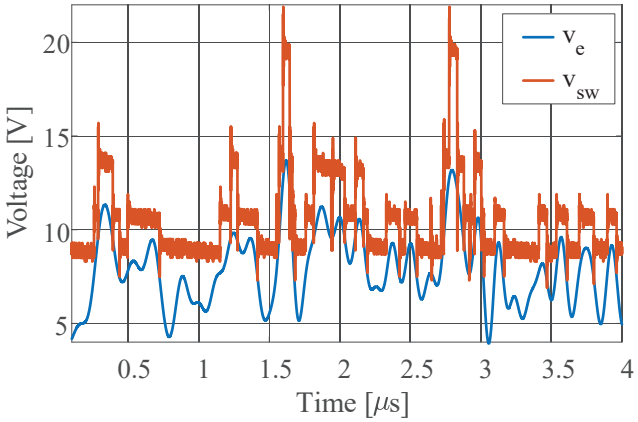


Figure 11: Output voltage v_{sw} of the multilevel converter prototype overlaid with a 10 MHz LTE envelope signal.

The optimized converter minimum switching interval T_{sw}, the voltage levels, and the corresponding efficiencies are given for 10 MHz and 20 MHz LTE signals in Table I. The average switching frequency for a multilevel converter is defined as:

$$f_{sw,avg} = \frac{m}{T}, \tag{22}$$

where m is the total number of switching events during the signal segment of length T. One may note that on average the optimized multilevel switching frequency is comparable to the envelope signal bandwidth in these examples. The multilevel efficiency includes gate-driver losses, which are significant, mainly due to quiescent bias current in the gate drivers. Excluding gate-driver losses, the multilevel power-stage efficiencies are above 98%. While the overall drain supply efficiencies are somewhat lower compared to some of the recently reported switched-mode PWM envelope tracking supplies for comparable signals [6], [9], [16]–[18], the multilevel approach would be easier to extend to very wide bandwidth systems.

V. Experimental Results

Using the chip shown in Fig. 5(a) in a QFN package, a prototype of the multilevel converter is designed and built as shown in Fig. 5(b). In order to reduce the bond wire inductance at the output node (v_{sw}) of the converter, the die is placed toward a side of the QFN package. In addition, multiple bond wires are used in parallel to further reduce the inductance. The converter chip is mounted on a four-layer test PCB, which is designed using the high-frequency layout techniques described in [6]. Low ESR ceramics capacitors from American Technical Ceramic are used as off-chip decoupling capacitors in the test circuit. The control signals (c_1 to c_4 in Fig. 2) are obtained from an Altera Stratix IV FPGA, which provides 125 ps resolution. A simple level-shifter interfaces the FPGA with the integrated gate driver inputs. For the purpose of this experiment, four bench power supplies are used to provide the input voltages V_{DD1} to V_{DD4}. In practice, the input voltages can be supplied from a single DC-DC converter with multiple outputs. This DC-DC converter provides fixed dc voltage levels and hence can be designed for very high efficiency.

Two sets of experiments are carried out to demonstrate the performance of the monolithic four-level converter for different RF envelope signals. A resistor, $R_{PA} = 33\ \Omega$, is used as the load, representing the drain impedance of a PA. The output voltage v_{sw} for an 8 MHz sine-wave envelope signal is shown in Fig. 10(a). The converter provides four different voltage levels: 5 V, 10 V, 15 V and 20 V, with a minimum switching interval of $T_{sw} = 5$ ns.

The output of the converter for a 10 MHz LTE envelope signal is shown in Fig. 10(b). For this signal, the converter generates output voltage levels of 10 V, 12 V, 15 V and 21 V. The converter achieves greater than 97.3% power

stage efficiency and 87.5% overall efficiency (including the gate-driver losses) at 3.5 W average output power level. In both experiments, the output voltage shows quick level-to-level transitions with relatively small ringing. The converter measured output voltage v_{sw} overlaid with the 10 MHz LTE envelope signal is shown in Fig. 11.

VI. Conclusions

This paper presents a monolithic GaN multilevel converter, which is used as an envelope tracking drain supply modulator for high efficiency radio-frequency (RF) power amplifiers (PA). The prototype chip is a four-level converter with on-chip integrated gate drivers and damping networks designed to mitigate effects of parasitics during level transitions. The chip is used in a four level converter prototype operating from up to 50 V, where high-frequency printed-circuit board (PCB) design techniques are employed to minimize the parasitics. An optimization procedure is developed to select the output voltage levels and the minimum switching interval of a multilevel converter to maximize the system efficiency. Experimental results are presented for the cases when the four-level converter is tracking 8 MHz sine-wave and 10 MHz LTE envelope signals. The output voltage of the converter exhibits fast level-to-level transients with minimal ringing.

References

[1] P. Asbeck and Z. Popovic, "ET Comes of Age: Envelope Tracking for Higher-Efficiency Power Amplifiers," *IEEE Trans. Microw. Mag.*, vol. 17, no. 3, pp. 16–25, Mar. 2016.

[2] J. Hoversten, S. Schafer, M. Roberg, M. Norris, D. Maksimovic, and Z. Popovic, "Codesign of PA, Supply, and Signal Processing for Linear Supply-Modulated RF Transmitters," *IEEE Trans. Microw. Theory and Tech.*, vol. 60, no. 6, pp. 2010–2020, Jun 2012.

[3] D. Li, M. Rodriguez, A. Zai, D. Sardin, D. Maksimovic, and Z. Popovic, "RFPA Supply Modulator Using Wide-Bandwidth Linear Amplifier with a GaN HEMT Output Stage," in *Proc. IEEE 14th Workshop on Control and Modeling for Power Electron,*, 2013, pp. 1–6.

[4] P. Theilmann, J. Yan, C. Vu, J.-S. Moon, H. Moyer, and D. Kimball, "A 60MHz Bandwidth High Efficiency X-Band Envelope Tracking Power Amplifier," in *Proc IEEE Compound Semicond. Integr. Circuit Symp*, 2013, pp. 1–4.

[5] M. Norris and D. Maksimovic, "10 MHz Large Signal Bandwidth, 95% Efficient Power Supply for 3G-4G Cell Phone Base Stations," in *Proc. IEEE 27th Annu. Appl. Power Electron. Conf. Expo.*, 2012, pp. 7–13.

[6] M. Rodriguez, Y. Zhang, and D. Maksimovic, "High-Frequency PWM Buck Converters Using GaN-on-SiC HEMTs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2462–2473, May. 2014.

[7] Y.-P. Hong, K. Mukai, H. Gheidi, S. Shinjo, and P. Asbeck, "High efficiency GaN switching converter IC with bootstrap driver for envelope tracking applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2013, pp. 353–356.

[8] S. Shinjo, Y.-P. Hong, H. Gheidi, D. Kimball, and P. Asbeck, "High speed, High Analog Bandwidth Buck Converter Using GaN HEMTs for Envelope Rracking Power Amplifier Applications," in *Proc. IEEE Wireless Sensors and Sensor Networks*, 2013, pp. 13–15.

[9] Y. Zhang, M. Rodriguez, and D. Maksimovic, "100 MHz, 20 V, 90% Efficient Synchronous Buck Converter With Integrated Gate Driver," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sept 2014, pp. 3664–3671.

[10] C. Hsia, A. Zhu, J. Yan, P. Draxler, D. Kimball, S. Lanfranco, and P. Asbeck, "Digitally Assisted Dual-Switch High-Efficiency Envelope Amplifier for Envelope-Tracking Base-Station Power Amplifiers," *IEEE Trans. Microw. Theory and Tech.*, vol. 59, no. 11, pp. 2943–2952, Nov. 2011.

[11] M. Vasic, P. Cheng, O. Garcia, J. Oliver, P. Alou, J. Cobos, D. Tena, and F. Ortega-Gonzalez, "The Design of a Multilevel Envelope Tracking Amplifier Based on a Multiphase Buck Converter," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4611–4627, Jun. 2016.

[12] D. Diaz, M. Vasic, O. Garcia, J. Oliver, P. Alou, R. Prieto, and J. Cobos, "Three-Level Cell Topology for a Multilevel Power Supply to Achieve High Efficiency Envelope Amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers,*, vol. 59, no. 9, pp. 2147–2160, Sep. 2012.

[13] M. Rodriguez, P. Miaja, A. Rodriguez, and J. Sebastian, "Multilevel Converter for Envelope Tracking in RF Power Amplifiers," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sept 2009, pp. 503–510.

[14] Y. Zhang, M. Rodriguez, and D. Maksimovic, "Very High Frequency PWM Buck Converters Using Monolithic GaN Half-Bridge Power Stages with Integrated Gate Drivers," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1–1, 2016.

[15] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer, 2001.

[16] Y. Zhang, J. Strydom, M. de Rooij, and D. Maksimovic, "Envelope tracking GaN power supply for 4G cell phone base stations," in *Proc. IEEE 31th Annu. Appl. Power Electron. Conf. Expo.*, 2016, pp. 2292–2297.

[17] D. Maksimovic, Y. Zhang, and M. Rodriguez, "Monolithic very high frequency GaN switched-mode power converters," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2015, pp. 1–4.

[18] Y. Zhang, M. Rodriguez, and D. Maksimovic, "Output filter design in high-efficiency wide-bandwidth multi-phase buck envelope amplifiers," in *Proc. IEEE 30th Annu. Appl. Power Electron. Conf. Expo*, 2015, pp. 2026–2032.