Design and Characterization of Low Phase Noise Microwave Circuits

by

Jason Breitbarth

B.S. Electrical Engineering, Oregon State University, 1997

M.S., Electrical Engineering, University of Colorado, 2001

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written by Jason Breitbarth
has been approved for the Department of Electrical and Computer Engineering

Prof. Zoya Popović

Dr. Kipp Schoen

Date

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Breitbarth, Jason (Ph.D., Electrical Engineering)

Design and Characterization of Low Phase Noise Microwave Circuits

Thesis directed by Professor Prof. Zoya Popović

This thesis addresses the short term stability, expressed as phase noise, of a variety of microwave circuits relevant to communication and radar systems. In specific, the following types of circuits are discussed in detail: (1) low-phase noise fundamental-frequency oscillators for carrier signal generation; (2) high-efficiency amplifiers with low additive phase noise for carrier amplification; and (3) harmonic generators with ultra-low phase noise using varactor nonlinear transmission lines (NLTLs).

A low phase noise 4.6-GHz local oscillator design is applied to a Cesium miniature atomic clock. The design is based on a micro-coaxial resonator and silicon bipolar transistor. The goal of this work is to determine the tradeoff between low DC power consumption, size (volume) and low phase noise at small deviations from the carrier. To that end, a smaller than 0.2 cubic centimeter varactor-tuned oscillator that consumes 16mW of DC power with a phase noise of -102dBc/Hz at 10kHz from the carrier is developed.

When amplifying a clean oscillator in a transmitter, the noise added by the amplifier close to the carrier frequency is relevant. This thesis analyzes additive phase noise in several high-efficiency X-band power amplifiers based on different device technologies and compares it to the equivalent linear power amplifier. It is shown that highly-efficient PAs have on the order of 10-20dB higher phase noise between 100Hz and 10kHz as compared to the linear PA.

Often it is more desirable to multiply a clean lower frequency oscillator in order to achieve higher frequency generation. Step recovery diodes exhibit additive noise greater than the oscillator reference, degrading overall performance. The main contri-

bution of this thesis is design and characterization of NLTLs as low-phase noise frequency converters. Additive phase noise measurements at the fundamental and 10th harmonics demonstrate true 20logN multiplication with an input referred phase noise of -182dBc/Hz. The work has demonstrated, both theoretically and in measurement, that NLTLs exhibit ultra-low phase noise as high-order frequency multipliers.

Dedication

This thesis is dedicated to my family for their years of love and support.

Acknowledgements

Professionally, I thank Picosecond Pulse Labs for their tremendous support and providing guidance towards an excellent thesis topic. In particular, discussions with Dr. Kipp Schoen gave valuable insight to the device physics of semiconductor devices.

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Personally, I thank my wife, Cindy, for her unwavering love and support through the past three years. My parents, Rob and Vicki, and sister, Jennifer, for their love and continual support. My two dogs, Basil and Guinness for their companionship through the writing of this thesis. Last, but certainly not least, thank you to all my friends who were always available for a pint of beer.

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Chapter 1

Introduction and Background

1.1 Introduction

Every microwave system, whether communication or radar, requires a signal source at the carrier frequency. The generation can be accomplished either directly at the carrier or by frequency multiplication from a low-phase noise source. In either case, stability and spectral purity of the source determines the main properties of the system, such as sensitivity, range, capacity and bandwidth. Amplification is usually required and the amplification characteristics can substantially influence the transmitted signal quality.

The work presented in this thesis covers three related topics, illustrated in Fig. 1.1. First, the design of a low-power voltage controlled oscillator (VCO) for use as the local oscillator in chip scale atomic clocks (CSAC). Second, the spectral performance of high-efficiency class-E X-Band power amplifiers (PA) is evaluated for use in signal sources. Third, nonlinear transmission lines (NLTLs) are designed and characterized for the purpose of ultra-low noise, high-order frequency multiplication.

Three low-cost phase noise measurement systems are developed to characterize phase noise of oscillators, amplifiers and frequency translation devices. Each system is optimized to the component being characterized.

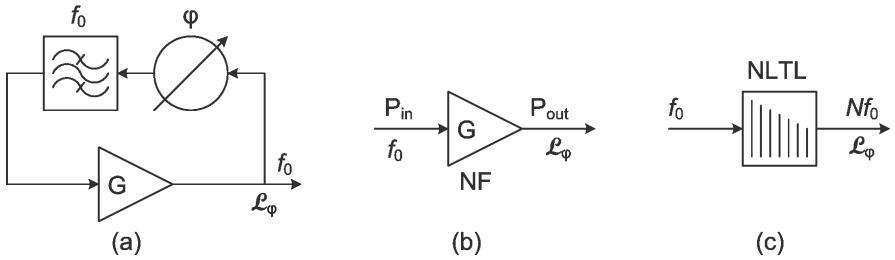


Figure 1.1: Three components used in low-phase noise signal sources. (a) A frequency source (b) Amplifier (c) Frequency Multipliation.

1.2 Thesis Organization

This thesis is organized as follows:

- Chapter 1 presents the overview of the thesis and fundamentals of phase noise. The theoretical basis of open and closed loop phase noise is presented in mathematical form. Effects of phase noise and current state of the art are presented in summary.

- Chapter 2 addresses the design and phase noise performance of ultra low-power microwave bipolar transistor oscillators for use in cesium-based atomic references. The goal of this work is to produce a local oscillator for a chip scale atomic clock (CSAC) with sufficient spectral purity, output power and minimal size while consuming only 16mW.

  This oscillator has the best simultaneous performance in regards to size, power consumption, phase noise and temperature stability of any published or commercial design [1]. The main conclusion is that it is possible to design a low-cost miniature low-power consumption oscillator with sufficient purity to lock to an atomic clock frequency reference.

- In chapter 3, three measurement systems are described. The method of characterization of microwave oscillator phase noise, added phase noise in X-band

power amplifiers and added phase noise in frequency translation devices from 200MHz to 10GHz is described.

A delay-line discriminator for measuring oscillators is presented. The use of an extremely low loss line and appropriate use of power splitting has extended the range of fundamental delay-line measurements to over 10GHz.

In these, it is critical to have a low noise floor, so methods for reducing system level phase noise are detailed. In particular, low-cost, high-performance dedicated solutions are proved.

- In Chapter 4, the spectral performance of X-band class-E PAs is analyzed in the context of high-efficiency CW transmitters. The use of power amplifiers (PA) with 70% efficiency at 10GHz significantly reduces the overall system power consumption, but is shown to affect the phase noise performance. The extent of the degradation due to high-efficiency PAs will depend on the spectral purity signal source being amplified.

- Presented in Chapter 5 is the design and simulation of NLTLs for use as frequency multipliers. NLTLs have been used successfully in equivalent time sampling and pulse shaping circuits. However, the noise process of NLTLs, until now, have not been explored as an alternative to the step recovery diode. It is shown for the first time that varactor based NLTLs have superior noise performance to step-recovery diode multipliers. The phase noise is comparable to two-diode multipliers with the potential for improved noise.

- Chapter 6 contains the phase noise measurement setup and results of the NLTLs designed in Chapter 5 with the measurement system described in Chapter 3.

  Measurements of high multiplication factors (X20-X40) from schottky-varactor based NLTLs are presented. No detectable difference between the measurement

noise floor and that of the NLTLs was observable in a single channel measurement system.

A second measurement at lower frequency (200MHz to 2GHz), is the first measurement to show both fundamental and high order (X10) additive phase noise measurements. Greater than theoretical noise multiplication was observed in step recovery diodes while NLTLs followed ideal multiplication. Optimization of NLTL bias was used to improve phase noise to -180dBc/Hz at 10kHz offset.

- Chapter 7 is a discussion of the main contributions of the thesis, as well as some suggestions for future work.

1.3 Phase Noise

The metric in this thesis is phase noise. The goal of this section is to provide a phase noise overview and introduce quantities used in the remainder of this thesis.

1.3.1 Phase Noise Defined

Frequency stability can be defined as the degree to which an oscillating source produces the same frequency throughout a specified period of time. Every RF and microwave source exhibits some amount of frequency instability. This can be broken down into two components - long-term and short-term stability. [2]. Fig. 1.2 is an illustration of the two stability measurements.

Mathematically, an ideal oscillator is described by:

$$v(t) = V_0 \cos(2\pi f_0 t) \tag{1.1}$$

Amplitude and phase noise can be added with $\epsilon(t)$ and $\Delta\phi(t)$, respectively.

$$v(t) = (V_0 + \epsilon(t)) \cos(2\pi f_0 t + \Delta\phi(t)) \tag{1.2}$$

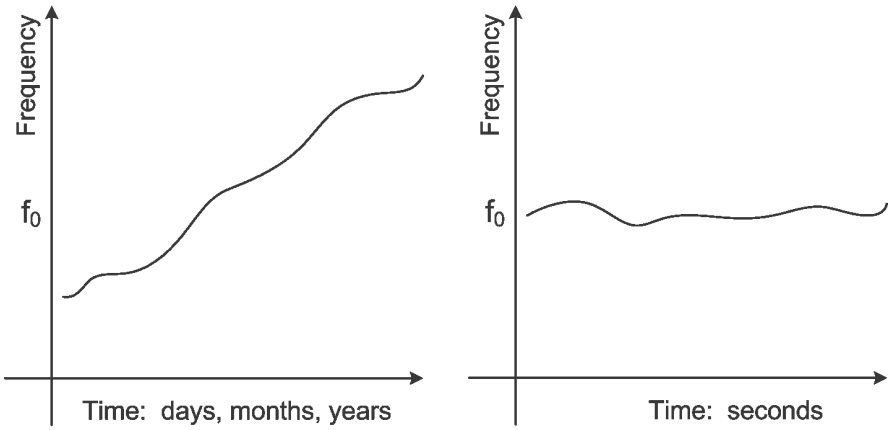


Figure 1.2: Illustration of long-term stability (left) and short-term stability (right). Long term stability is measured over minutes to years. Short term stability is typically measured at seconds or less.

This thesis is primarily concerned with short-term stability, commonly referred to as phase noise. Phase noise is random in nature and is observable as a power spectral density at an offset frequency from the carrier. The fundamental definition of phase noise is a power spectral density of phase fluctuations on a per-Hertz basis for a given fourier or offset frequency f_m described by:

$$S_\phi(f_m) = \frac{\Delta\phi^2(f_m)}{\mathrm{BW}} \left[\frac{\mathrm{rad}^2}{\mathrm{Hz}}\right] \tag{1.3}$$

S_ϕ is a double sideband (DSB) definition. Most often phase noise is referred to as a single sideband (SSB) quantity, $\mathcal{L}(f_m)$, by the relation [3]:

$$\mathcal{L}(f_m) = \frac{1}{2} S_\phi(f_m) \tag{1.4}$$

The quantitiy $\mathcal{L}(f_m)$ is likewise expressed in relation to the carrier power normalized to a 1Hz BW:

$$\mathcal{L}(f_m) = \frac{\mathrm{P_{SSB}}}{\mathrm{Pcarrier}} (\mathrm{dBc/Hz}) \tag{1.5}$$

Leeson [4] quantified noise processes observed in phase noise measurements from properties in an oscillator, commonly referred to as the Leeson equation. In the next few sections, noise processes exhibited by amplifiers, oscillators and frequency multipliers are presented.

1.3.2 Johnson Noise and Noise Figure

Passive and active components exhibit noise. Passive components exhibit noise dominated by the Johnson noise of the equivalent resistance. In a 50Ω microwave system the thermal or Johnson noise level is approximated by:

$$N = kTR = -204\mathrm{dBW/Hz} = -174\mathrm{dBm/Hz} \tag{1.6}$$

This level is commonly referred to as the thermal noise floor. Thermal noise is built up of equal components amplitude noise and phase noise [5]. The discussion here is limited to phase noise and the amplitude noise portion of the thermal noise floor is removed.

$$N_{phase} = \frac{kT}{2} = -177\text{dBm/Hz} \tag{1.7}$$

For the remainder of this thesis, the thermal limit of -177dBm/Hz is used in this context of a 50Ω environment at room temperature.

A two-port network may contribute additional random noise to the the thermal noise floor. An amplifier, for example, adds a quantity of noise called the noise factor (F), more commonly expressed in dB as noise figure (NF). The noise figure is related to an equivalent temperature of the device, typically much higher than room temperature. The phase noise floor is modified by the introduction of this two port noise by:

$$N_{phase} = \frac{kTF}{2} = -177\text{dBm/Hz} + \text{NF(dB)} \tag{1.8}$$

Relating the noise floor to the input power and expressing in terms of $\mathcal{L}(f_m)$:

$$\mathcal{L}f_m = \frac{kTF}{2P_{in}}(\text{dBc/Hz}) \tag{1.9}$$

This is the introduction of the phase noise floor in terms of thermal and noise figure properties in relation to the power input. The noise is flat with respect to offset frequency.

1.3.3 Flicker Noise

All semiconductor based components, as well as some passive components, exhibit a frequency dependent noise known as flicker noise [6]. In active devices, it relates to the random electron or hole path velocity across the crystal structure. This is a near

DC noise that is proportional to $\frac{1}{f}$. The flicker noise is upconverted to microwave frequencies through nonlinearities in the semiconductor device [7]. The flicker corner, f_c is defined at the point the flicker noise doubles the noise power, or an increase in 3dB. $\mathcal{L}(f_m)$ may be written in terms of thermal noise (kT2), noise factor (F), power input P_{in} and flicker corner (f_c) as a function of frequency offset (f_m).

$$\mathcal{L}(f_m) = 10\log_{10}\left[\left(\frac{kTF}{2P_{in}}\right)\left(1+\frac{f_c}{f_m}\right)\right] \text{(dBc/Hz)} \tag{1.10}$$

This is shown graphically in Fig. 1.3 and is descriptive for any passive or active device. The noise figure due to passive devices is typically the loss associated with them. A 6dB attenuator has a noise figure of 6dB. Passive components may exhibit a flicker noise effect [8]. For example, ferrite based components can be sensitive to internal current densities and introduce a frequency dependent noise. Any time an electron moves in a material, there exists an average velocity with some distribution based on physical interaction. The mean distribution of this velocity is seen as flicker noise.

1.3.4 Phase Noise in Oscillators

The discussion up to this point has involved additive phase noise contributions in a two-port open-loop environment. An oscillator consists of a closed-loop environment and noise contributions from those discussed become multiplicative. The introduction of a resonator adds a second order (20dB/decade) noise process based on the selectivity of the resonator. The components of an oscillator are illustrated in Fig. 1.4.

Leeson developed heuristically an equation describing the observed phase noise of an oscillator relative to performance parameters of the components in an oscillator in [4, 9] and subsequently derived in [10, 11].

The closed loop phase noise is the noise due to the amplifier in the presence of a frequency selective feedback with finite bandwidth. The loaded quality factor (Q_L) of a resonator is defined as the average energy stored divided by the average energy lost per

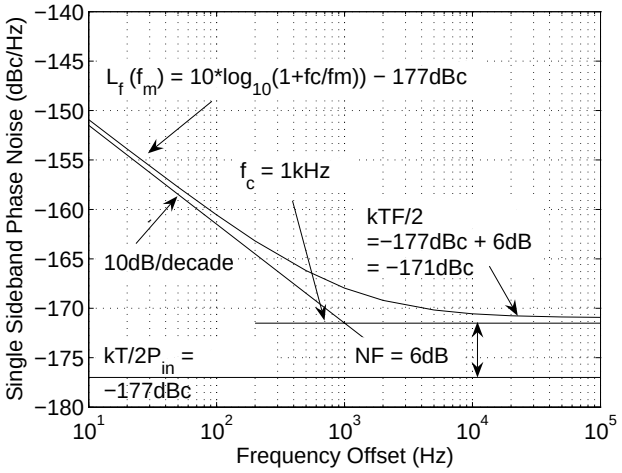


Figure 1.3: Illustrative example of phase noise due to an amplifier. Assuming a Pin to the amplifier of 0dBm, the noise floor is -177dBc. The amplifier increases the noise floor by the noise figure of 6dB to -171dBc/Hz. Close to the carrier, the flicker noise of the amplifier increases the phase noise at 10dB/decade with a corner frequency f_c of 1kHz.

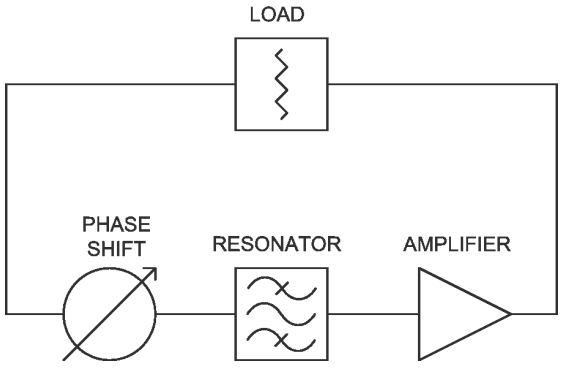


Figure 1.4: The main components of an oscillator. Amplifier, load, frequency selective feedback (resonator) and phase shifter. The two source of phase noise are the amplifier and resonator.

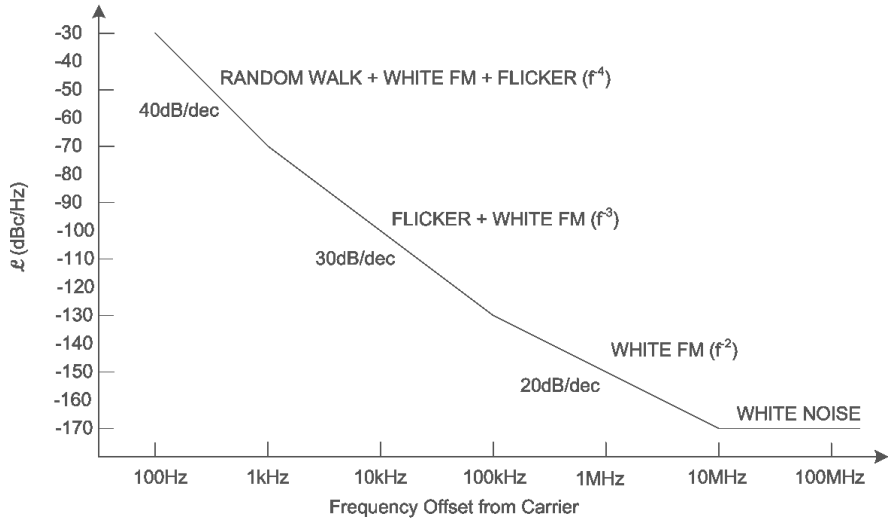


Figure 1.5: An example phase noise plot from a 1GHz oscillator with representative phase noise values at appropriate frequency offsets.

second, multiplied by the resonant frequency. This may be rewritten in terms of circuit parameters as the resonant frequency divided by the bandwidth.

$$Q_L = \omega \frac{2W_m}{P_{loss}} = \frac{f_0}{BW} \tag{1.11}$$

The phase noise due to the finite Q factor of the resonator added to Eqn. 1.10 and known as Leeson's equation [4].

$$\mathcal{L}_\phi(f_m) = 10 \log_{10} \left[\left(1 + \frac{f_0^2}{(2f_m Q_L)^2} \right) \left(1 + \frac{f_c}{f_m} \right) \left(\frac{kTF}{2P_{in}} \right) \right] \text{(dBc/Hz)} \tag{1.12}$$

Fig. 1.5 is a graphical representation of the phase noise components identified in Eqn. 1.12.

1.3.5 Frequency Multiplication and Division

The performance of an oscillator is significantly dependent on the technology used to construct the frequency selective element or resonator. Physical standards that use acoustical components such as crystal oscillators exhibit unloaded Q factors over 1

million and achieve optimal phase noise near 100MHz. A high frequency microwave oscillator utilizes a resonator based on electromagnetic properties. Examples are dielectric resonators, coaxial resonators, waveguide cavities, Fabry-Perot, etc. A lower frequency oscillator may be frequency multiplied by N to a higher frequency with the degradation in phase noise related by:

$$N_{additional} = 20log(N) \tag{1.13}$$

If N is less than 1, as in a frequency divider, the noise will be negative, or improve the phase noise of the system. If N is greater than 1, then the phase noise is degraded. By this relation, the optimum oscillator and multiplication circuit can be derived for the lowest possible noise at a given frequency. For a frequency multiplication of X2:

$$v(t) = \sin(2\pi f_0 + \Delta\phi(t)) \cdot \cos(2\pi f_0 t + \Delta\phi(t)) = \frac{1}{2}\sin(4\pi f_0 + 2\Delta\phi(t)) \tag{1.14}$$

Here, the noise is multiplied by the same factor as the frequency. The relation is 20logN because the multiplication is in terms of voltage.

Phase noise can alternately be seen in the time domain as jitter. If a 100MHz signal exhibits 1ps of jitter and is then multiplied by 10, the jitter remains at 1ps, while the period of the multiplied signal is 10X shorter. Thus, 1-ps jitter is a larger fraction of the signal. The relative phase fluctuations have increased by a factor of 10.

1.4 Phase Noise and System Performance

Phase noise requirements vary for all types of systems. A common cellular phone local oscillator may exhibit a phase noise of -80dBc/Hz at 10kHz at 1.8GHz. By contrast, a GPS satellite system may exhibit -150dBc/Hz at 10kHz at 1.5GHz. Laboratory grade low-phase noise standards are often 20-30dB below that of a high performance communication or radar source.

It can be concluded that low-phase noise is a relative term. This thesis focuses on low-phase noise sources in the context of application rather than laboratory standards. While the frequency multipliers shown in Chapter 5 and 6 exhibit phase noise on par with the best low frequency sources, some laboratory grade equipment will exceed this performance at the expense of size, power, repeatability, etc.

Discussed in this section is a brief qualitative analysis of phase noise in two systems. Frequency multiplication technology vs. fundamental oscillators and the phase noise compromise is discussed. Again, it is stressed that low-phase noise is always in terms of some system design goal, and not necessarily an absolute measure.

1.4.1 Effects of Phase Noise on Communications System Performance

The effects of noise present in a phase modulated communications system is graphically presented in the phasor diagram of Fig. 1.6. Here, a constellation diagram identifies the four symbol locations of a quadrature phase shift keying (QPSK) system and the effects of AM and PM noise on symbol location. Phase noise affects the polar angle locations of the symbols. The symbol error rate (SER) increases proportionally to phase noise as discussed in [12, 13].

In space based communications systems, the cost of data transmission is directly proportional to the data rate that can be transmitted with a reasonable bit error rate. Within an allocated channel, increasing the number of symbols at the same frequency increases data transfer linearly. Improvements in low noise satellite and ground based sources will lead to a lower cost of data transfer.

1.4.2 Effects of Phase Noise in Radar Systems

A Doppler radar identifies the velocity of a object by beating the transmitted carrier with the wave reflected from the moving target and monitoring the small change in frequency. The Doppler shift for object moving at speeds between 10m/s and 500km/s

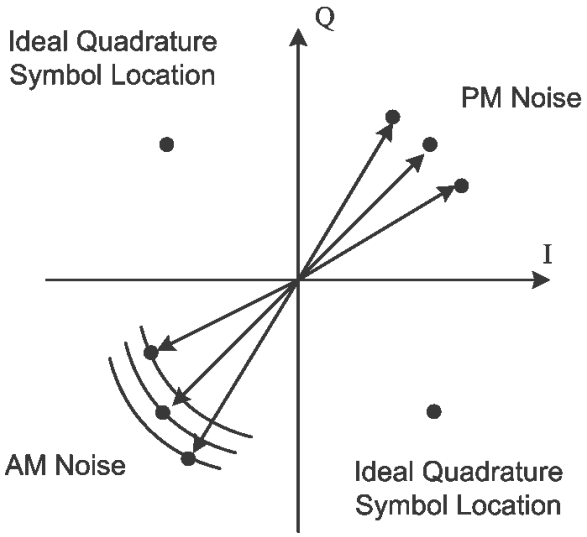


Figure 1.6: IQ diagram showing the effects of amplitude noise (AM) and phase noise (PM) on a phase modulated signal. AM and PM noise cause dispersion of the symbol location, increasing the symbol error rate.

is in the range of 67Hz to 3.3MHz according to $F_D = \frac{2vf}{c}$, where v is the velocity of object. The source phase noise directly determines the radar sensitivity and is shown graphically in In Fig. 1.7. Any phase noise of the oscillator at offsets comparable to f_D can mask the the reflected signal.

1.5 Contributions to be Presented

The components of an example X-band multiplied source are shown in Fig. 1.8. Contributions from this thesis are marked on the lower half of the figure. Beginning from left to right, the chip scale atomic clock local oscillator is used to lock a crystal oscillator that exhibits excellent short term stability. The source is amplified a power amplifier and the added noise quantified. Tradeoffs in PA design are identified for reduced additive phase noise. The multiplier element, a nonlinear transmission line (NLTL) is developed in this thesis specifically for low phase noise frequency multiplication. Filtering and amplification are again followed by a second NLTL multiplier and a 10GHz filter. The final amplification can done through a high efficiency amplifier while maintaining acceptable phase noise.

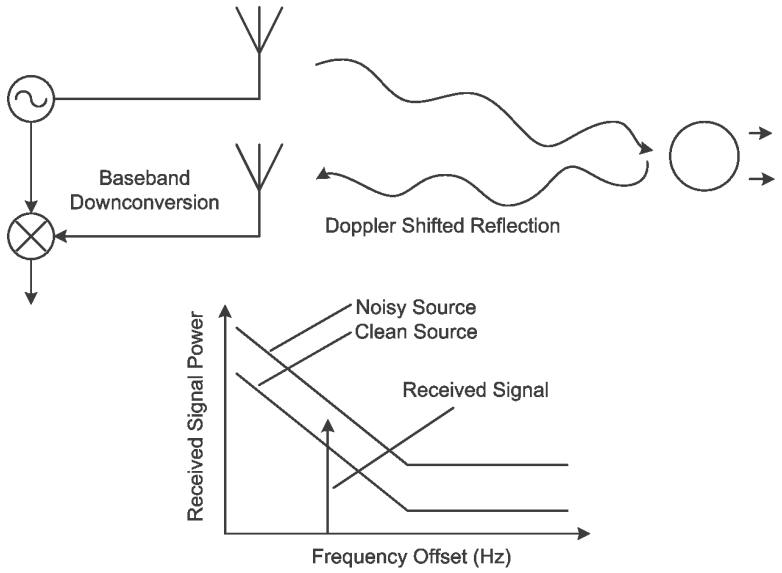


Figure 1.7: A simplified doppler shift radar system demonstrating the effects of phase noise on the downconverted doppler shift. The reflected signal will be extremely low power and can be overshadowed by an oscillator with too much noise.

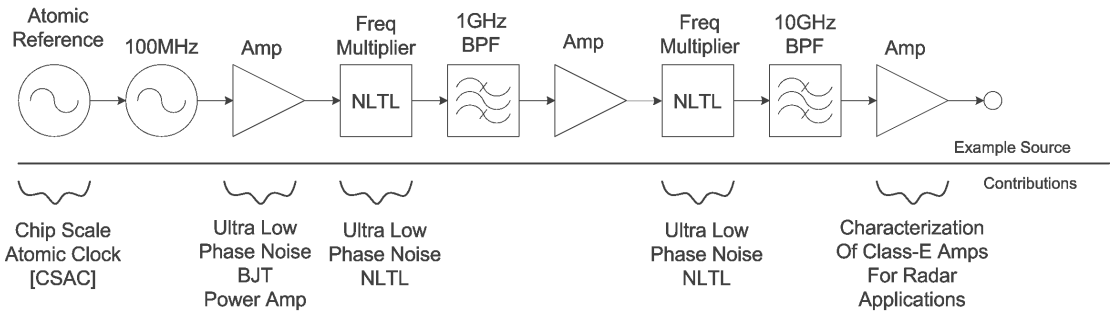


Figure 1.8: Sketch of component-level topics addressed in this thesis for communication or radar applications. A very stable low phase noise crystal oscillator is frequency locked to a long term atomic standard. The output is multiplied in two stages. In this example, two NLTLs are used with the appropriate harmonic filtered and efficiently amplified.

Chapter 2

Chip Scale Atomic Clock Oscillator

Free-running oscillators based on electro-mechanical or acoustic-mechanical resonance typically have excellent short-term stability while long-term stability suffers. Environmental aspects such as temperature and aging of components have the undesired effect of long-term frequency drift. Applications such as base station communication and network synchronization have stability requirements exceeding that of the best crystal oscillators. In 1945, it was proposed by Isidor Rabi that a microwave oscillator could be locked to a property of the ammonia atom using a technique called atomic beam magnetic resonance. The magnetic resonance has a very high effective Q, is based on atomic properties rather than a mechanical process and has the advantage of improved long-term frequency stability.

The National Bureau of Standards (NBS), now the National Institute of Standards and Technology (NIST), introduced in 1949 the first ammonia based atomic clock that utilized the technique proposed by Rabi. Then in 1952, NIST developed the first cesium based atomic clock known as the NBS-1. Work continued over the next 15 years, standardizing and commercializing the cesium atomic clock. In 1967, the 13th General Conference on Weights and Measures defined the International System (SI) unit of time, the second, as the duration of 9,192,631,770 cycles of microwave light absorbed or emitted by the hyperfine transition of cesium-133 (CS-133) atoms in their ground state undisturbed by external fields.

The cesium atomic clock operates on the following principle: according to quantum theory, atoms can only exist in certain discrete energy states depending on what orbits are occupied by the electrons. The atomic clock operates off a change in the electron and nuclear spin or hyperfine energy level of the lowest set of orbits called the ground state. The cesium atoms are kept as gas in a near vacuum to avoid interaction with other particles and are shielded from any stray magnetic fields.

Atomic clock size has in the past been limited by the size of the microwave cavity required to excite the ground state hyperfine splitting transition of alkali metals [14]. More recently, coherent population trapping has shown itself to be the most promising alternative to light-pumping of atoms for ultra-miniature frequency references because it eliminates the need for the microwave cavity, resulting in significantly smaller size and power consumption [15]. In this method, a laser is tuned to the optical absorption frequency of atoms (typically Rb or Cs). A microwave oscillator is then used to directly modulate the laser light field, causing the same hyperfine transition, but with no requirement for a large microwave cavity.

The ultimate goal is a chip-scale atomic clock (CSAC) that includes a glass cell containing atoms, a vertical-cavity surface-emitting laser (VCSEL) at the optical resonant wavelength of the atoms, a photodetector, associated optics, a microwave voltage-controlled oscillator (VCO) which locks to the atomic coherent population trapping (CPT) resonance, thermal management and locking circuitry, all in a 1-cm3, 30-mW package. A large fraction of the power needs to be dedicated to thermal management and locking [16], leaving a small power budget for the VCO. To be comparable in stability with existing compact atomic frequency references, a fractional frequency instability below 10-11 is required at one-hour integration times and longer [16].

In the system described, the VCSEL is modulated at half the CPT resonance of the atoms at approximately 4.6GHz. Frequency modulation is used to continually sweep across the CPT resonance and differentiated to find an error signal fed back to

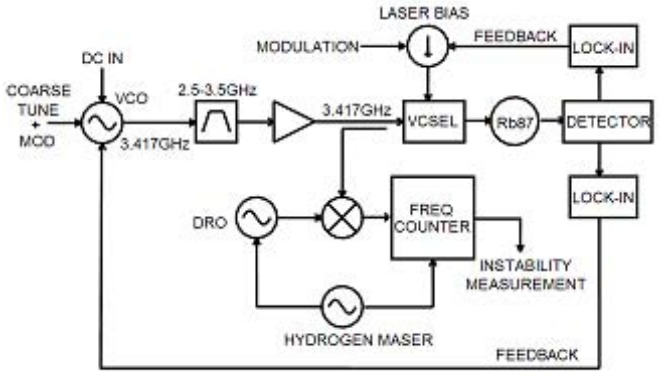


Figure 2.1: System used to lock the atomic clock The system shown is for a Rubidium-87 cell. Prior to locking the 4.6GHz oscillator to the cesium atomic cell, the project focus was switched to Rubidium. The oscillator presented here was downconverted using a synthesizer to the appropriate 3.4GHz frequency and inserted into the system shown.

the oscillator tune port. The feedback system described is a frequency locked. The schematic of the system used to lock the oscillator is shown in Fig. 2.1.

2.1 Local Oscillator for Chip Scale Atomic Clocks

The oscillator for a miniature atomic clock, at the time of the writing, is required to have a Allen deviation less than $1 \cdot 10^{-11}$ at one hour integration when locked to the miniature atomic package. This implies that it must simultaneous size, power consumption, phase noise and stability criteria unavailable in current oscillators, which consumes watts of power for Allen deviations of $1 \cdot 10^{-12}$. Rather than attempting new device research to improve Q or reduce size, a more practical approach targeting optimization of proven components was utilized.

The footprint of $1cm^2$ is set as the 2-dimensional limit of the $1cm^3$ goal for the chip-scale atomic clock, which is a current topic of research at a number of labs (NIST, Rockwell Collins, Agilent). The phase nosie and output power is derived from the calculated performance necessary to lock to the miniature atomics package. The oscillator power budget is calculated to be about 2/3 of the total DC power consumption.

Dr. John Kitching from NIST estimated the necessary phase noise of the local oscillator to be -25dBc/Hz at 100Hz from the carrier.

The oscillator presented in [1, 17] meets the specifications with the exception of the output power. However, recent work on the vertical cavity surface emitting laser (VCSEL) diodes for optical drive has reduced the RF power requirement by about 5dB. The DC power consumption listed is the highest power the oscillator has been operated and is optimum for phase noise. Lower DC power consumption levels are achieved by reducing the drain bias and the oscillator operates down to approximately 5mW. The specifications and final oscillator performance are summarized by 2.2.

Description	Specification	Results
Size	Planar $1cm^2$	$1cm^2$
Phase Noise	-25dBc Hz 100Hz	-30dBc Hz
DC Power	¡ 20mW	16mW (2V @8mA)
Shock and Vibe	non-crystal	Ceramic Coaxial Resonator
RF Power	0dBm	-3dBm
Temmperature Coefficient	Undetermined	20ppmC (25C)
Tunability	Sufficient to Lock	0.5% (23MHz)

Table 2.1: The required and measured oscillator performance specifications are shown here. Some parameters, such as shock and vibe and temperature stability were unspecified. Phase noise was the most critical parameter to meet beyond the general size and frequency requirements. Without good phase noise, the oscillator could not be locked.

2.1.1 Required Q Factor of the LO

A resonator loaded Q-factor of 50 is determined to be sufficient for this application from the following assumptions. Assuming a loaded Q of 50, an input power level of -6dBm, a flicker corner of 10kHz and a noise figure of 6dB, Eqn. 1.12 predicts the phase noise in Table 2.2.

A two-fold increase in Q factor will improve these values by 6dB. What is not predicted by Eqn. 1.12 are any effects such as thermal drift close to the carrier that can add an additional 10dB/decade of phase noise. A Q-factor of 50 allows a margin

Frequency Offset	Calculated Phase Noise
100Hz	-39dBc/Hz
1kHz	-68dBc/Hz
10kHz	-96dBc/Hz
100kHz	-119dBc/Hz

Table 2.2: Calculated Q factor based on a loaded Q of 50, 10kHz flicker corner and Pin of -6dBm.

of error of 14dB close to the carrier. This allows for a 1kHz thermal flicker corner and 4dB of uncertainty in the Pin and Noise figure estimation. Likewise, simulation models often do not include a good model of the flicker noise of the active device. The 10kHz and 100kHz values from Table 2.2 were used as a simulation design goal when harmonic balance analysis of the resonator was completed.

2.2 Oscillator Design

Many oscillator topologies exist , the two most common in texts being the Colpitts and Hartley [18]. In the microwave frequency range all microwave oscillators utilizing a 3-terminal active device (or 2-terminal grounded device) can be discussed as a common-emitter amplifier topology with either series or parallel feedback. The benefit to this is each component may be analyzed individually for improved model creation. Most importantly, components may be analyzed for spurious responses. The design of the oscillator circuit includes: (1) choice of transistor (2) choice of and positioning of tuning element and (3) bias design and (4) choice of resonator.

2.2.1 Choice of Transistor and Tuning Element

Available dielectric resonator oscillators at 4.6GHz typically use a Gallium Arsenide (GaAs) field effect transistor (FET) as the active device. Silicon Germanium (SiGe) has become a popular option for oscillator design as well. However, silicon bipolar devices still perform the best with regards to flicker noise. Flicker noise affects the

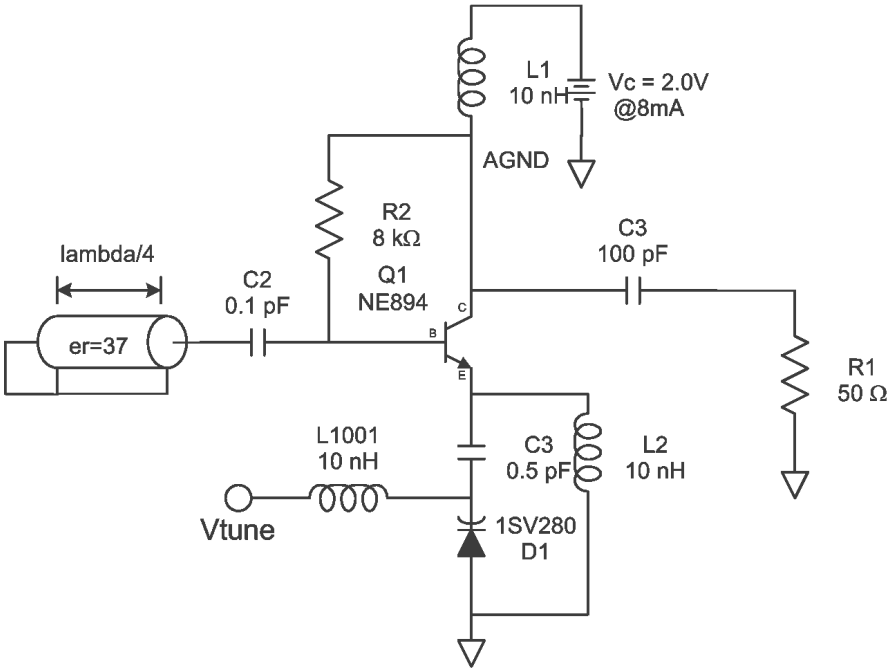


Figure 2.2: Oscillator schematic. L1, L2 and L3 provide DC bias. The quiescient bias current is set by R2 and the g_m of the NE894. R1 is the load external to the oscillator. In this case, 50Ω.

phase noise very close to the carrier by 10-30dB depending on the device technology.

The phase noise specification at 100Hz offset means the phase noise will be extremely sensitive to the flicker corner of the device. Silicon Germanium (SiGe) and MESFET both have flicker corners between 50kHz and 1MHz, respectively. Silicon bipolars typically have flicker corners between 5kHz and 15kHz. A new class of high frequency (f_T=25GHz device process) silicon bipolar devices has become available that is enabling oscillator designs to 10GHz.

Two factors determine how much gain a device should have: the loss of the resonator and the desired amount of compression of the closed-loop oscillator. For a critically-coupled resonator, where half the power is in the load and half the power is in the resonator, the loss is 3dB. Low levels of compression may seem to be ideal, but an oscillator must stay in compression at high temperatures, shock or voltage variance. Therefore a few dB of compression is desireable. At compression of more than 3-5dB, transistors begin to operate significantly different from small-signal mode. Therefore, an open loop gain of approximately 6dB, requiring adjustment for actual resonator losses, is a reasonable starting point.

Assuming a gain requirement of 6dB, practical oscillator theory suggests a transistor with an f_T of twice that of the resonance frequency. The f_T parameter of a given device is heavily current-dependent. In this design, an NE894 silicon BJT from California Eastern Laboratories was used. The datasheet specifies the gain to be approximately 1 at 10GHz, close to the desired 9GHz assumption.

The tuning element is a silicon hyperabrupt varactor available from Toshiba, 1SV280. Placement of the varactor allows tuning of frequency without affecting the loaded-Q of the resonator. In this design, it was incorporated into the feedback path. The feedback path sets the closed loop phase shift to be a multiple of 2π. Adjusting the phase around the loop tunes the frequency of oscillation inside the bandwidth of the resonator.

2.2.2 Passive Circuit Components

While chip and wire assembly for microwave oscillators has been the standard, improvements in surface-mount technology make 20GHz assembly nearly commonplace. Surface mountable 0402 size capacitors measuring 1mm by 0.5mm are available in values a small as 0.1pF. Internally, they are a ceramic dielectric metal-insulator-metal parallel plate capacitor. The tolerance is less than a coupled microstrip circuit could produce at $\pm 0.05\,\mathrm{pF}$ but careful tolerance analysis in simulation showed that this effect did not degrade performance by more than a few dB. Surface mountable resistors operate nearly ideally at 4.6GHz, as the distributed resistance over a large area ensures very low self inductance.

2.2.3 Bias Network Design

While inductors begin to suffer in accuracy at 4.6GHz, as their value increases while approaching the first self resonance frequency, they make excellent bias inductors. The same property that exhibits surface mountable inductors from high frequency filters, namely the parallel resonance, improves the performance as a bias inductor. The operation of a bias inductor is to appear as an open circuit to a transmission line. Mutual inter-winding capacitances between inductor turns are equivalent to a capacitance in parallel with the inductance. The first resonance of an inductor is therefore a parallel resonance. The input impedance of an inductor in parallel resonance is greater than $2\mathrm{k}\Omega$, a desirable trait for a bias inductor. The second, series, resonance does not occur until much later, typically at least twice the parallel resonant frequency. The conclusion is that a given inductor may be used as a bias inductor to approximately $1.5 f_{res}$ where f_{res} is the self resonant frequency given in manufacturers datasheets. A common 220-nH 0603 inductor from Coilcraft creates an excellent bias inductor from 50MHz, to 5GHz, spanning 2 decades and costing only pennies.

It must be noted however, that measuring the inductor in-situ is preferred to trusting the datasheets. It has been observed that the series resonance can be many orders of magnitude above the parallel resonance, creating a very useful bias inductor. Ferrite loaded inductors, commonly used in switching regulator and power supplies, benefit from a lossy magnetic material that decreases the Q-factor. An inductor with a Q factor approaching unity is by definition an ultra-wideband inductor without any visible self resonance. This method is exploited in wideband inductors made by Piconics Inc. A conical wirewound structure is backfilled with lossy ferrite material. As the inductance gets larger, where typically a parallel resonance would occur earlier, the lossy ferrite material effectively reduces the Q-factor, eliminating resonances. By this method, bias inductors operating from 100kHz to 60GHz with only a few tenths of a dB loss have been developed.

2.2.4 Resonator Choice, Design and Analysis

As previously introduced, a design approach focusing on optimization of commercially available components was used rather than introduction of new technology. The simple Q-factor analysis determined a loaded Q of 50 meets performance specifications. Dielectric resonator oscillators (DRO) offer the best performance for this application at 4.6GHz with a loaded Q between 100 and 500. Unfortunately, size of the pucks would exceed the $1cm^2$ specification. Therefore, a more traditional coaxial resonator. Dielectric pucks are often made of very high dielectric constant that come in a variety of temperature stabilities and are known for their tolerance to vibration. Recent advances in manufacturing have allowed this high dielectric material to be adapted to coaxial resonators, dramatically reducing their size and improving temperature stability.

The outer part of the coax is near rectangular with a circular center conductor. Plated silver forms the wall boundaries for low loss. The size of the resonator is a quarter of a guided wavelength and is shorted on the non-coupled end. The result is a highly

temperature stable, high-Q factor surface mountable component with the potential for low vibration sensitivity. In high quantities, the cost of a micro-coaxial resonator is expected to be below $1.00.

Two types of coaxial resonators are available, a shorted $\lambda/4$ and an open circuit $\lambda/2$. The $\lambda/4$ resonator was chosen for its smaller size and only slightly reduced Q-factor. The natural resonance of a shorted line is a parallel resonance. With a characteristic impedance of only 8Ω, an additional circuit component must be used to transform this impedance to that matching a circuit between 50Ω and 100Ω. Using the example in [19] the critical coupling capacitance, C_c for a given impedance and Q factor is:

$$Cc = \frac{1}{\omega Z_{res}} \sqrt{\frac{\pi}{2Q_U}} \tag{2.1}$$

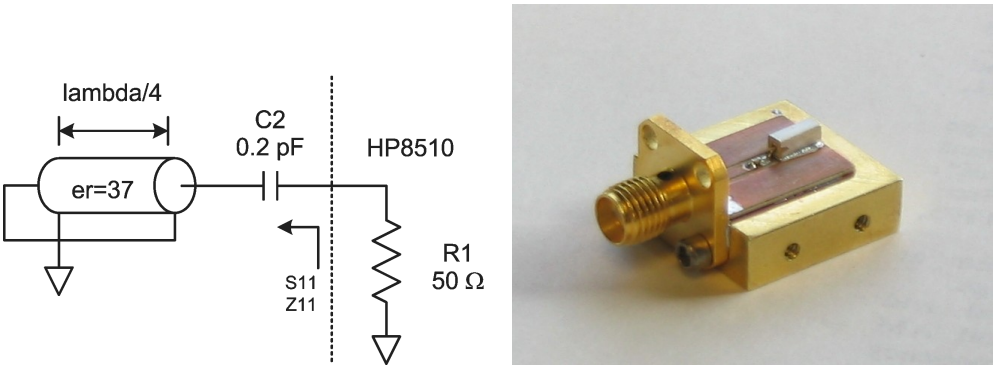
Table 2.3 lists a range of optimal C_c depending on circuit parameters. Tolerance analysis is critical as the coupling capacitors are extremely small and the tolerance is typically ± 0.05 pF.

Q_U	C_c for $Z_0 = 25\Omega$	C_c for $Z_0 = 50\Omega$	$Z_0 = 100\Omega$
200	0.122 pF	0.061 pF	0.03 pF
220	0.144 pF	0.057 pF	0.029 pF
240	0.110 pF	0.055 pF	0.028 pF
260	0.106 pF	0.053 pF	0.027 pF
280	0.102 pF	0.051 pF	0.026 pF
300	0.100 pF	0.05 pF	0.025 pF

Table 2.3: Critical coupling C_c capacitances assuming circuit impedance Z_res, frequency (ω) and unloaded Q, Q_U.

To determine loaded and unloaded Q for a given coupling coefficient a test circuit was constructed. Fig. 2.3(a) and 2.3(b) show schematically and physically the coplanar waveguide (CPW) test structure on Rogers 4003. The final circuit is constructed as a CPW structure in order to use the substrate as thermal isolation to the mounting structure.

The coupling coefficient for this measurement was determined above to be 0.1pF.



(a) (b)

Figure 2.3: Schematic and photograph of test fixture to determine loaded Q Q_L, equivalent circuit and temperature stability of the u-coaxial resonator.

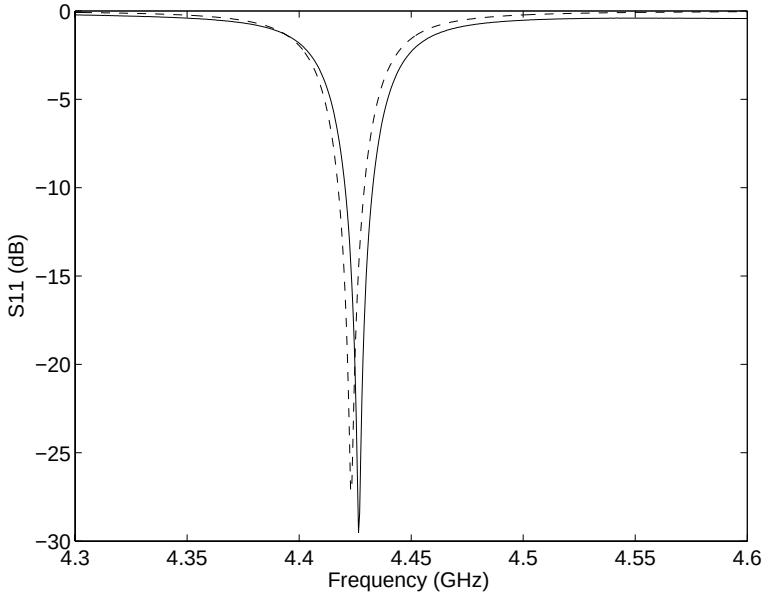


Figure 2.4: Measured S-parameters showing Q-loading from 50Ω network analyzer.

The measured S-parameemter response is shown in fig. 2.4. A transformation between S-parameters and Z-parameters is shown in Fig. 2.5 and 2.6. S-parameters measure only loaded Q-factor in a 50Ω environment. The Z-parameter transformation de-embeds the source impedance of the network analyzer, allowing easy viewing of the actual circuit impedance and phase over frequency. Using Z-parameters both the unloaded Q and loaded Q for any arbitrary circuit can be calculated using the relation:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{\omega}{2}\frac{\delta\phi}{\delta\omega} \tag{2.2}$$

In Figs. 2.5, 2.6 the impedance of the equivalent circuit, calculated with substitution from Eqn. 3.5 is shown. The equivalent circuit, shown in Fig. 2.7, has values corresponding to Q-factor and not necessarily values resembling a physical mechanism.

The resonator temperature coefficient was measuring using a one-port measurement on an 8510 network analyzer while adjusting the temperature of the coaxial resonator. The measurement spanned 1MHz and provided 12.5kHz resolution. A metal enclosed 100ohm 50W resistor was bolted to the brass package base the coaxial res-

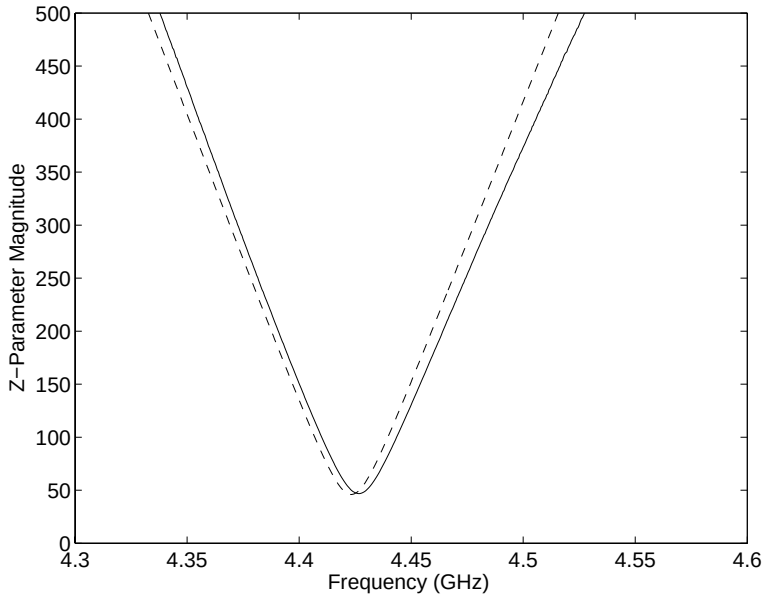


Figure 2.5: Measured S-parameters showing Q-loading from 50Ω network analyzer.

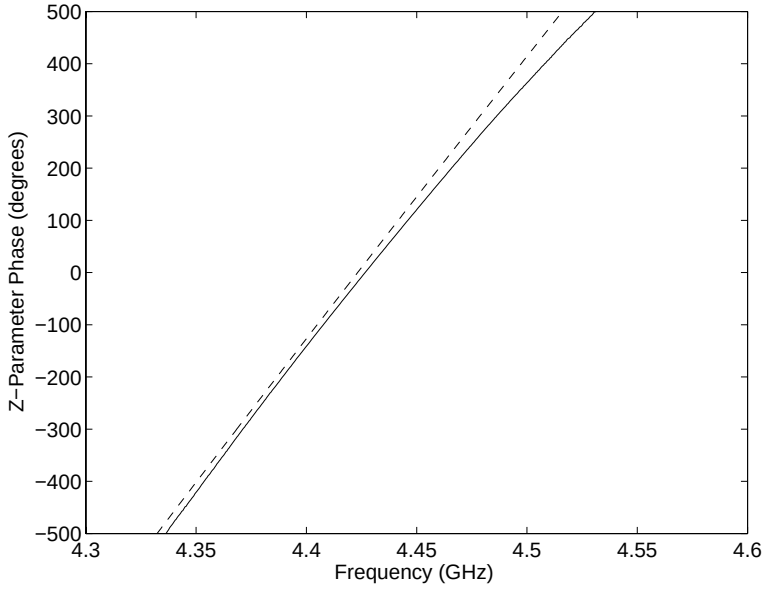


Figure 2.6: Measurements of the resonator (solid) compared to the equivalent circuit model (–). $Q_{unloaded}$ calculated to be 260 from 3.5 while the Q measured directly from S-parameters is 102.

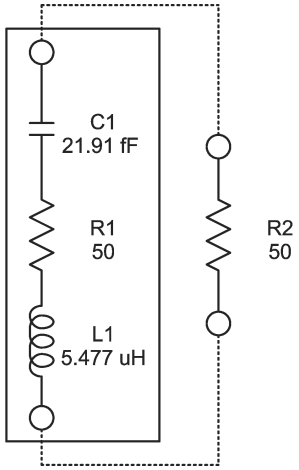


Figure 2.7: Equivalent circuit derived from Z-parameters.

onator was mounted to and the temperature was controlled via a temperature feedback circuit. Temperature was monitor through a Fluke Thermocouple attached to the brass baseplate. The results are presented in Table 2.4.

temp	F_0 (MHz)	S_{11} (dB)	Δf	ΔT	$\Delta T/\Delta C$	T_{coeff}
28.8C	4465.525MHz	-15.04				
29.4C	4465.350MHz	-15.3	175kHz	-6.6C	26.5kHz/$^\circ C$	-5.9ppm/$^\circ C$
36.7C	4464.925MHz	-15.9	425kHz	-7.3C	58.0kHz/$^\circ C$	-13.0ppm/$^\circ C$
43.9C	4464.500MHz	-17.0	425kHz	-7.2C	59.0Hz/$^\circ C$	-13.2ppm/$^\circ C$
50.5C	4464.075MHz	-17.7	425kHz	-6.6C	64.0kHz/$^\circ C$	-14.3ppm/$^\circ C$

Table 2.4: Resonator temperature stability analysis with 0.1pF coupling capacitor present.

The expected results were a temperature coefficient of around +7ppm/C as specified from published coaxial resonator data. The coupling capacitor of 0.1pF has a wide temperature specification of 0ppm/C $\pm$ 30ppm/C. It appears the capacitor dominates most of the temperature coefficient in terms of the resonator. Discussions with Val Jackson at Val Jackson and Assoc. has led to the idea of using the same dielectric of the resonator in a coupling capacitor, thereby improving the temperature coefficient. This may allow matching of the temperature coefficient to that of a selected transistor. Overall the temperature coefficient is approximately -13ppm/C.

2.2.5 One Port to Two Port Conversion and Analysis

The oscillator topology shown in Fig. 2.2 has traditionally been analyzed as a negative resistance oscillator. In [20] it is shown that the oscillator can be broken at the base of the oscillator and plot $1/S_{11}$ of the transistor with S_{11} of the resonator to analyze oscillation condition. Q-factor can also be determined but is difficult to analyze.

A virtual ground technique is presented in [21, 22, 23, 24] that allows two port analysis of all components. In this manner, all components in an oscillator can be analyzed with a network analyzer, and used directly in a model. In steady state conditions, the ground connection is arbitrary and can be placed anywhere in the circuit. In Fig.

2.8(a) the ground connection is closed and shown as a wire while all bias components are removed for simplicity. The virtual ground is placed at the emitter of the BJT for convenience in 2.8(b) and the circuit is redrawn in 2.8(c) in the format for a generalized oscillator.

What is derived from this analysis is identification of all components and their effect on the system. The amplifier and resonator can be analyzed independently using available s-parameters for the active device the resonator using the discussed method. The uncertainty regarding the Q-factor of the varactor on system performance can now be accurately analyzed. In the shown position the varactor is simply a phase shift network tuning the frequency. A low Q-factor varactor here would only reduce the loop gain by a small amount, rather than affecting the Q-factor in any way. However, if the capacitor had been placed in series with the 0.1pF coupling capacitor in the resonator, the Q-factor would have been reduced by a small amount. Conversely, the tuning varactor would not only change the frequency, but the coupling amount, potentially over or under-coupling the resonator.

The output power of the device when in compression may now be independently verified through standard 2-port techniques. One of the most important aspects of the two-port is the load condition is now in the feedback loop and alternate load conditions can be analyzed for oscillation condition and frequency.

2.3 Oscillator Simulation, Construction and Measurements

The simulation is shown in both 2-port small signal analysis and harmonic balance large signal. The simulation schematics used to analyze the oscillator are shown in Fig. 2.9, 2.10 and 2.11. Fig. 2.11 uses the approximate VCSEL load impedance of 1.2pF and 30Ωs.

Harmonic balance simulation using Agilent's Advanced Design System (ADS) accurately and repeatedly predicted the performance of the coax based oscillator in

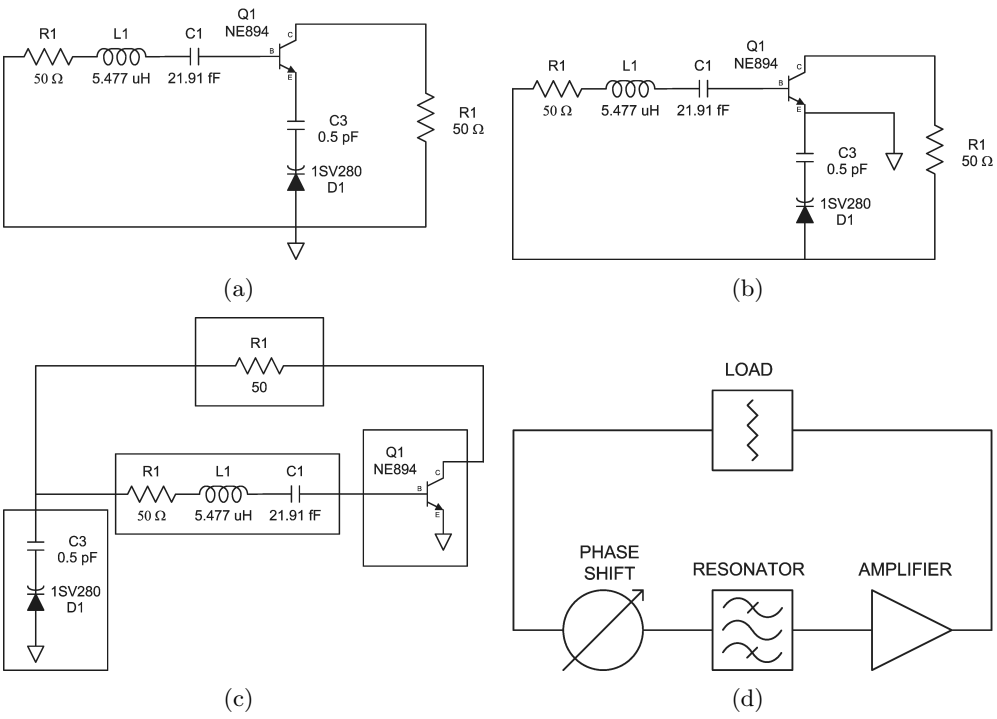


Figure 2.8: Transformation from a 1-port to 2-port oscillator using the virtual ground technique. (c) and (d) show schematically that a 1-port oscillator can be broken into four general oscillator components for individual analysis.

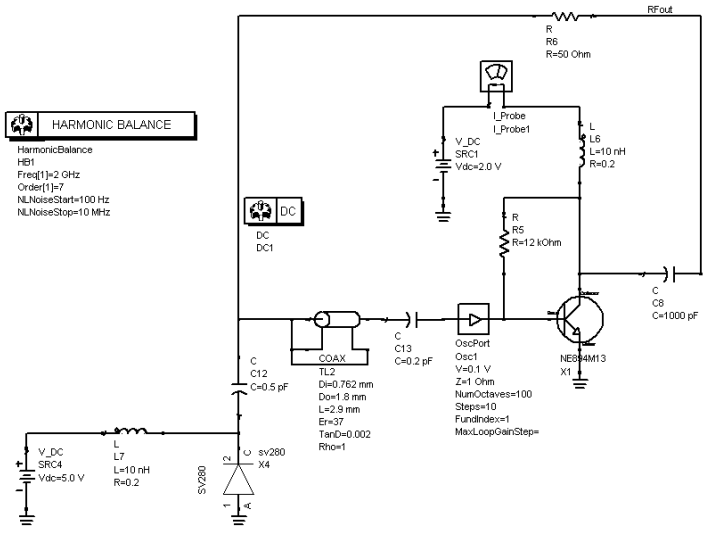


Figure 2.9: Harmonic balance simulation redrawn using the virtual ground technique. The results are identical to the traditional one port schematic shown previously.

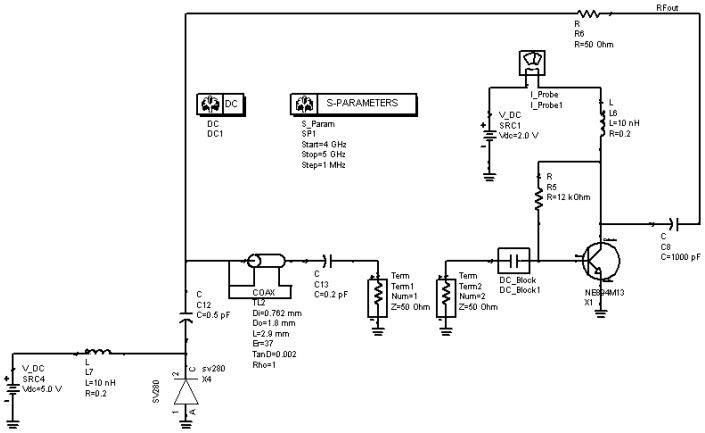


Figure 2.10: Breaking the 2-port loop for linear analysis. This plot shows the phase to be 0degrees around the loop and the gain is 3dB - ideal for an oscillator.

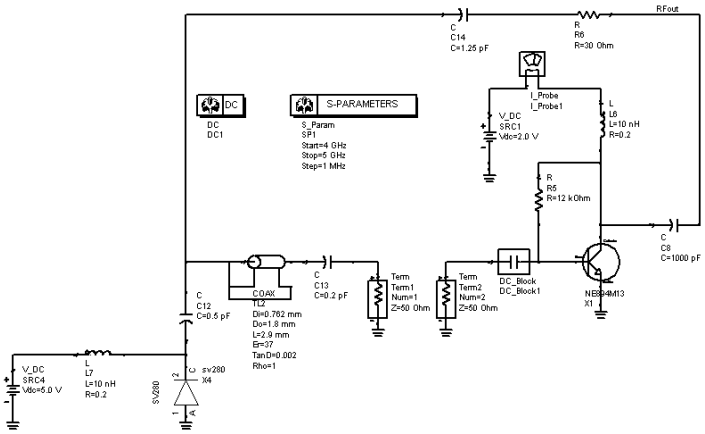


Figure 2.11: Changing the load conditions to the VCSEL shows only a minor shift in operational frequency - up about 10MHz.

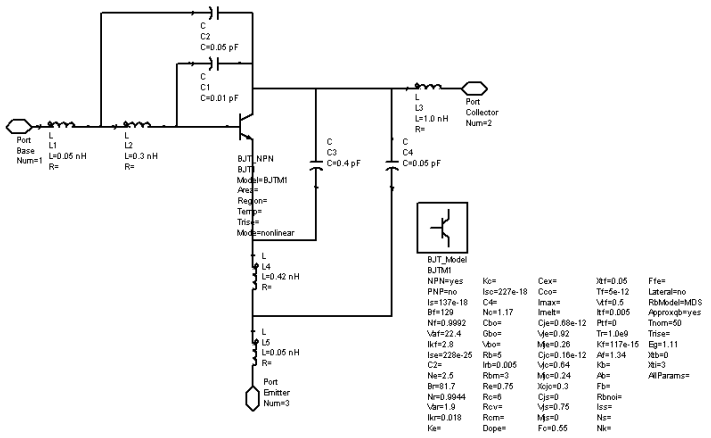


Figure 2.12: Agilent Advanced Design System (ADS) schematic showing setup for harmonic balance simulation.

both 2-port and standard topologies. The summary of simulation vs. measurement is shown in Table 2.5. Berkely Spice 2G6 models supplied by Toshiba and California Eastern laboratories shown in Fig. 2.12 and 2.13 were used. A rectangular coax model matching that of measurements as well as an equivalent RLC were used in the oscillator simulation is shown in the oscillator schematics in Fig. 2.14.

The oscillator was fabricated on Rogers 4350 as a CPW structure. A photograph of the completed circuit is in Fig. 2.15. The top CPW ground is not tied to the lower half through vias for the purpose of thermal isolation. SMA connectors do connect the grounds on this test structure but will not in the final configuration. The size of the ground is less than 1cm on a side which equates to less than $\frac{1}{10}$ of a wavelength at 4.6GHz and determined to be a reasonable ground.

Initial measurements were done using an HP 8722 spectrum analyzer. The oscillator demonstrated stability such that it could be viewed on a screen with 100kHz and 10kHz spans. The 10kHz span is shown in Fig. 2.16 with an on screen displayed noise of -60dBc with a 1kHz BW. This equates to -90dBc (10log(1kHz)) in a 1Hz BW.

A delay line discriminator phase noise measurement system described in Chapter 3 enabled free running phase noise measurements. The measured, simulated and system

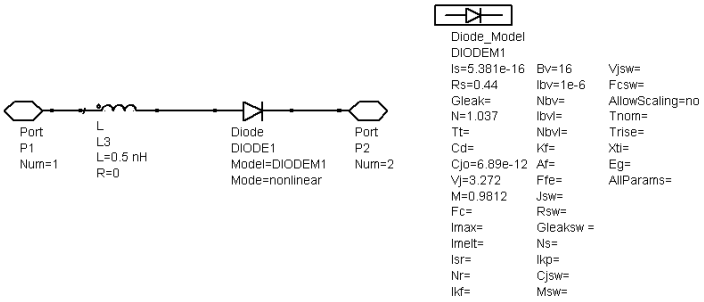


Figure 2.13: Agilent Advanced Design System (ADS) schematic showing setup for harmonic balance simulation.

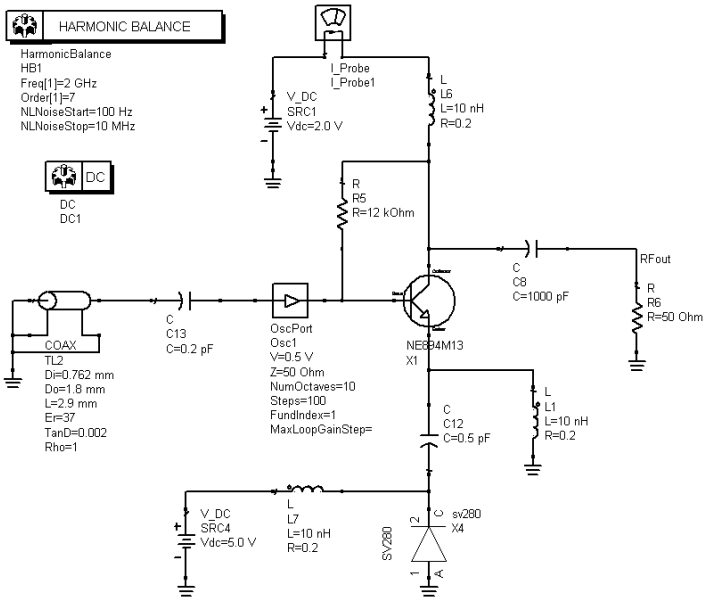


Figure 2.14: Agilent Advanced Design System (ADS) schematic showing setup for harmonic balance simulation.

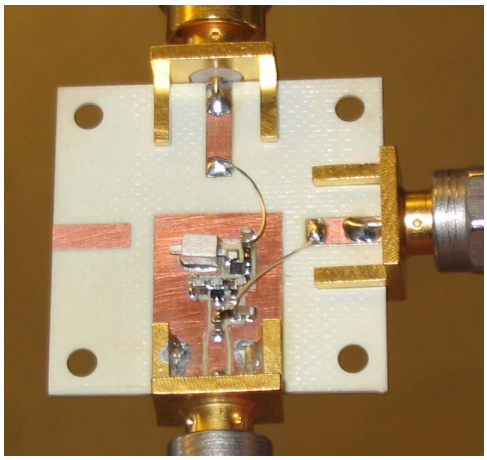


Figure 2.15: Photograph of constructed oscillator.

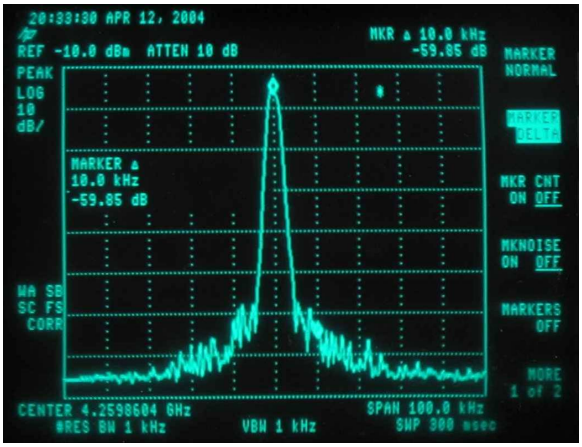


Figure 2.16: Photograph of the spectrum analyzer measurement. The spectrum analyzer reads -90dBc/Hz phase noise at 10kHz offset. This is the limit of the spectrum analyzer which motivated the design of a delay line discriminator phase noise measurement system.

Harmonic	Meas. Freq.	Sim. Freq.	Meas. Pwr	Sim. Pwr
1	4.3GHz	4.15GHz	-3dBm	-1dBm
2	8.6GHz	8.3GHz	-12dBm	-10dBm
3	12.9GHz	12.45GHz	-28dBm	-25dBm

Table 2.5: Measured vs. simulated frequency and harmonic output power.

noise floor is shown in Fig. 2.17. A simulated noise of -100dBc/Hz at 10kHz compared well with the measured noise of -102dBc/Hz. The system accuracy is estimated to be within +-2dB. The simulated results did not compare favorably at the desired 100Hz BW. The simulation model did not incorporate an accurate model of the flicker corner, which increases the phase noise at 10dB/decade from 8kHz on in measurements.

An additional 40dB/decade curve is present very close to the carrier and it is believed to be due to thermal drift during the measurement. Measurements close to the carrier can take minutes to measure and small changes in temperature are viewed as a 10dB additional increase in phase noise beginning at the inverse of the thermal time constant.

The 4.6GHz LO was locked to an atomic cell. However, prior to measurements, NIST changed the direction of the project to a Rubidium-87 reference for improved performance that operated at approximately 3.4GHz. Therefore this oscillator was mixed with a 7.6GHz synthesizer and downconverted to 3.4GHz. The resulting Allen deviation measurements are shown in Fig. 2.18. This is the very first locking of a free-running oscillator to the prototype chip scale rubidium cell. High modulation was used to ensure locking and the effects of that compared to low modulation are shown with comparable synthesizer plots.

Improvements to the oscillator design (now at 3.4GHz) and to locking to the Rubidium standard have been made by Alan Brannon in [1, 17]. The specification of 1e-11 at 1 hour of integration has been met with an oscillator with similar phase noise performance characteristics to the one demonstrated here.

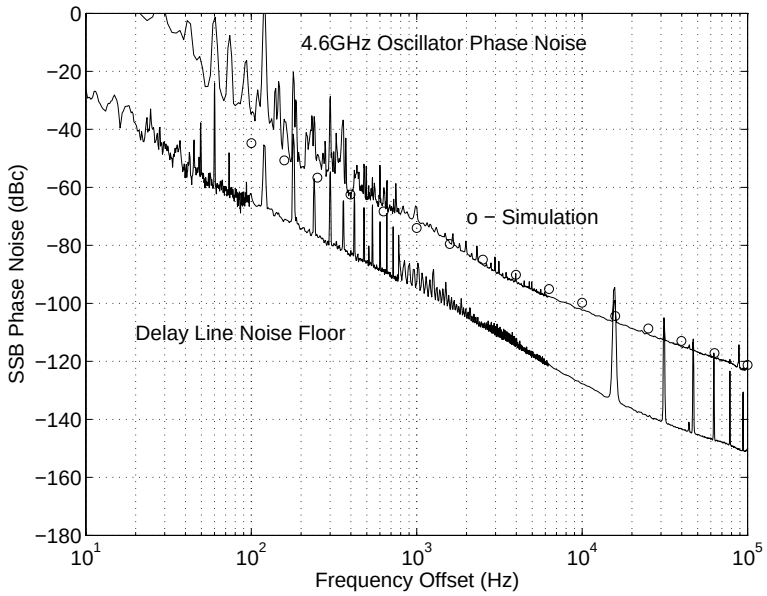


Figure 2.17: Phase noise measurements (top solid) and simulation (o) with system noise floor measurement (bottom solid).

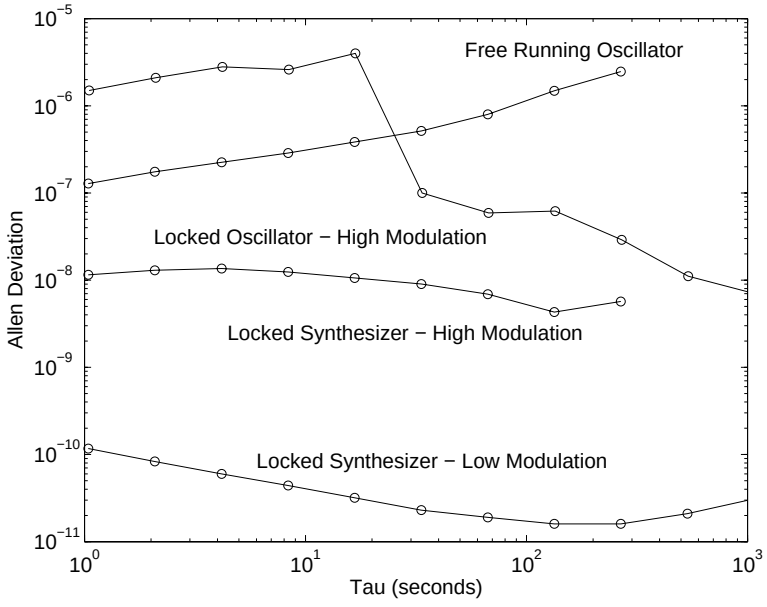


Figure 2.18: Allen deviation measurements of the CSAC-LO locked to a rubidium atomic resonance.

V_{bias}	I_c (meas)	I_c (sim)	P_{dc} (mW - meas)
2	8mA	7.8mA	16mW
1.8	7mA	5.6mA	12.6mW
1.6	5mA	4.8mA	8mW

Table 2.6: Measured vs. simulated DC power dissipation.

The final constructed oscillator was calculated to have a temperatures stability of ¡10ppm/C near 25C. [To be included]. The temperature vs. change in frequency is shown in Fig. 2.19

2.4 Chapter Summary

A 4.6GHz local oscillator for use in a miniature atomic clock has been presented. Optimization of commercial components has reduced the size and power consumptions to 1cm^2 an less than 16mW while maintaining a phase noise of -102dBc/Hz. The phase noise exhibited by the oscillator is sufficient to lock to the hyperfine transition frequency in a micro-Rubidium atomic cell.

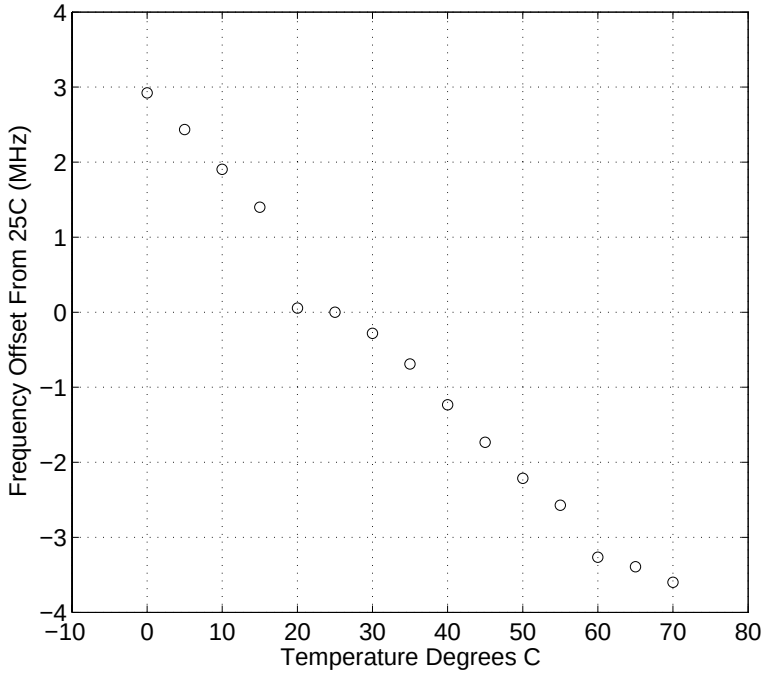


Figure 2.19: Temperature measurement of the final oscillator normalized to 25C. The oscillator exhibits an average temperature coefficient of 93kHz/C. This equates to 20ppm/C.

Chapter 3

Phase Noise Measurement Systems

3.1 Introduction to Phase Noise Measurements

The purpose of the phase noise measurement is to quantify the short term stability of an oscillator, or alternately, the added noise by a 2-port component. Phase noise measurements are perhaps the most sensitive measurements being done at microwave frequencies. State-of-the-art cross correlation systems, such as that presented in this chapter, have the ability to measure 1nV/Hz or $4 \cdot 10^{-21}$ Watts at 10kHz offset from a microwave carrier.

Throughout this thesis, five phase noise measurement systems were designed, created and optimized for specific measurements. This chapter describes five phase noise measurement systems in sections 3.2 to 3.5. In each case, the system operation and calibration is presented first, followed by possible improvements and a specific measurement example.

The five systems are referred to as:

- Delay Line Discriminator Phase Noise Measurement System
- Single Channel Additive Phase Noise Measurement System
- Frequency Translation Single Channel Additive Phase Noise Measurement System

- Cross Correlation (Dual Channel) Measurement System
- Frequency Translation Cross Correlation (Dual Channel) Measurement System

3.2 Delay Line Discriminator Phase Noise Measurement System

Several methods for oscillator phase noise measurements have been developed [25, 2], such as the delay-line and two oscillator phase locked method, each with distinct advantages. The delay-line measurement system was chosen for the flexibility in measuring a free-running oscillator between 1GHz and 10GHz. The delay-line technique has sufficient sensitivity to measure most microwave oscillators with loaded Q-factors of several hundred and does not require a second reference oscillator.

3.2.1 Operation and Calibration

Delay line discriminator measurements for oscillators were first introduced in 1966 by Tykulsky and improved by Halford in 1975 with a cross-correlation system. The delay-line system developed in this chapter is shown in Fig. 3.1. In this measurement, the oscillator output is split, one of the outputs is delayed, and multiplied in a mixer with the non-delayed path. The mixer operates as a phase-detector, translating phase changes between between the RF and LO ports to a measurable voltage at the IF. The measured voltage power spectral density is proportional to the phase noise of the oscillator.

Delay-line discriminators are limited by the loss of the delay-line. The delay line used in this system is a 12.7-mm diameter Heliax coaxial cable available from Andrews Corporation with only 0.045 dB/m/GHz of loss. The measurements presented here use a 125ns, 33meter cable with 8.9dB of loss at 4.6GHz and 14.6dB of loss at 10GHz. Measurement sensitivity is -125dBc/Hz at 10kHz offset.

The delay line discriminator phase noise measurement system, shown schemat-

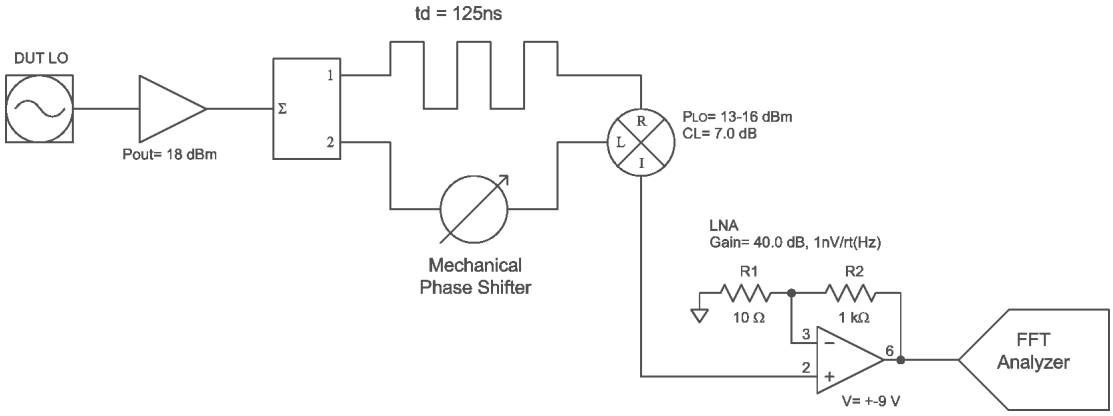


Figure 3.1: Delay-line phase noise measurement system schematic. The oscillator under test is amplified to 18dBm and split with a 3dB power divider. One branch is delayed by 125ns and phase compared against reference branch using a double balanced mixer as a phase detector. The mechanical phase shifter is used to set the system in quadrature (Mixer IF = 0V). A LNA amplifies the mixer output voltage before sampling with an FFT analyzer.

ically in Fig. 3.1 converts short-term frequency fluctuations into voltage fluctuations that can be measured with and ADC or baseband analyzer. Small frequency fluctuations of the oscillator are converted to phase fluctuations in the delay line. The phase detector converts the phase difference between the delayed path and undelayed path into a DC voltage related by the phase discriminator constant K_ϕ. The small frequency fluctuations of the oscillator are related to the phase detector constant K_ϕ and τ_d by:

$$\Delta V(f_m) = [K_\phi 2\pi\tau_d]\,\Delta f(f_m) \tag{3.1}$$

The voltage output is measured as a double sideband voltage spectral density $S_v(f_m)$. Phase noise $S_\phi(f_m)$ is related to the measured $S_v(f_m)$ by:

$$S_\phi(f_m) = \frac{S_v(f_m)}{K_d^2 f_m^2} \tag{3.2}$$

Where $K_d = K_\phi 2\pi\tau_d$. Conversion to single sideband phase noise:

$$\mathcal{L}_\phi(f_m) = \frac{S_v(f_m)}{2K_d^2 f_m^2} \tag{3.3}$$

Rewritten in terms of dB:

$$\mathcal{L}_\phi(f_m)[\mathrm{dBc/Hz}] = \mathrm{S_v(f_m)} - 3 - 20\log 10(\mathrm{K_d}) - 20\log 10(\mathrm{f_m}) \tag{3.4}$$

With a single calibration of the mixer as a phase detector, K_ϕ and known delay τ_d, the phase noise of an oscillator can be measured on an FFT analyzer. K_ϕ is in V/rad and is determined by measuring the DC output voltage change of a mixer while in quadrature (nominally 0V DC) for a known phase change in one branch of discriminator. The value of K_d is dependent upon the RF input power of the mixer. Fig 3.2 shows a range of values for K_d vs. RF input power. RF input power is directly proportional to the noise floor shown in Fig. 3.3.

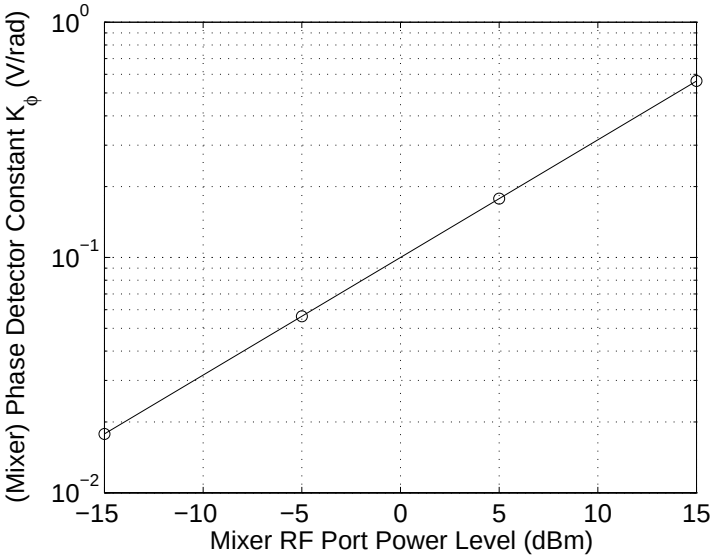


Figure 3.2: The phase detector sensitivity in terms of RF power (assuming LO power is great than RF) and phase detector constant K_Φ. Noise Floor sensitivity is 1:1 to mixer RF input power.

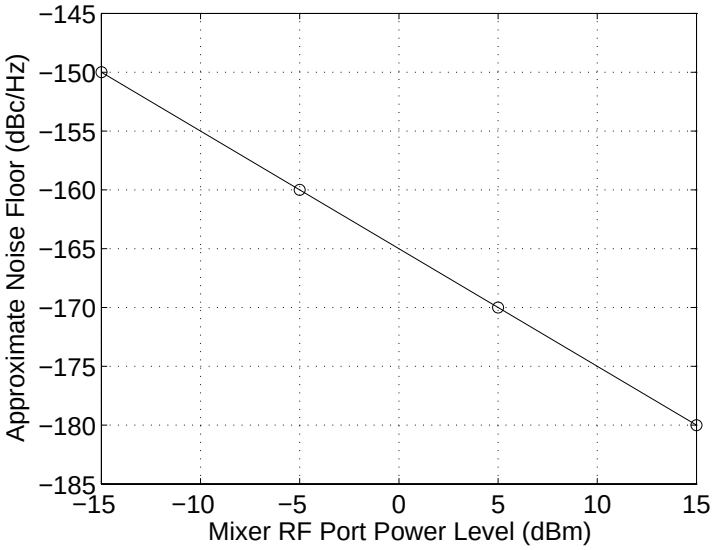


Figure 3.3: The phase detector sensitivity in terms of RF power (assuming LO power is great than RF) and phase detector constant K_Φ. Noise Floor sensitivity is 1:1 to mixer RF input power.

The sensitivity of the delay line discriminator can be determined first by introducing Q-factor as the derivative of the phase change in a resonator:

$$Q = \frac{\omega}{2}\frac{\delta\phi}{\delta\omega} \tag{3.5}$$

A coaxial delay-line has a linear phase relation with frequency across the useable bandwidth of the transmission line. Relating this linear phase relationship in a coaxial line to the derivative of the phase change in a resonator results in an effective Q, Q_E for a transmission line with time delay τ_d:

$$Q_E = \pi f_0 \tau_d \tag{3.6}$$

The effective Q-factor increases linearly with both delay line length and frequency of operation. Using Q_E as the Q-factor in Leeson's equation from 1.12 and using an approximate mixer noise floor of -170dBc. The flicker corner is set at 10kHz, typical for a silicon diode mixer. The measurement phase noise floor using a 125ns and 250ns delay line is shown in Fig. 3.4, calculated from:

$$\mathcal{L}_\phi(f_m) = 10\log_{10}\left[\left(1+\frac{1}{(2\pi\tau_d f_m)^2}\right)\left(1+\frac{f_c}{f_m}\right)\right] + N_{mixerfloor} \tag{3.7}$$

The digitization of the mixer output voltage is completed by a Stanford Research Systems SR760 FFT Analyzer which requires the addition of an LNA due to the insufficient sensitivity of the analyzer. An op-amp from Analog Devices, part AD797, in a non-inverting configuration and gain of 40dB is used as a pre-amplifier, shown in Fig. 3.1. The input voltage noise is 1nV/Hz with a flicker corner of 100Hz. The non-inverting input is a 2kΩ resistor to ground. Several values were tested for phase detector optimization [26]. Above 2kΩ, the phase detector sensitivity did not improve but the input offset current of the AD797 produced a significant voltage output offset. Below 500Ωs, the phase detector sensitivity was reduced by up to a few dB.

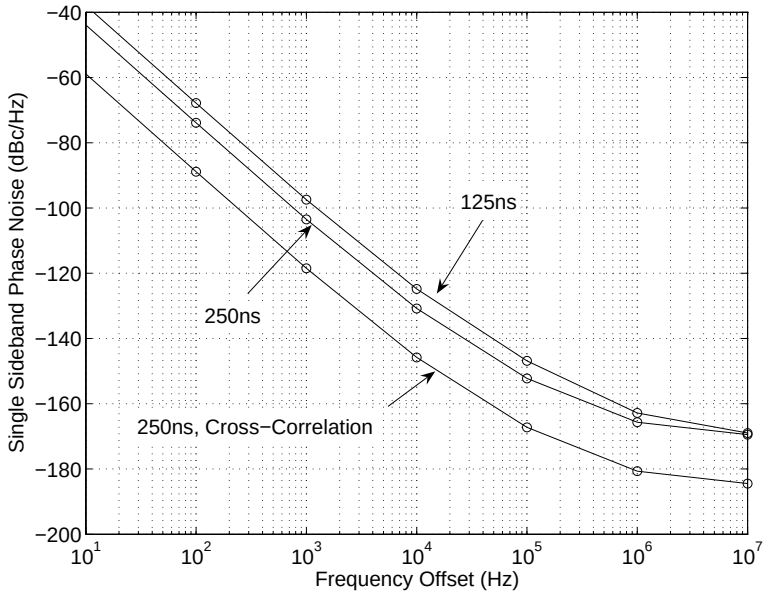


Figure 3.4: Phase noise floor of a delay line system. The phase noise of the oscillator under test must be approximately 6dB above this for an accuracy of 1dB.

3.2.2 Delay Line Measurements and Improvements

The 4.6GHz oscillator presented in Chapter 2 was measured using the delay line technique. The oscillator RF output power of -2dBm was amplified to 18dBm using an HP power amplifier. A microstrip wilkinson power divider was designed to split the signal at 4.6GHz with 20dB of isolation. A Marki Microwave M8-0420 7dBm mixer was used as a phase detector. The lower trace is the noise floor of the system measured using the designed oscillator as the reference.

If the delay line has significant loss, the delayed signal level at the mixer, reducing the sensitivity of the measurement. The optimum sensitivity of a delay line system is achieved when the loss of the delay line is approximately 8.7dB [2]. In the case where a long delay is required for sensitivity, unequal power splitting can be used ensure the RF port of the mixer receives sufficient power to provide a low noise floor. For example, assume a mixer requires an LO power of 13 dBm and the delay line has 18.7 dB of loss while the optimum delay loss is approximately 8.7 dB [2]. Instead of using a 3 dB power divider, a 10 dB coupler can be used with the -10 dB coupled port driving the LO and the main path attached to the delay line. The input power required is 23dBm vs 16dBm previously, with an increase in sensitivity of 10dB.

The measurement noise floor is directly proportional to the mixer noise floor from Eqn: 3.7. The dual-channel cross correlation system introduced later in this chapter may be used to reduce the noise due to the mixers by an additional 15dB with 1000 averages. With a delay line of 250ns and a 15dB reduction in noise floor, the delay-line system sensitivity at 10kHz offset is -145dBc/Hz shown as the lowest plot in Fig. 3.4

3.3 Single Channel Additive Phase Noise Measurement System

The system presented here is a phase discriminator measurement system used to characterize the additive or residual phase noise of a two port device. Two port

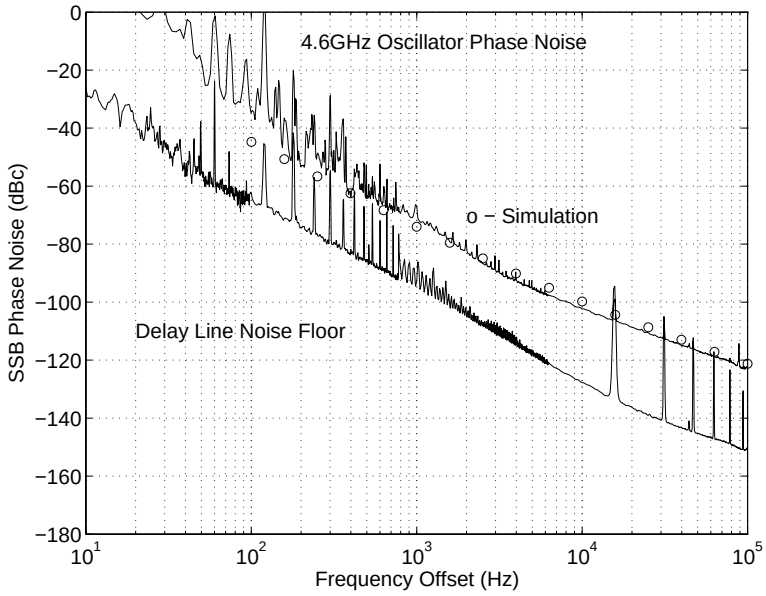


Figure 3.5: Measured phase noise of the 4.6GHz oscillator from Chapter 2. Simulations are done in ADS using available SPICE models which do not adequately model the flicker corner. The lower plot is the measured noise floor of the delay-line system with 125ns delay.

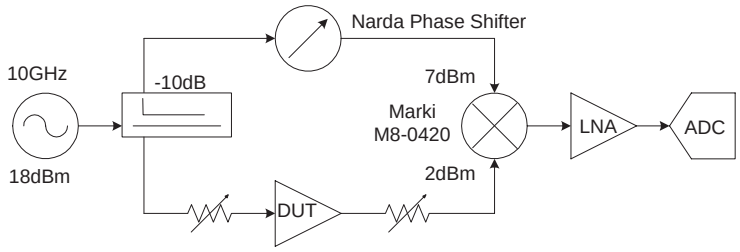


Figure 3.6: Single channel additive phase noise measurement system used to characterize the additiv ephase noise of in class-E and class-A amplifiers at 10GHz.

devices may include amplifiers, filters, isolators, etc. Additive phase noise of frequency translation devices such as multipliers, dividers and mixers may also be measured but will be discussed in the next section.

3.3.1 Operation and Calibration

The system shown schematically in Fig. 3.6 measures the added phase noise of an amplifier. The noise due to the oscillator are correlated and canceled at the phase detector. Noise due to the amplifier is uncorrelated and measured as additive phase noise [27].

Mixers have the ability to cancel only a finite amount of source phase noise. The available HP83620 synthesizer exhibited too high of a phase noise level and a sufficient noise floor could not be achieved. A custom 10-GHz source is designed as shown in Fig. 3.7 to provide a source with higher spectral purity.

To create a 10GHz output, A 100 MHz Wenzel Sprinter crystal oscillator is multiplied using a LPN7100 comb generator from Picosecond Pulse Labs (PSPL). The 2 GHz harmonic is bandpass filtered to create an intermediate frequency and amplified by a Hittite HMC479 SiGe amplifier. A second comb generator from PSPL, model LPN7103, yields harmonics past 10 GHz. The 10 GHz harmonic is bandpass filtered and amplified first by a Hittite HMC462 broadband LNA (NF=2.5 dB) and then by a HP8449B power amplifier (Pout=18dBm).

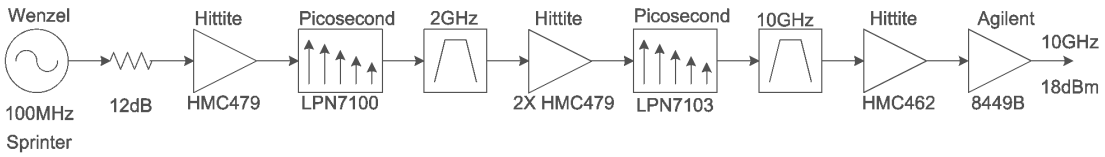


Figure 3.7: Custom 10GHz source schematic. Two stages of frequency multiplication were used to reject nearby harmonics.

The phase noise of the custom 10 GHz source is measured using the 125ns delay line discriminator described previously. The delay-line measurement offers a very good noise floor far from the carrier but the measurement is limited in sensitivity close to the carrier for this application. The measured phase noise is shown in Fig. 3.8 and compared to a HP83620A synthesizer at 10 GHz. At 100 kHz offset, the phase noise of the multiplied oscillator is measured to be -123 dBc/Hz, only 2dB higher than theoretical 20logN multiplication of the 100MHz oscillator.

In the case of MESFET amplifiers, it is desirable to measure phase noise at high carrier offset frequencies. A custom FFT analyzer was designed using a Picotech 12Bit ADC with a memory of 64kB per channel. The memory depth limited the amount of data taken over a given time. Two ADC channels were used to measure both low and high offset frequencies without reconfiguring the system as shown in Fig. 3.9. The amplification was broken into two stages to increase the bandwidth of the LNA to 2MHz. A total gain of 60dB is required to overcome the noise floor of the ADC.

The single sideband phase noise is proportional to the measured voltage spectral density at the output of the mixer by the relation:

$$\mathcal{L}_\phi(f_m)[\mathrm{dBc/Hz}] = \mathrm{S_v(f_m)} - 20\log 10(\mathrm{K_d}) - 3; \tag{3.8}$$

The calibration constant K_d is V/rad is measured by introducing a known phase shift in one branch of the system and measuring the output voltage of the mixer. Typical values of K_d (previously listed as K_ϕ for the delay-line) and noise floor based on RF

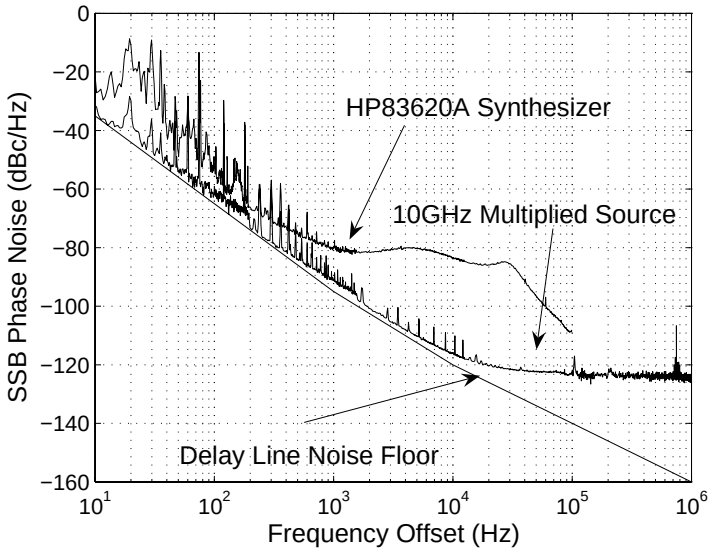


Figure 3.8: Delay line measurements of the custom 10GHz source demonstrating a noise floor of -123dBc/Hz at 100kHz offset as compared to an HP83620A synthesizer at 10GHz.

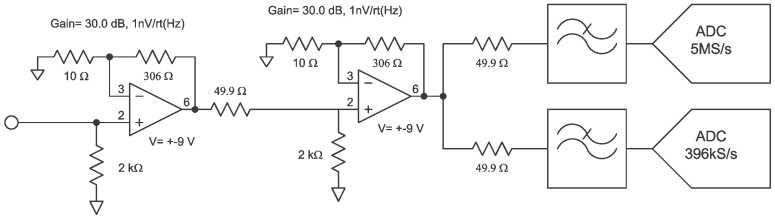


Figure 3.9: Schematic of the LNA used for 10Hz to 1MHz measurement. The Picotech ADC has limited buffer size requiring both channels to be utilized to cover the entire band.

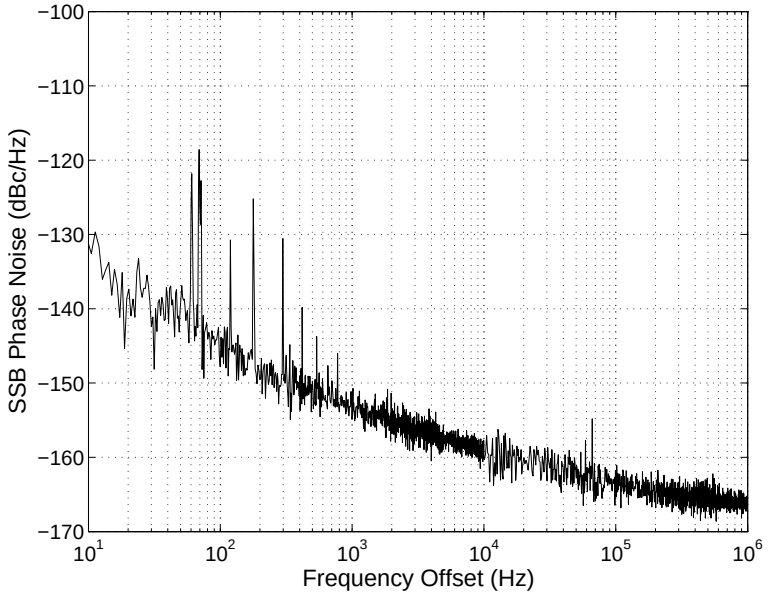


Figure 3.10: The additive measurement noise floor at 10GHz.

input power are shown in Figs. 3.2 and 3.3.

An improved calibration method is introduced in this measurement. A switched delay line of known delay difference is used. Two coaxial relays with only 0.2dB loss each are used to switch between two coaxial lines with a broadband delay difference of 9ps. This small delay allowed accurate calibration from near DC to 18GHz.

3.3.2 Measurements and Improvements

The measured residual phase noise floor of the system shown in Fig. 3.10 demonstrates the measurement sensitivity to be -164dBc/Hz at 100kHz offset. The system noise floor is determined by the ability of the mixer to cancel the oscillator phase noise in relation to the drive level of the mixer. A Marki Microwave M8-0420 Level 7dBm mixer was chosen based on the isolation characteristics and low conversion loss. A higher level mixer will improve the noise floor proportionally. The system noise floor of -164dBc/Hz was sufficient to measure the Class-E PA additive phase noise.

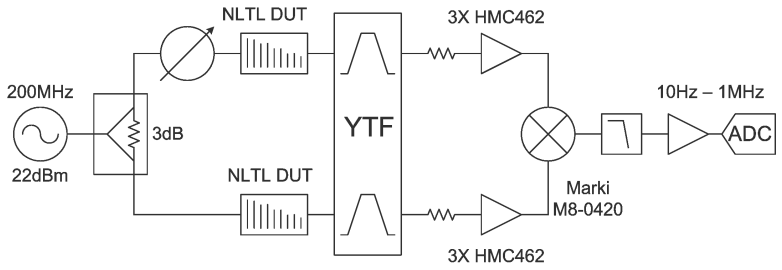


Figure 3.11: Additive phase noise measurement system showing a pair of NLTLs being measured. A dual YIG-tuned filter selects the harmonic and ammplified with 39dB of gain using 3X HMC462 amplifiers. Phase comparison is accomplished using a Marki Microwave M8-0420 mixer and the baseband amplifiers and ADC from the 10GHz system.

3.4 Frequency Translation Single Channel Additive Phase Noise Measurement System

Frequency translation devices, usually multipliers or dividers, are measured similarly to amplifiers but require a more complicated system. When measuring frequency translation devices, a pair of device must be measured to keep the RF and LO ports of the mixer at the same frequency. Phase noise measurements are as yet undefined for phase detectors operating at harmonically related frequencies. The schematic of the system discussed in this section is shown in Fig. 3.11.

3.4.1 Operation and Calibration

Measurement of two devices assumes that the noise processes are independent and uncorrelated. The magnitude of the noise may not be identical. The noise of either device will not be greater than that measured for a pair of devices. However, if all noise is due to one device, then the noise performance of the second device is lower but unknown to what extent. Three devices measured interchangeably can reduce this error to 1-2dB. It has been found that frequency multipliers of a given design are consistent from device to device to within 1-2dB.

The highest frequency multiplication harmonic measured to date is no more than

the 11th harmonic described in [28, 29]. The measurement system presented here is designed to measure up to the 90-th harmonic (18GHz) with a 200MHz fundamental. The comb spacing is 200MHz apart across the entire 200MHz - 20GHz output of the NLTL. A Yttrium-Iron-Garnet (YIG) tunable filter (YTF) was used to select the desired harmonic. With a -3dB bandwidth of only 20MHz, rejection at 200MHz from the center of the passband was 50dB between 1GHz to 18GHz shown in Fig. 3.12. As a magnetically sensitive device, any stray magnetic fields such as power lines, motors or generators can create noise close to the carrier. Additionally, a YTF can be temperature sensitive and must have a good heatsink with feedback thermal control. The devices are current controlled and noise in the drive circuitry can lead to additive phase noise in the YTF.

To reduce this effect, a dual YTF was purchased from Micro Lambda Inc. The dual filter simultaneously tunes two YIG elements with the same magnetic field, making any magnetic or current noise common to both paths. Common mode noise is canceled in the phase detector.

In practice, two factors contributed to problematic noise. First, the two YIGs did not track well enough for our purposes as shown in Fig. 3.13. While the 3dB pass-bands did overlap, the group delay across each filter was flat for only 1-2MHz of the bandwidth and proved difficult to find. If one filter was at a point where the derivative of the group delay was greater than zero, the noise at offset frequencies of 1kHz or less increased at 20dB/decade. The second contribution came from the temperature control circuit. The temperature is feedback controlled via an on-off switch and if transitioned during a measurement, contributed significantly to close to the carrier noise. Removing the temperature control is not an option because the tuned center frequency of the YTF would change if the temperature drifts.

The output power of the NLTLs at high harmonics is -20dBm to -30dBm with a loss of 4dB in filtering and cabling. The filtered harmonic harmonic must be amplified up

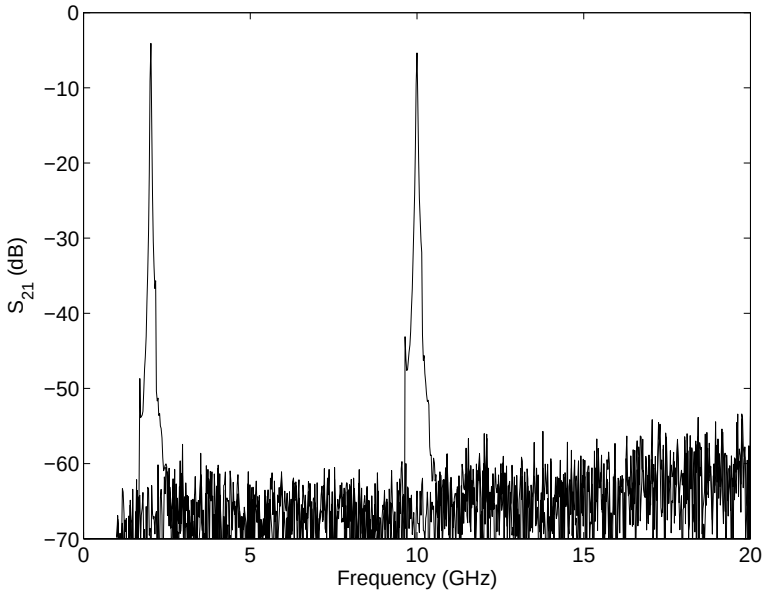
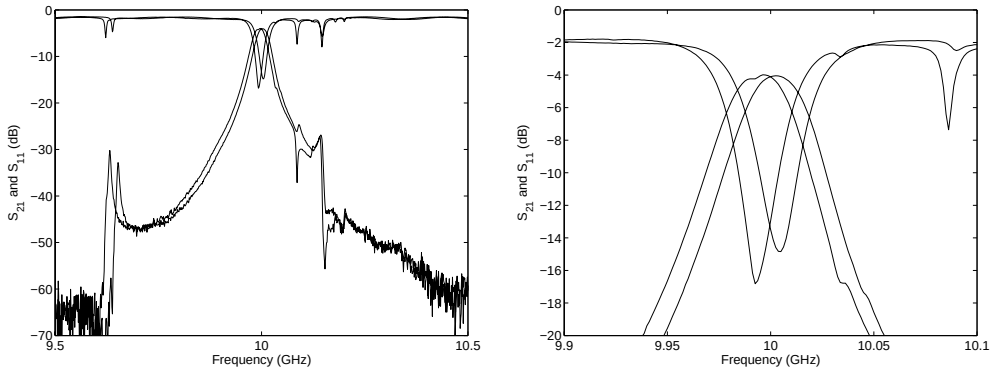


Figure 3.12: YIG-tuned filter wideband response with 2GHz and 10GHz responses plotted on the same graph. The response is spurious free to -50dB.



(a) (b)

Figure 3.13: Narrowband response of the dual-YIG tuned filter at 10GHz. Slight offset in passband frequencies causes a group delay problem. A small range of 2MHz is common between the two passbands where the group delay is flat and good measurements can be achieved.

to 7dBm for proper operation of the phase detector. Broadband amplification is required to operate the system from the desired 2GHz to 18GHz. Three Hittite HMC462 traveling wave LNA's totaling 39dB of gain were used per channel with appropriate attenuation prior to the first amplifier. The amplifiers contain an internal bias control network that degraded the phase noise and is shown in Fig. 3.14. The additional flicker noise affected sensitivity close to the carrier and was a dominant source of noise in the measurement.

3.4.2 Measurements and Improvements

The YIG-tuned filters were included in the system noise floor measurement. In order to measure the noise of the system at the desired harmonic, an NLTL, described in detail in Chapter 5, is placed prior to a broadband 6dB power splitter to create harmonics to 20GHz, schematically shown in Fig. 3.15. The noise due to the oscillator and NLTL combination are common mode and canceled in the phase detector. Measured noise is due only to the system.

The system noise floor at 8GHz is shown in Fig. 3.16. For direct additive phase noise to noise floor comparison, the NLTLs were driven such that the comb power of the desired harmonic matched that of the NLTL additive phase noise measurement. The system sensitivity is highly dependent on the amount of power entering the YIG at a given harmonic.

It is concluded that YIG-tuned filters are a good method to measure additive phase noise of high harmonics at frequency offsets greater than 1kHz. However, the dual YIG was not precisely matched to be useable in a general test system. Measurements took several hours to because of YIG related issues. Two independent YIG-tuned filters with a linear feedback temperature control may be optimal.

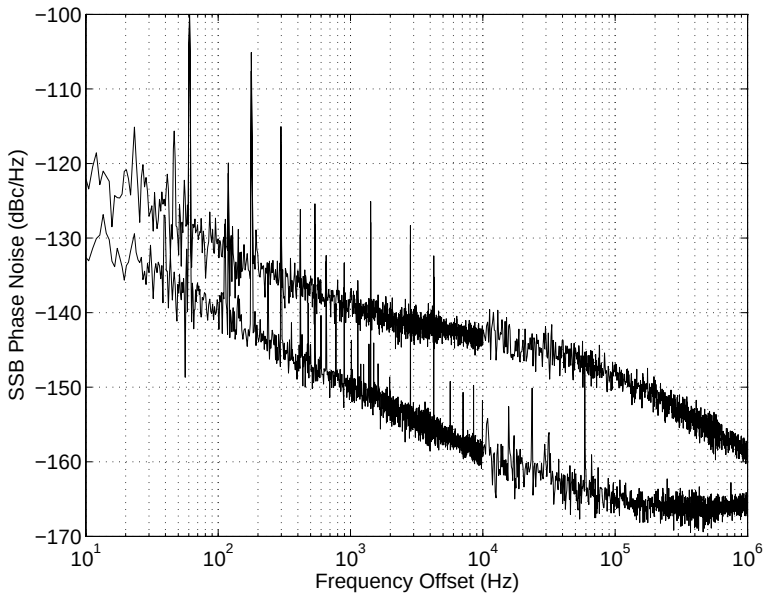


Figure 3.14: The spectral performance of the Hittite HMC462 broadband low noise amplifier. The phase noise increase centered around 10kHz is believed to be from an active bias circuit. The lower trace is the measurement system noise floor

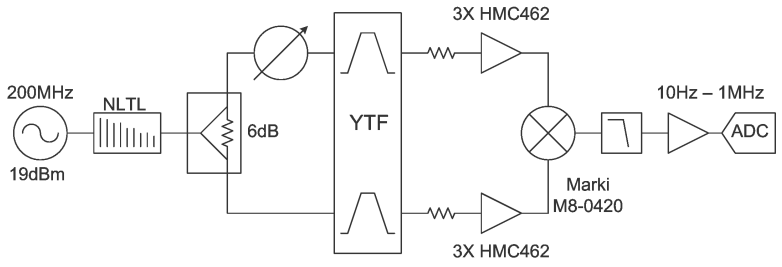


Figure 3.15: Schematic of the setup used to measure the noise floor of the YIG-tuned system. The NLTL is used to create harmonics prior to splitting the signal with a broadband (DC-18GHz) 6dB resistive power divider. The noise due to the YIG-tuned filter, post amplification, mixer and baseband amplification may then be characterized.

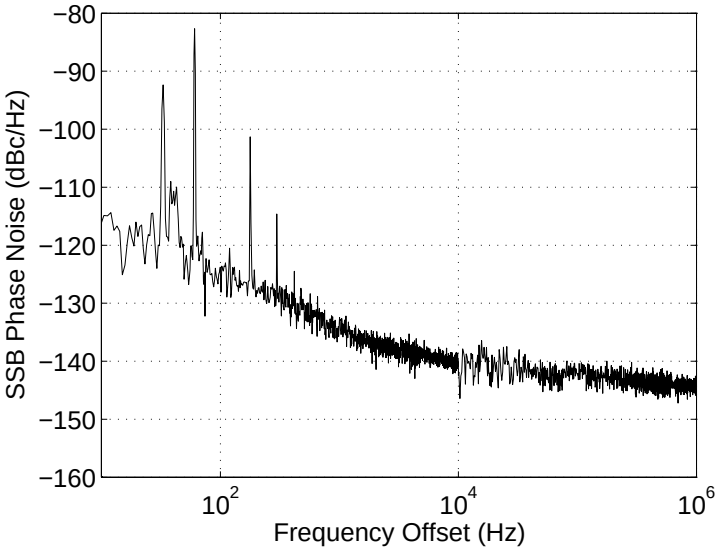


Figure 3.16: Noise floor of the system (3dB subtracted assuming path noise is identical). Below 1kHz, noise is dominated by flicker noise of the HMC462 amplifiers. Above 1kHz, the noise is limited by the signal power level from the filter and noise figure of the amplifiers.

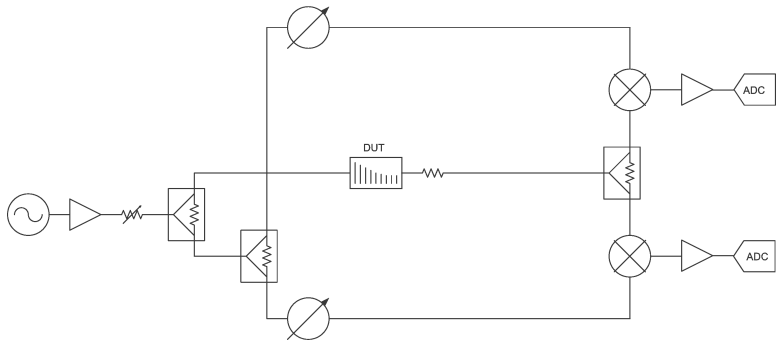


Figure 3.17: A two-channel cross-correlation measurement system. The source is split to three paths. Noise due to the mixers is uncorrelated while noise added by the DUT (common path) is correlated. Using data sampled simultaneously at the output of the two mixers, statistical cross-correlation identifies noise only common to the two mixers, the noise of the DUT.

3.5 Cross Correlation (Dual Channel) Measurement System

The single channel (one mixer) additive phase noise measurement system described in the last section exhibits more noise than the components being analyzed. The dominant source of noise is the flicker noise of the post amplifiers and sensitivity of the mixers, neither of which can be improved significantly. A two channel system (two mixers) using cross-correlation is capable of removing the uncorrelated noise sources due to mixers and post amplifiers. The schematic of the system used to measured the added noise of an amplifier is shown in Fig. 3.17 [30, 31, 32].

3.5.1 Operation and Calibration

Cross correlation is a standard method of estimating the degree to which two series are correlated. The two series being cross-correlated in this system are the sampled time domain waveform at the output of the two mixers. The series, called a sample, is vector averages with N samples. Uncorrelated noise is reduced by the relation $5 \log 10(N)$ while correlated noise remains at the same level. For every ten-fold increase in samples, the uncorrelated noise is reduced by 5dB. 1000 averages are required for a 15dB improvement in the noise floor. It is beneficial to improve the single channel measurement as much as

possible before applying cross correlation to reduce the required number of samples and measurement time. To measure frequency offsets down 10Hz, 1 second of continuous data is required per sample. After including data processing, it may take 1 hour to take a single phase noise measurement from 10Hz to 20kHz with 1000 averages.

Baseband digitization is the greatest difference in the single channel vs. dual channel systems. The cross-correlation system requires a uninterrupted time series related to the offset frequencies of interest for each channel and each sample. The Picotech ADC used in the previous systems did not have enough memory to allow a reasonable range of offset frequencies during simultaneous sampling. Alternatively, a USB audio card was used to measure from 10Hz to 20kHz. 20kHz was chosen as a reasonable upper limit to phase noise measurement from specification of the available oscillators. By 10kHz offset, high performance oscillators have reached the white phase noise floor and are flat in power spectral density from 10kHz to 1MHz offset. If the frequency multipliers are as spectrally pure as desired, the additional noise from the frequency multiplier must also be flat past 10kHz.

Both channels on the audio card were operated simultaneously at a f_s=96kHz rate with 2^{16} data points per sample, for approximately 0.68seconds of data per sample. The Fourier resolution is 1.46Hz per bin. The voltage input range on an audio card varies between manufacturers. The 5V, 1kHz calibration signal available on a Tektronix oscilloscope was used as a calibration standard as shown in Fig. 3.18 to determine appropriate scaling of the amplitude data.

The gain stage prior to the audio card is the same used in the previous systems. A gain of 60dB was sufficient to overcome the noise floor of the audio card. The audio card has two distinct advantages over the 12-bit ADC used in the single channel system. First, audio cards are available in 16-bit and 24-bit, allowing greater dynamic range, reducing the likelihood of requiring alternate gain stages. The second advantage is an audio card uses delta-sigma analog to digital conversion. The delta-sigma converters are

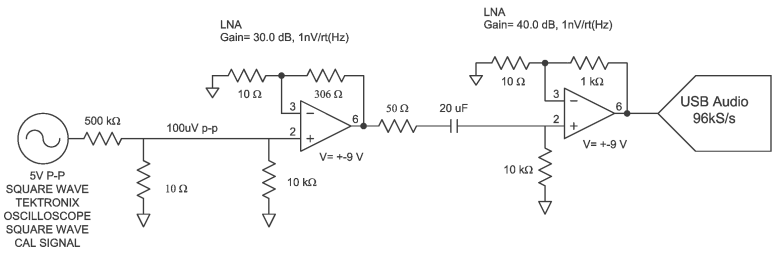


Figure 3.18: Calibration of low noise amplifier chain and ADC.

over-sampled systems and have a digital anti-aliasing filter built in. This eliminates the need for filtering after the LNA. Additionally, the anti-aliasing filter tracks the sample rate if lower sample rates are desired, eliminating aliasing problems.

Matlab software was written using the 'wavrecord' function and 'xcorr' function from the DSP toolbox. To test the baseband system, two LNAs were constructed and a separate 50Ω resistor is placed at the input of each LNA. Each channel measured approximately -177.5dBV/Hz shown in Fig. 3.19. The cross correlation of the two, after 1000 averages, is 15dB below that of either channel at 192.5dBV/Hz shown as the bottom trace in Fig. 3.19. The two 50Ω resistors and amplifiers are independent noise sources and uncorrelated, consistent with the measurements. Measurements with averages of 10, 100, 1000 and 10,000 were completed for the uncorrelated case. The noise floor improved by 5dB in each case.

A 50Ω resistor was then placed in common between the two LNAs. The noise measured by each LNA is 177dBc/Hz. The noise due to each LNA is uncorrelated and only the noise due to the resistor common to the two amplifiers is correlated. The measurements are shown as the second trace in 3.19 at -180.5dBV/Hz. The predicted value of a 50ohm resistor at room temperature is -181dBV/Hz. The results concluded the baseband processing is working as expected, to within an error of 0.5dB while measuring 0.9nV/Hz.

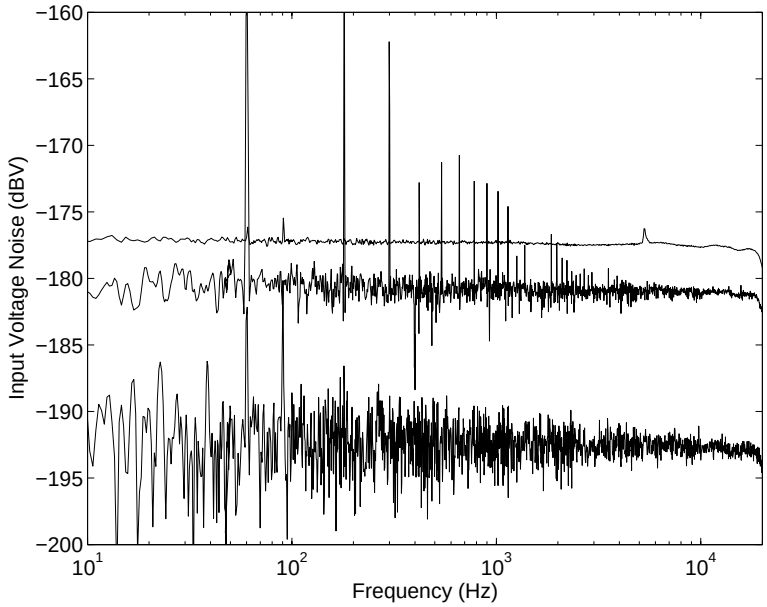


Figure 3.19: Baseband voltage noise (dBV) of the two LNA demonstrating the cross-correlation function. The highest curve is the measured voltage spectral density of either LNA with a 50ohm resistor. The second curve is the cross-correlation measurement using two LNAs, two ADC channels and a 50Ω resistor in common. The measured average noise of -180.5dBV/Hz is only 0.5dB higher than theoretical. The bottom curve is the cross-correlation measurement using two LNAs, two ADC channels and two separate (uncorrelated) 50Ω resistors, demonstrating a 15 dB improvement in sensitivity with 1000 averages.

3.5.2 Measurements and Improvements

The cross-correlation system was characterized at 200MHz. The results of which are shown in Fig. 3.20. The top trace is the noise floor of a single channel at -172dBc/Hz at 10kHz offset. The cross-correlated noise floor is -187dBc/Hz at 10kHz offset demonstrating a 15dB improvement with 1000 averages. This system was used to measure a power amplifier in Chapter 4 that exhibited a phase noise of -176dBc/Hz, 4dB below that of a single channel system. It was again used to measure the noise at the fundamental frequency for NLTLs and SRDs in Chapter 6. Once again, high level mixers may be used to improve the noise floor of the single channel, and thus the dual channel system. Using level 13dBm mixers, this system is currently state-of-the-art.

3.6 Frequency Translation Cross Correlation (Dual Channel) Measurement System

The dual channel cross-correlation system may be adapted for use in frequency translation devices.

3.6.1 Operation and Calibration

Recalling that a single channel system requires two devices, one for each path. The two-channel system requires three devices. The advantage using the cross-correlation measurement is the additive phase noise of only the device common to both mixers is correlated. The noise due to the devices in the other two paths is uncorrelated. Again the assumption must be made that the noise process of each device is uncorrelated and magnitude approximately equal. This was established to be true by measuring multiple devices. The frequency translation cross-correlation system developed is shown in Fig. 3.21.

The lessons learned from the single channel system is post amplification requires high spectral purity amplifiers and the filters should be fixed frequency passive compo-

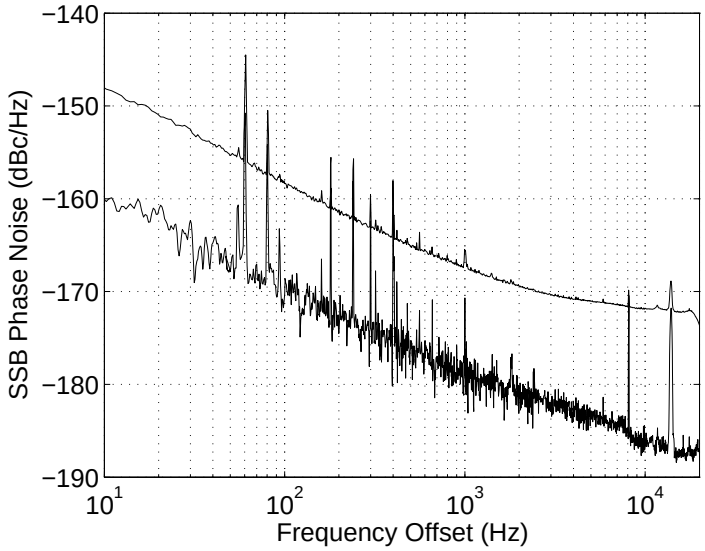


Figure 3.20: Measurement noise floor of the cross correlation system at 200MHz. The top trace is that of one channel in the cross correlation system. The bottom trace is the noise of the cross-correlation analysis of the two channels.

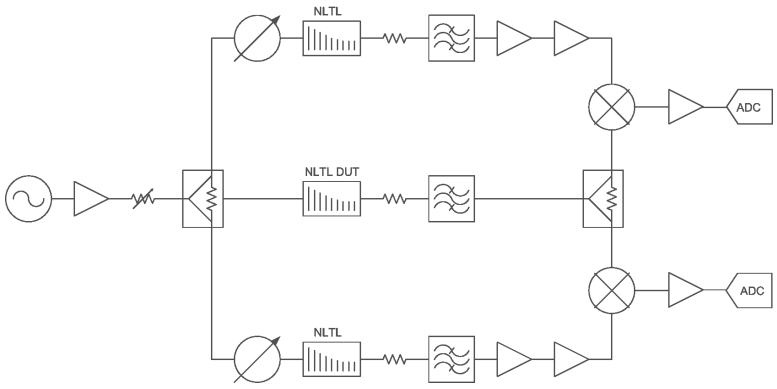


Figure 3.21: A frequency-translation cross-correlation system. Three nearly-identical NLTLs are used to create harmonics. The 10th harmonic (2GHz) is filtered in each branch. Using cross-correlation, the noise due to the NLTL in the central path is determined.

nents to avoid additional noise contribution. Post amplification was accomplished using a Hittite HMC479 broadband SiGe HBT amplifier. The spectral performance measured at 200MHz is shown in Fig. 3.22. The HMC482, a higher power version of the amplifier, has nearly the same phase noise at lower power levels but increases drastically near 1dB compression. The HMC479, up to 1dB of compression, continues to provide adequate spectral purity.

The 10th harmonic was chosen to be measured using this system by the performance obtainable in microstrip filters. A 5th order, 2GHz microstrip filter on Rogers 4350 substrate was designed and measured to reject harmonics at 1.8GHz and 2.2GHz by 50dB with only 2dB of loss. Experimentation prior to this determined that harmonics at greater than -20dBc begin to affect measurement in unpredictable ways. In the time domain, nearby harmonics can create an beatnote or amplitude variance, reducing the effectiveness of the mixer as a phase detector. It was found that harmonics below 35dB had virtually no effect on single channel system performance. The filters were designed with a goal of 50dB to reduce the chance that the harmonics may interfere in the cross-correlation measurement.

Calibration of a cross-correlation system is the same as a single channel system but with two phase detector constants, one for each mixer. The best calibration was achieved using the 9ps switched delay line in the common path and measuring ΔV at the output of each mixer to determine K_{d1} and K_{d2}.

3.6.2 Measurements and Improvements

A phase noise measurement using this system is shown in Fig. 3.23. Three NLTLs are measured at the 10th harmonic. The output power is low, reducing the sensitivity of a single channel to -150dBc/Hz. The cross-correlation system improves this by 15dB, allowing an accurate measurement of the added phase noise of the NLTL. Currently, no improvements are planned for this system. In this situation, a high drive level mixer

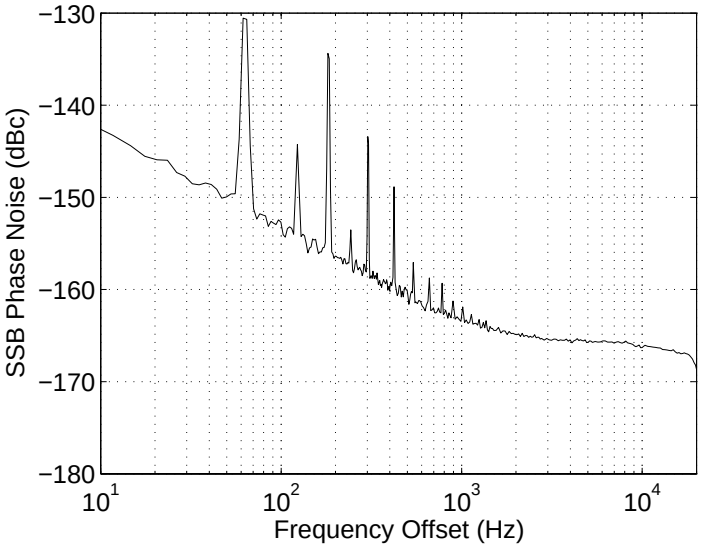


Figure 3.22: Phase noise measurements at 200MHz of the HMC479 used for amplification after filtering in the cross-correlation system.

does not improve sensitivity because the RF power is already so low. Increasing LO drive level only improves system performance if the RF level can be similarly increased.

3.7 Chapter Summary

Five measurement systems have been presented with results summarized in Table 3.1. The last 3 rows contain contributions that are for the first time described in this thesis.

Measurement System	Noise Floor	Validation Circuit
Delay Line Discriminator Phase Noise Measurement System	-125dBc/Hz @10kHz f_0 = 1GHz-10GHz	4.6GHz LO -102dBc/Hz @10kHz
Single Channel Additive Phase Noise Measurement System	-164dBc/Hz @100kHz f_0 = 10GHz	Class-A PA -157dBc/Hz
Frequency Translation Single Channel Additive Phase Noise Measurement System	-142dBc/Hz @100kHz f_{meas} = 2GHz - 8GHz f_0 = 200MHz Input	NLTL (8GHz) -142dBc/Hz @10kHz
Cross Correlation (Dual Channel) Phase Noise Measurement System	-186dBc/Hz f_0 = 200MHz	Class-AB PA f_0 = -176dBc/Hz
Frequency Translation Cross Correlation (Dual Channel) Phase Noise Measurement System	-165dBc/Hc f_0 = 200MHz f_{meas} = 2GHz	NLTL (2GHz) -152dBc/Hz

Table 3.1: Measured vs. simulated frequency and harmonic output power.

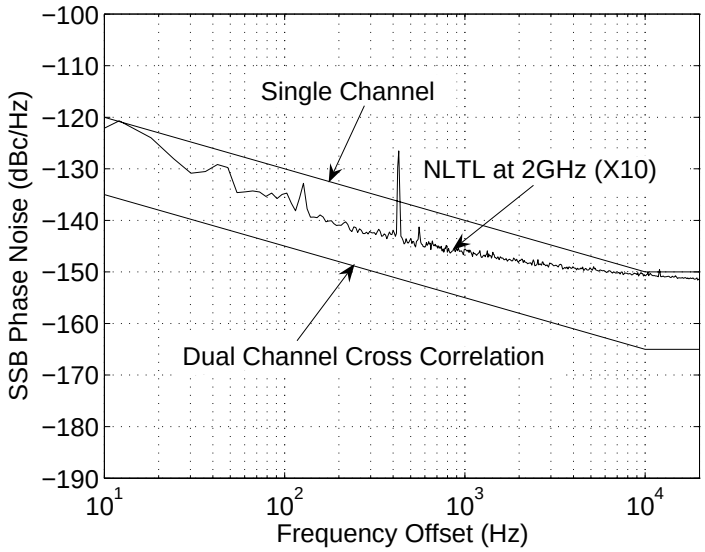


Figure 3.23: Phase Noise Measurements at 2GHz using the dual channel frequency translation measurement system. The top trace is the approximate noise floor of a single channel system with RF drive of -10dBm (output of NLTL after filter) and the bottom trace is the approximate noise floor of the dual channel system. The NLTL has sufficiently low phase noise to be measured by a cross-correlation system.

Chapter 4

Additive Phase Noise in Low-Noise and High-Efficiency Power Amplifiers

4.1 Introduction

Additive, otherwise known as residual, phase noise has been characterized in microwave linear amplifiers [33, 34, 35, 36]. There has been limited characterization of additive phase noise in saturated power amplifiers. In [37], the phase noise of a 50% efficient saturated 4.6-GHz MESFET PA is shown to have an 11 dB increase in phase noise compared to the same circuit in class-A bias.

Added phase noise is typically dominated by the flicker (1/f) noise of the device [7, 6]. Data from this thesis demonstrates a correlation between drain voltage to S_{21} phase measurements and added phase noise in class-E PAs as compared to class-A PAs using the same active devices. Moreover, it is shown that MESFET devices may tend to have better spectral purity than HBTs due to a reduced AM-PM effect when driven into large signal.

4.2 Class-E Amplifiers

In a variety of applications which require stable frequency and good selectivity, such as Doppler radar and phase-modulated communications, phase noise of the primary oscillator is critical [38, 39]. Oscillator noise is however only one element in the overall system phase noise. The analog front end chain almost without exception contains

amplifiers, which also add noise close to the carrier. This noise component is often referred to as additive or residual phase noise and is typically dominated by the flicker (1/f) noise of the device [40].

Additive phase noise has been characterized in microwave linear amplifiers [33, 34, 35, 36]. However, there has been limited characterization of additive phase noise in saturated power amplifiers. In [37], the phase noise of a 50% efficient saturated 4.6-GHz MESFET PA is shown to have an 11 dB increase in phase noise compared to the same circuit in class-A bias. High-efficiency amplifiers operating in switched mode have lately been studied extensively in the microwave frequency range [41], as well as at lower RF frequencies [42]. These PAs have been proposed for radar and high-power communications transmitters [43], in which case the additive phase noise is a significant parameter of interest.

Measurements from [44] show a significant S_{21} phase change across bias conditions. The nonlinearity of capacitance to drain voltage may affect phase noise as AM-PM conversion within the amplifier in large signal condition. The goal of this work is to quantify and compare the additive phase noise of high-efficiency and linear PAs implemented with both FET and HBT devices at X-band.

4.2.1 Power Amplifier Design

For additive phase noise comparison, both class-A and high-efficiency saturated PAs are designed with Skyworks GaAs MESFETs and Northrop Grumman InP DHBTs. The class-A PAs are standard conjugate match designs. The high-efficiency amplifiers are designed to operate in switched class-E mode, following simplified ideal-switch theory backed by load-pull measurements [45]. In the ideal switch model, the transistor is treated like an ideal switch with a shunt capacitance. For design, the output capacitance of the device is found from the s-parameters at the appropriate bias point. In practice, the switch is driven with a 50% duty cycle. The peak voltage and current stresses on

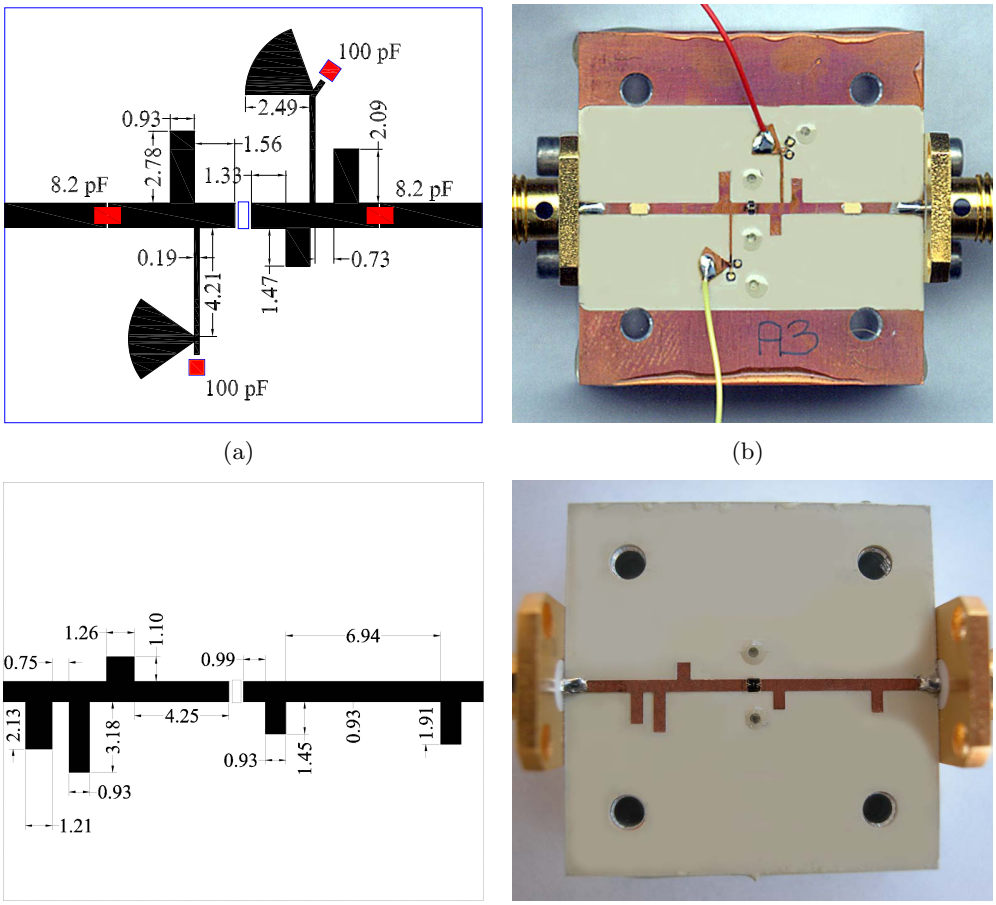


Figure 4.1: Layout and photograph of the (a-b) GaAs MESFET and (c-d) InP DHBT class-E PA. The PAs are fabricated on 0.635-mm thick Rogers TMM6 substrates with er=6. The 50Ω microstrip lines in the matching networks are 0.93mm wide. High impedance bias lines are used for providing gate and drain supply voltages for the MESFET PA. Single layer mm-wave capacitors are used for power supply bypassing and AC coupling. The HBT PA is biased with external bias Tees.

the device are $3.6V_{DD}$ and $2.7I_{DD}$, requiring a power backoff around 1.5 dB. Since the device has to be a good switch, the operating frequency limit for class E is several times smaller than f_T, and depends on the transistor output capacitance C_{OUT} and maximal current rating, I_{MAX}. The output impedance presented to the device, assuming an ideal switch, a high-Q output circuit assumption, a 50% duty cycle and soft turn-on voltage waveforms [42] is given by

$$f_{CLASS-E} = \frac{I_{MAX}}{56 \cdot C_{OUT} \cdot V_{DS(CE)}} \tag{4.1}$$

$$Z_E = \frac{0.28}{\omega_s \cdot C_{OUT}} \cdot e^{j49.1^\circ} \tag{4.2}$$

This impedance is designed at the fundamental switching frequency and implemented with transmission lines at 10 GHz. The matching network also presents a high impedance (open) at the second harmonic. In practice, the device does not have enough gain at the third harmonic to justify a more complicated harmonic tuning circuit. After designing the output impedance, a load and source pull is performed in the neighborhood to optimize the efficiency, gain and power for a realistic non-ideal switching device. The class-E topology is not as sensitive to circuit variations as some other tuned amplifier topologies and lends itself well to the described design approach, with demonstrated power added efficiencies (PAE) of 60% to 70% in [46, 43, 47].

For the MESFET and HBT transistors used for the PAs in this work, the output capacitances and f_T/f_{max} are (0.11 pF, 30/60 GHz) and (0.185 pF, 80/150 GHz). The corresponding optimal source and load impedances for class E operation are found to be (9.1-j2.4 Ω, 35.9+j37 Ω) and (15.1-j0.5 Ω, 15.8+j18.2 Ω). The measured performance for the PAs from Fig. 4.1 is given in Tables 4.1 and 4.2.

Table 4.1: Compared characteristics of 10-GHz MESFET and HBT class–A hybrid PAs.

	V_{DC-OUT} [V]	V_{DC-IN}	I_{DC-OUT} [mA]	P_{1dB} [dBm]	G [dB]
GaAs MESFET	5	-0.64	70	19	10
InP DHBT	5	0.72	40	21.9	10.5

DC Operating points for Collector and Drain (Output) and Base and Gate (Input) with associated current consumption, output power and gain. The GaAs MESFET and InP DHBT devices have f_Ts of 30GHz and 80GHz, respectively.

4.2.2 Additive Phase Noise Measurement Comparison

The residual phase noise measurements were carried out for both class-E and linear class-A amplifiers. Two compression levels were measured for class-A to understand phase noise behavior as the device compresses.

The MESFET amplifier exhibits a significant change between class-E and linear class-A modes as shown in Fig. 4.2. While consistently following a 1/f behavior, the noise level increases by 15dB between classes A and E. The class-A PA in 1-dB compression has a noise pedestal increase of 2-7 dB between 100 Hz and 10 kHz.

These results differ slightly from those discussed in [37], where the phase noise offsets less than -100 dBc/Hz converged for the class-E and class-A 5-GHz PAs, while the measurements presented here show the same increase in phase noise from 10 Hz to 1 MHz. The difference between the results in this work and that in [37] is possibly due to the fact that the 50-% efficient PA in [37] is likely operating in class AB and has different AM-PM conversion, as discussed in the next section.

The HBT amplifier phase noise measurement results are shown in Fig. 4.3. A large noise pedestal exists between 10 Hz and 10 kHz for both classes of HBT amplifiers. The class-A and class-E PAs have a relatively large amount of noise at small offsets, but above 10 kHz offset, the noise drops to levels below -160 dBc/Hz.

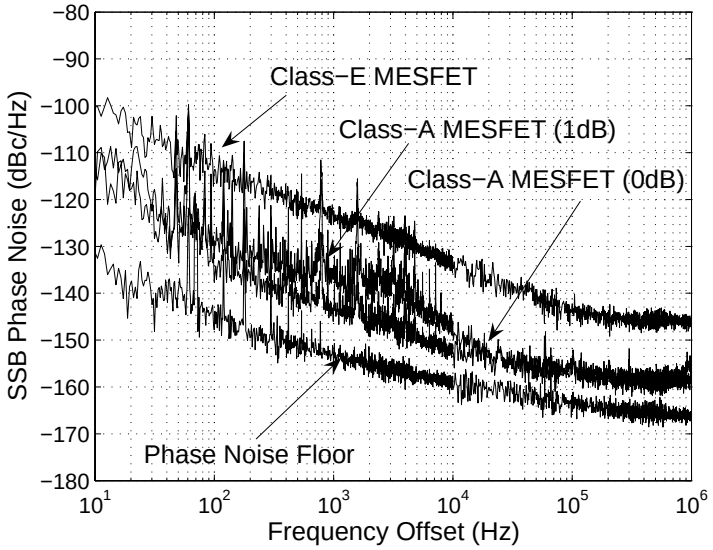


Figure 4.2: Class A vs. Class E residual phase noise measurement of the 10-GHz MESFET PAs. Here it can be seen the phase noise of the class-E PA is degraded by abotu 15dB from the class-A version. The class-A amplifier is shown in 0dB and 1dB compression with a slight degredation of phase noise at 1dB in compression.

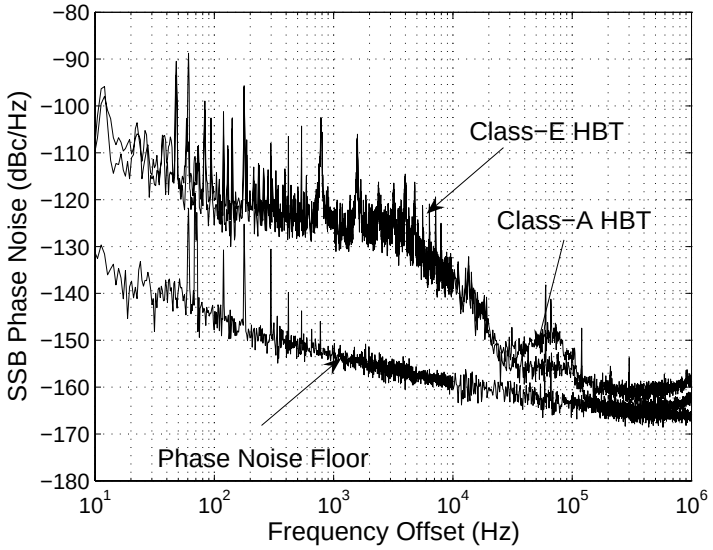


Figure 4.3: Class A vs. Class E residual phase noise measurement of the 10-GHz HBT PAs. Here it can be seen the phase noise of the class-E HBT is not significantly different from teh class A HBT for either 0dB or 1dB compression levels. The HBT is shown here to not follow conventional 1/f behavior of 10dB/decade increase in phase noise as the fourier frequency becomes smaller.

Table 4.2: Compared characteristics of 10-GHz MESFET and HBT class–E hybrid PAs.

	V_{DC-OUT} [V]	V_{DC-IN}	I_{DC-OUT} [mA]	P_{OUT} [dBm]	G [dB]
GaAs MESFET	-1.55	4.2	4	20.7	8.3
InP DHBT	0.35	4.35	0	21	9.8
	η [%]	ρ_{IN} [dB]	$\Delta\phi$ [°]	CL [dB]	
GaAs MESFET	70	13	53	1.5	
InP DHBT	69	12	105	3.3	

V_{DC-OUT} and I_{DC-OUT}–drain (collector) DC voltage and current, V_{DC-IN}–gate (base) DC voltage, P_{OUT}–nominal output power, G–power gain, η–drain (collector) efficiency, ρ_{IN}–input return loss, $\Delta\phi$–relative phase deviation at nominal P_{OUT}, CD–compression level at nominal output power.

4.2.3 Class-E Discussion

In order to help explain the phase-noise measurement of the HBT and MESFET PAs, the AM-PM conversion is measured at different bias points in class-E and shown in Fig. 4.4. In this measurement the drain (collector) bias voltage is changed and the S_{21} phase measured on a network analyzer. The results are normalized to 5 V drain bias. This data shows significant AM-PM conversion under large signal conditions. Any voltage noise on the drain or collector bias will result in phase noise at the output, as discussed in [34, 35, 36].

The results in Fig. 4.4 are consistent with the measured phase noise. The MESFET amplifier has a significant AM-PM increase between small-signal operation (P_{IN}=3 dBm) and high compression (P_{IN}=12.4 dBm). Consistently, in Fig. 4.2, we see a broad phase-noise increase between linear class-A and highly-saturated class-E, as would be expected with a higher AM-PM conversion.

The HBT amplifiers in Fig. 4.3 also show consistent results with the AM-PM measurements. The AM-PM ratio of the HBT amplifiers is greater than that of the MESFET and virtually the same for low and high compression conditions. This may cause the increase in phase noise of the HBT over the MESFET.

The noise spectra seen in the HBT phase-noise plots seem to be related to the noise of the power supply that is used in the measurement, further concluding that

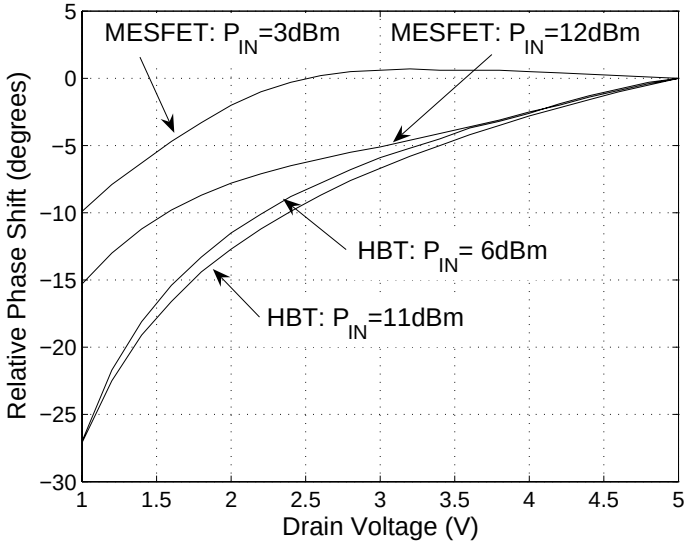


Figure 4.4: AM to PM conversion for the drain/collector bias voltage to output phase shift (in degrees). The MESFET has a marked difference in AM-PM conversion V/degree between class-A and class-E operation. The HBT amplifiers both exhibit nearly the same AM-PM conversion for different modes of operation. The MESFET always has lower AM-PM conversion. These measurements are consistent with the residual phase noise measured for the MESFET and HBT class-A and class-E amplifiers.

more upconversion of DC bias noise is taking place in the HBT devices. It would be interesting to examine bias-noise reduction methods [48] for class-E PAs, which points to tradoffs in upconverted noise and gain and PAE.

4.3 Low Noise High Power 200MH Amplifier Design

In chapters 5 and 6, NLTLs are discussed for the purpose of low phase noise frequency multiplication. The input referred phase noise is shown to be below -172dBc/Hz while theory predicts achievements could be near -180dBc/Hz. Current 100MHz crystal oscillators at 100MHz are available as low as -178dBc/Hz while commercial 1/2 Watt power amplifiers available are measured to be -172dBc/Hz. Oscillators at 1GHz in [49] have been shown to have a -185dBc/Hz noise floor with 29dBm output power.

This leaves room for improvement in power amp design focused on improved phase noise. Oscillators presented in [49] utilized several different transistors for low noise, one of which is a silicon bipolar device, the BFG591 from Philips. In class-C operation -180dBc/Hz was achieved in a closed loop environment. This became the basis for design of a PA for low phase noise.

While researching phase noise contributions to class-E PAs, papers from [50, 48, 51, 5] show that silicon bipolar devices can be designed for optimal phase noise. The results presented were for very low phase noise distribution amplifiers with lower output power. The 200MHz amplifier presented here is an application of this research at higher output powers. The goal is to design a 1/2Watt PA at 200MHz for use in the measurement system as well as for driving comb generators at high powers. Measurements reveal a phase noise of -176dBc/Hz at 20kHz offset.

4.3.1 Designing for Low-Phase Noise

While designing for low phase, two performance parameters are used as design criteria. First, what is the far from the carrier phase noise and the determinant factors.

From [5]:

$$L_{floor}(dBc) = -177dBm + NF - P_{in} \tag{4.3}$$

Rewritten in terms of output gain and power:

$$L_{floor}(dBc) = -177dBm + NF - P_{out} + Gain \tag{4.4}$$

Here, we see power output can increase the signal to noise ratio of the amplifier, but gain reduces it. Microwave amplifiers are typically designed for optimal gain, power output and noise figure. For low phase noise, this is not necessarily appropriate. If the gain is decreased by more amount than the noise figure is increased or conversely, the output power is increased without increasing gain, then the overall.

It was shown in [51] that the reduction in gain, if the output power remains constant, is equal to the reduction in added phase noise. To reduced gain, an emitter resistance of 5ohms was used to reduce gain while only marginally affecting output power. Very large emitter resistances create a severely bilateral device and become difficult to match.

A resistive bias was used instead of an active one but with a slight modification. A resistance is placed between the amplifier bias input and the collector bias inductor. The transistor bias resistance is tapped from this location. This creates a voltage divider effect. If the voltage divider is similar to the gain of the transistor, a low frequency negative feedback occurs. In principle, any collector or base current noise will have a self canceling feedback path.

4.3.2 Small Signal and Harmonic Balance Simulation

The power amplifier schematic is presented in 4.5. Only simple matching was. The capacitor directly on the collector was used to improve harmonic content. Without

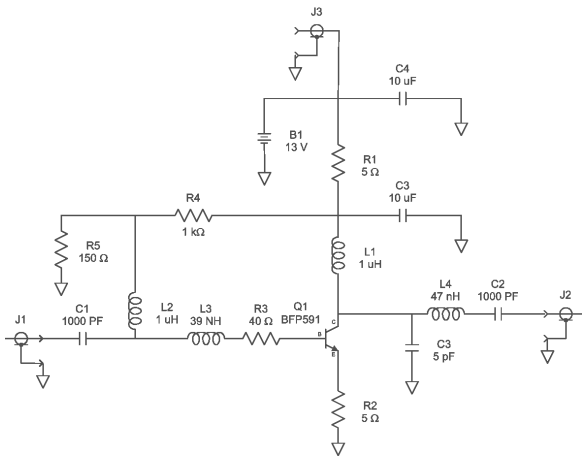


Figure 4.5: Schematic of a low phase noise Power Amplifier at 200MHz.

the capacitor, a strong second harmonic appeared, with 5-8pF, the second and third harmonic were reduced to -30dBc.

Harmonic balance and s-parameter simulations in ADS were carried out. The model did not accurately predict the exact values for the output match and is most likely due to the added emitter resistance creating a strongly bilateral device. The spice model may not have been sufficient to predict this effect. Alternatively, the s-parameter simulation in ADS uses an extremely small input power while in measurements, a larger (-5dBm) source was used.

4.3.3 Measured Performance

It was desired to run this amplifier in compression to help suppress any AM noise. The power input vs. power output curves in Fig. 4.6 show a very soft gain compression. At 2.5dB of compression, the operating point, all harmonics were at 30dBc, exhibiting near sinusoidal behavior. While operating at p_{in}=27.5dBm (562mW) and p_{out}=10dBm (10mW), the amplifier consumes 90mA at 13V (1.17W). This equates to a power added efficiency of 47.6%.

The amplifier was first measured in a single channel additive phase noise system

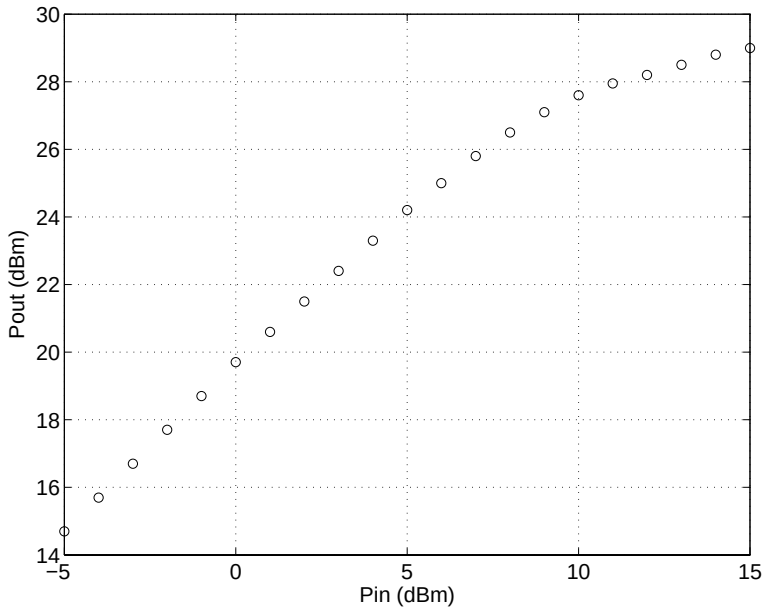


Figure 4.6: Power input vs. power output measurement. The device is operated at 10dBm input with 27.5dB output, or approximately 2.5dB in compressions

but only the system noise floor was observed at -170dBc/Hz at 10kHz offset. The cross-correlation system improves this noise floor by 15dB to -185dBc/Hz at 10kHz. The measured performance is shown in Fig. 4.7. The measured performance is -175dBc/Hz at 10kHz offset from the carrier, a 3dB improvement over the industry standard UTO-1023 with a measured floor of -172dBc/Hz at 10kHz offset and 27dBm output power.

Small signal noise figure measurement was completed using the same system and shown as the higher curve in Fig. 4.7 Substitution of Eqn. 4.4 yield a noise figure of 8.8dB:

$$NF = +177(dB) + P_{out}(dB) - Gain(dB) + L_{floor}(dBc) = 8.8dB \tag{4.5}$$

4.4 Chapter Summary

Two amplifiers were presented for application in a frequency multiplier chain at the source and as a final PA. It has been shown class-E amplifiers, using MESFET technology, are a viable alternative to standard class-A, AB and C amplifiers where the additive phase noise is acceptable. The 1/2Watt silicon BJT amplifier presented applies low phase noise amplifier design theory from to higher power PAs.

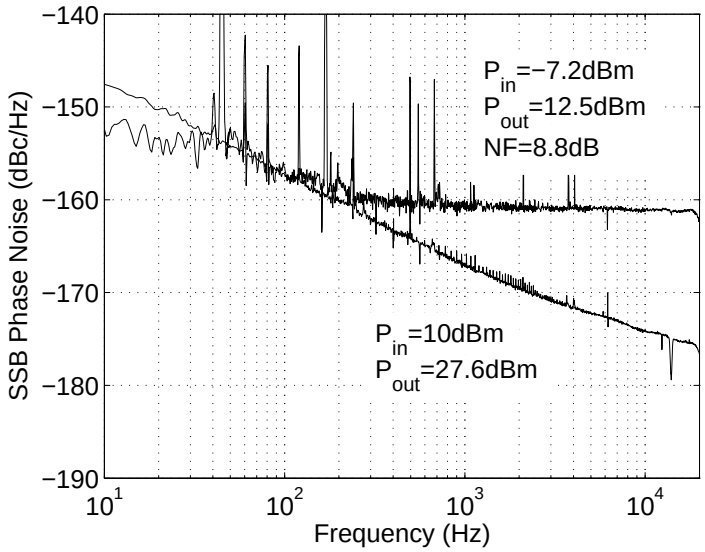


Figure 4.7: Phase Noise measurements in a cross-correlation system. With a phase noise of -175dBc@10kHz from the carrier, this is below virtually any single channel system. This was measured with 27.5dBm output and 10dBm input. The upper curve is the measurement in small signal demonstrating the ability of the cross correlation phase noise measurement to calculate noise figure in large signal conditions.

Chapter 5

Frequency Multiplication With Diode Multipliers

5.1 Introduction

Frequency generation at microwave frequencies may be accomplished fundamentally or by frequency multiplication. Lower frequency oscillators typically exhibit better close to the carrier phase noise, even after multiplication, than fundamental frequency oscillators. A phase noise comparison of a typical 10-GHz dielectric resonator oscillator (DRO) and a 100MHz crystal oscillator multiplied by 100 is shown in Fig. 5.1. Below 20kHz, the phase noise of an ideally multiplied source is far superior to that of a fundamental oscillator [52, 53]. The exceptions are fundamental laboratory standards using advanced phase noise reduction techniques that can produce a lower phase noise than a multiplied source at the expense of size, weight and portability.

At low (100MHz - 500MHz) frequencies, quality (Q) factors of SC-cut crystals used in high performance crystal oscillators are significantly higher than resonators available at X-Band. A multiplied frequency source benefits from the higher Q-factor at frequency offsets close to the carrier, even with the 20logN degradation due to frequency multiplication. Fundamental oscillators offer better performance at higher offset frequencies (20kHz). In a high performance system, it is common to phase lock the free running fundamental oscillator to the multiplied reference to achieve a compromise in phase noise both close to and far from the carrier. Inside the feedback loop bandwidth, the phase locked loop adds additional phase noise from the phase comparison and lock

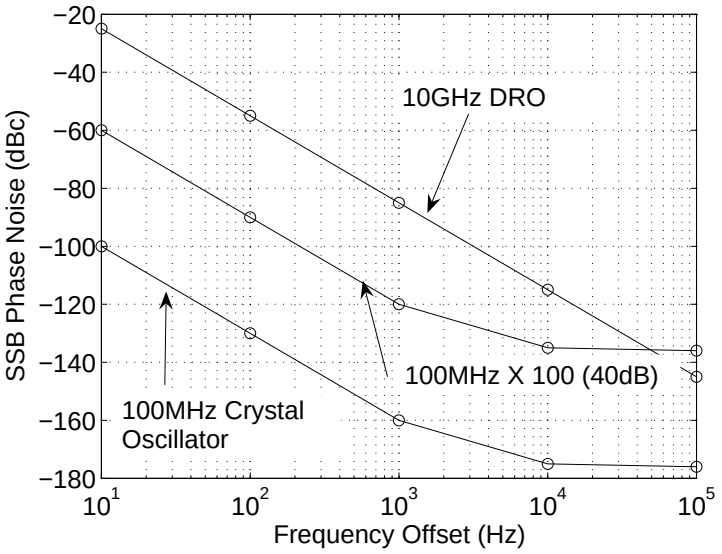


Figure 5.1: Phase noise comparison of an ideally multiplied 100MHz source to a dielectric resonator oscillator at 10GHz. At offset frequencies less than 20kHz, the multiplied source offers superior performance.

circuitry.

5.1.1 Traditional Frequency Multipliers

Frequency multiplication is typically accomplished using the two-diode multiplier for frequency doubling or tripling or the step recovery diode for high harmonic generation. Phase noise measurements reveal that two-diode frequency doublers have the best spectral purity, or lowest additive phase noise of any available frequency multiplier [28, 29]. Two-diode frequency triplers are also possible with similarly low added phase noise [54]. Step recovery diodes create a harmonic rich output based on a sinusoidal input. High order multiplication can be accomplished in a single step rather than cascaded X2 and X3 multiplication, simplifying system architecture. Phase noise measurements of step recovery diodes vary considerably based the type of step recovery diode used, the way it is implemented as a multiplier and the system in which it is measured.

During frequency multiplication by the the factor N, the phase noise is increased by the relation:

$$L_\phi = 20 \cdot \log 10(N) \tag{5.1}$$

Phase noise relates to the amount of noise at a particular offset relative to the carrier power. During frequency multiplication, the noise is multiplied similarly to the fundamental. In terms of time deviation within a sinusoid (jitter), the total noise equates to a certain percentage of the period. After frequency multiplication, that time deviation remains constant while the period is reduced by half in terms of voltage, creating a 20logN increase in phase noise.

Two-diode multipliers are very consistent in terms of spectral purity but require complex architecture for high-order multiplication. Step-recovery diode ease frequency multiplication at the expense of noise [8]. In this thesis, nonlinear transmission lines for use as frequency multipliers are introduced as high-spectral purity, high-order frequency

multipliers with simple circuit architecture.

5.1.2 Nonlinear Transmission Lines (NLTL

Nonlinear transmission lines (NLTL) have been successfully used in pulse shaping, equivalent time sampling oscilloscopes and time domain calibration standards for nearly 20 years. The monolithic NLTL was introduced in 1991 and has been successfully used to measure signals as fast at 2ps [55, 56, 57, 58, 59, 60].

The NLTL operates as a voltage variable transmission line. As the input waveform propagates, higher voltage amplitudes travel faster than lower voltages creating a step function in time [61]. The step function is harmonic rich up to appoximately one-third the inverse of the risetime of the signal. The output harmonics of an NLTL typically have less power than the SRD but are driven at a much lower power input level. However, with more research, this statement may not be true much longer. A qualitative comparison of harmonic output spectrum of the three multiplier technologies is shown in Fig. 5.2.

The exploration of the NLTL noise properties and design optimization for frequency multiplication is motivated by the desire to replace the step-recovery diode with a high-order frequency multiplier with noise properties similar to the two-diode doubler. NLTLs have been explored as frequency multipliers with high input frequencies in [25, 62], focusing primarily on high harmonic content. Until this work, the noise properties of NLTLs have been unexplored. Techniques used to increase harmonic output while reducing phase noise are introduced.

5.2 Diodes

Three types of diodes are discussed that are relevant to high order frequency multiplication: Schottky, PN and Step-Recovery or PIN diodes. The distinction between silicon (Si) and Gallium Arsenide (GaAs) and will be discussed as a generality [63, 64].

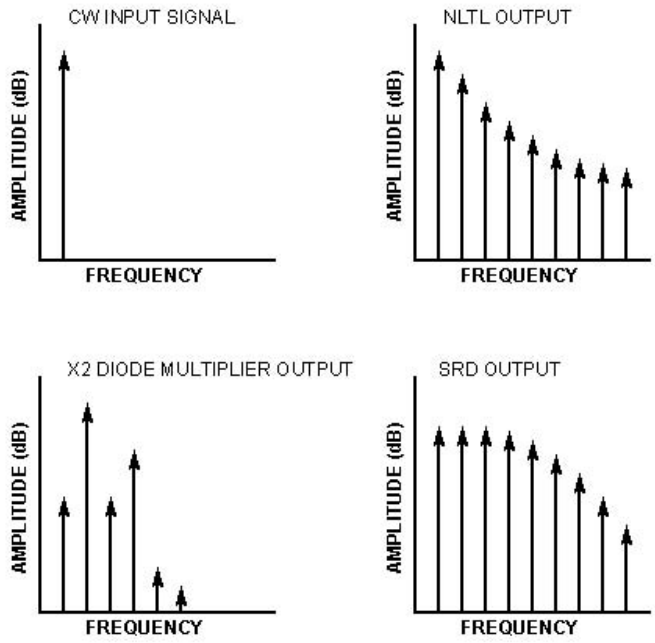


Figure 5.2: Sketch of spectral outputs for X2, SRD and NLTL multipliers.

5.2.1 Schottky Diode

The Schottky diode is a metal-semiconductor junction that is typically an N+ doped material. It is a majority carrier device that does not store charge. The majority carriers respond nearly instantaneously to applied voltage up to the relative RC time constant from the on resistance and zero bias capacitance. Silicon diodes typically operate up to 100GHz while GaAs diodes operates to 1THz. Additionally, the barrier height is much lower than a PN-junction diode allowing optimal conversion efficiency in mixers when operated as a switch. The majority of microwave mixers and diode doublers use schottky diodes [65].

In reverse bias, the schottky diode acts as a varactor, similarly to the PN-junction diode with improved high frequency performance. PN junctions suffer from large self capacitances at zero bias, limiting the useful frequency range to 10's of GHz. GaAs Schottky diodes in reverse bias are used in virtually all published monolithic NLTLs. The advantages of NLTLs exploited for use in pulse sharpening require extremely fast diodes operating in reverse bias. Currently, GaAs Schottky diodes are the only available diode meeting those requirements. A majority of the research is with linear doped abruped junction diodes with only a 2 to 1 capacitance change. Recently, modified doping profiles have been created for NLTLs, increasing the C-V response of the diodes similar to that of a hyperabrupt P-N junction varactor to improve pulse compression [66]. In order to operate to low input frequency (100MHz), large GaAs diodes would be needed.

5.2.2 PN Junction Varactor Diode

The PN junction diode is the typical switching diode used in a variety of applications. As with any diode, it operates as a voltage variable capacitor, or varactor, in reverse bias. With appropriate doping, the capacitance in reverse bias can be adapted

to a wide variety of C-V relationships. The PN junction diode is a minority carrier device that has the ability to store charge along the PN junction boundary. However, when operated well below the RC diode cutoff, the capacitance changes nearly instantaneously with voltage, creating a very useful device that is used in oscillators to tune frequency and voltage variable phase shifters. The PN junction varactor is used in nonlinear transmissions designed for low frequencies presented in this thesis. PN-junction varactors are available in abrupt and hyperabrupt profiles. An abrupt varactor typically has a 4:1 capacitance change over a very large (30V) voltage range. A hyperabrupt varactor may change nearly 9:1 in capacitance over only a few volts. The hyperabrupt varactors allow pulse compression in a few number of stages.

5.2.3 Step Recovery Diode

The step-recovery diode is a PIN architecture. A PIN diode, with a large intrinsic region, is most commonly used as an current controlled resistor or attenuator at microwave frequencies. The PIN diode will not respond to RF frequencies above the minority carrier lifetime of the diode. When the minority carrier lifetime is on the order of the inverse of the input frequencies, a snap-back transient occurs within the diode during the transition between forward and reverse bias. During forward conduction, charge is stored in the intrinsic region in the minority carriers. During reverse bias, the carriers are swept out of this region, creating a current snap-back, or step-recovery. This can be exploited with matching circuits to obtain an impulse output [67, 68, 69, 70, 71, 72].

5.2.4 Material - GaAs or Si

Material selection for each diode depends heavily on the frequency of operation and specific characteristics. The Schottky diode short majority carrier lifetime allows use of silicon up to 65GHz in mixer and diode doubler applications [73]. GaAs Schottky diodes operate to 1THz [74]. PN junction varactors can be either Si or GaAs based on

the desired reverse bias capacitance. Step-recovery diodes are predominately silicon as slow minority carrier lifetimes are required for proper operation with input frequencies of 100MHz to 1GHz. High frequency input SRDs have been made using GaAs in /citeChudobiak.

In forward conduction, Si has been well documented to offer superior noise characteristics to GaAs. Lattice structure impurities in GaAs create a large standard deviation to the velocity across the semiconductor as compared to silicon. Therefore, it is advisable to use silicon whenever possible if the diode is to go into forward conduction. This is observed as flicker noise at baseband and is upconverted to microwave frequencies from device nonlinearities.

The noise in reverse bias silicon PN junctions has only been published in [33] and to the author's knowledge, not been studied for GaAs. No recommendations can be made for noise properties of GaAs vs. Silicon for reverse bias. Measurements from this thesis do not significantly differentiate noise from NLTLs using GaAs Schottky varactors compared to PN junction silicon varactors. It may be hypothesized that the noise in reverse bias for both Si and GaAs diodes may be negligible compared to that in forward conduction, but this would need further analysis and measurement to prove. It has been stated in several oscillator papers that Si is superior to GaAs for varactor tuning. None of the articles contained a reference for this and appears to be unsubstantiated data.

5.3 Diode Frequency Multipliers

In this section, operation and general noise processes of frequency multipliers is presented.

5.3.1 Two Diode Multipliers

The two-diode frequency doubler will be primarily discussed here as the tripler is very similar and the analysis is thorough in [54].

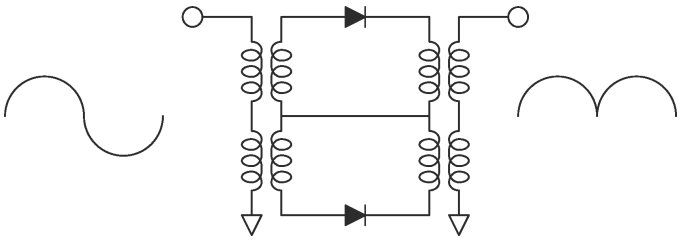


Figure 5.3: Schematic of the two-diode multiplier. It is nearly identical to that of a low frequency AC voltage rectifiers except the baluns are designed to operate at microwave frequencies. The conversion efficiency is related to the peak voltage input and the voltage drop of the diodes.

5.3.1.1 Operation

The two-diode doubler is a rectification circuit as shown in Fig. 5.3. During half the sinusoidal cycle of the input signal, the input is passed directly to the output. In the second half of the input cycle the phase is reversed 180 degrees and passed to the output. The graphical representation of the voltage waveform is shown in Fig. 5.4. The signal is reduced by one diode voltage drop when doubling. A typical input power for a diode doubler is 12dBm, approximately 2V p-p. With a forward voltage of 0.5V, there is a four times reduction in voltage or 12dB reduction in output power. An advantage to the diode doubler is that all other harmonics are below the desired output harmonic by 12dB, reducing filter requirements.

5.3.1.2 Noise Properties

The dominant noise in a diode doubler originates from forward conduction shot noise within the diodes. Shot noise will affect the zero crossing time when the diode transitions from forward conduction to an approximate open-circuit. Shot noise is proportional to the average diode current per Hz by:

$$< i_{sh} >= \sqrt{2qi_{avg}} \tag{5.2}$$

In a diode doubler, the output voltage is linearly proportional to the input voltage

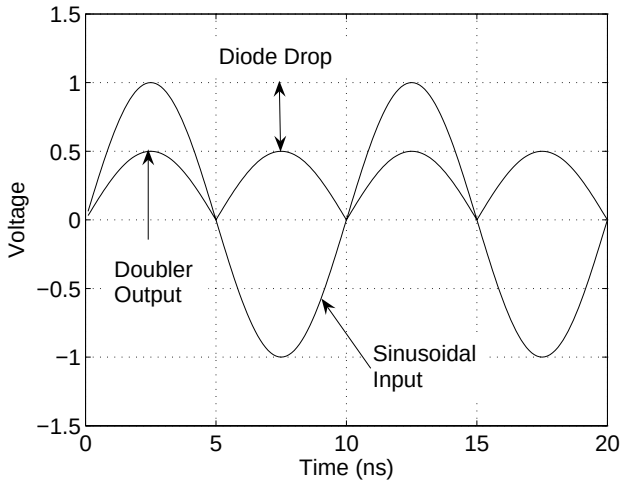


Figure 5.4: Two-diode doubler input and output voltage waveforms. The input is rectified to the output. Conversion efficiency is set by the barrier height of the diode and the maximum input power.

minus the diode voltage drop. The shot noise is proportional to the square root of the average diode current, which is linearly proportional to the output voltage. Therefore, to increase the signal to noise ratio of a diode doubler, a larger input signal can be used. The signal output will increase faster than the diode adds shot noise. Therefore, high level Si-based diode doublers are the standard in low noise frequency multiplication, allowing input powers as high as 23dBm and signal to noise ratios in excess of -180dBc/Hz.

5.3.2 Step Recovery Diodes

Step-recovery diode multipliers exploit the snap-back effect of the diode to produce an impulse response. The snap back is the sudden release of charge when after the transition from forward conduction to reverse bias. Input and output matching networks well documented in [67, 68, 69, 72] provide the necessary matching conditions to shape the current snap back into a voltage impulse.

5.3.2.1 Operation

During forward conduction, charge is stored in the intrinsic region of the diode. As the SRD is switched from forward conduction to reverse bias the stored charge is swept out rapidly from the fields produced by reverse bias. Step recovery diodes are designed for long storage time (low input frequency) and short fall time (high harmonic output) [67]. The intrinsic region width and doping in the PIN structure are adjusted to optimize this effect. In high reverse bias, avalanche conditions can occur, creating a noise multiplication effects while improving harmonic efficiency [71]. Diodes specifically designed to avalanche are used in noise sources and therefore the operation of the step recovery diode is critical to the additive phase noise.

5.3.2.2 Noise Properties

The step-recovery diode exploits two diode characteristics to create harmonics that are typically associated with high noise levels. First, to store charge, the step-recovery diode must be driven very hard (19dBm-27dBm) in forward conduction to push carriers into the intrinsic region. More than 500mA of peak current may be observed. While shot noise is proportional to the square root of the mean current flow, high current levels exceed the shot noise relation and excess current noise is produced [63]. Contrary to the two-diode doubler that improves the phase noise (signal to noise ratio) with increased input power, the SRD may actually degrade the phase noise at higher input power levels.

The second mechanism is the output current transient from carriers swept out quickly from the intrinsic region. The carriers will be uniformly distributed across the intrinsic region in forward conduction. During reverse bias, the carriers closest to the P and N regions will be swept out first. Those near the center of the intrinsic region will be swept out last and have the most interaction with the semiconductor lattice structure. This interaction creates a deviation in the amount of time it takes for the carriers to leave from cycle to cycle. The distribution in time it takes for carriers to leave this region will be observed as added phase noise. This is shown from a exaggerated graphical representation in Fig. 5.5.

The description given is a very qualitative view of the noise mechanisms in an SRD. To the authors knowledge, no paper has quantified the effect of each of these sources. Most likely, the quantities are highly device dependent. Measurement and experimentation may be the solution to phase noise optimization.

Observed noise phenomena in SRDs within the industry have motivated much of this work. The summary of observed noise in SRDs and potential causes given here result from discussions with Dr. Kipp Schoen of Picosecond Pulse Labs based on his

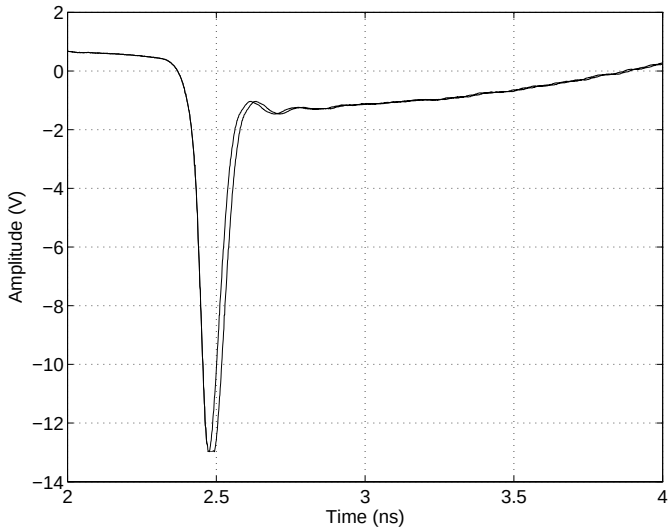


Figure 5.5: An exaggerated graphical representation of the uncertainty of the fall time that may contribute to additive phase noise at higher harmonics greater than the ideal 20logN relation.

interactions with designers using SRDs.

- The additive phase noise in a SRD multiplier is known to be sensitive to output mismatch [28]. When filtering a single harmonic, high rejection filters are required that are almost exclusively reflective. Large signal reflections may drive the SRD either out of snap-back effect or into avalanche conditions [71] creating additional undesired noise or reducing output harmonic content. Attenuation must be used between the SRD and filter to reduce this effect and is optimized through experimentation. The length of line between the SRD and filtering circuit may also be used to reduce destructive interference from reflected signals.

- High frequency step recovery diodes tend to perform better than low frequency SRDs. This is undocumented and is included as an observation. High input frequency SRDs have a smaller intrinsic region than low frequency SRDs proportional to the decreased time for charge storage. If the time it take for carriers to exit the intrinsic regions is proportional to phase noise, then it may be concluded a smaller intrinsic region diode will exhibit less additional phase noise.

- The SRD tends to exhibit more additional phase noise when driven with a higher input power than at lower input power. This may be related to the increase in shot noise due to the increased average input current going into the diode. Shot noise will affect the time when the leading edge of the output impulse occurs, thereby adding additional noise to all harmonics. Alternatively, at high drive levels, the SRD may be near avalanche condition, creating noise in excess of shot noise.

5.3.3 Nonlinear Transmission Lines

A transmission line can be modeled as an equivalent circuit using a series of inductors and shunt capacitors. The upper frequency limit for using this type of modeling is

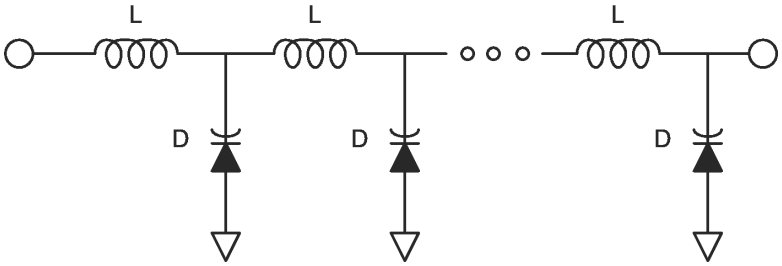


Figure 5.6: Simplified NLTL schematic showing the distributed L-C elements. The voltage variable capacitor is the nonlinear element that creates the pulse compression.

set by the low pass filtering effect of individual inductors and capacitors sections. This is a linear system in which the inductor and capacitor never differ in their value depending on voltage. Nonlinear transmission lines introduce a nonlinear element that is voltage dependent as shown in Fig. 5.6. The voltage variable circuit component alters propagation velocity based on voltage. Typically, a varactor is used that decreases capacitance as voltage increases, resulting in a voltage dependent phase velocity. Higher voltages propagate faster than lower voltages, causing a decrease in the rising edge of the signal, referred to as pulse compression. The pulse compression is eventually limited by the dispersion and loss of the NLTL. In fact, if the nonlinearity is balanced with dispersion, a soliton line can be obtained [61].

5.3.3.1 Operation

The characteristic impedance of such a lumped element transmission line is defined as:

$$Z(V) = \sqrt{\frac{C(V)}{L}} \tag{5.3}$$

The phase velocity of propagation along the line is:

$$v_p(V) = \frac{1}{\sqrt{LC(V)}} \tag{5.4}$$

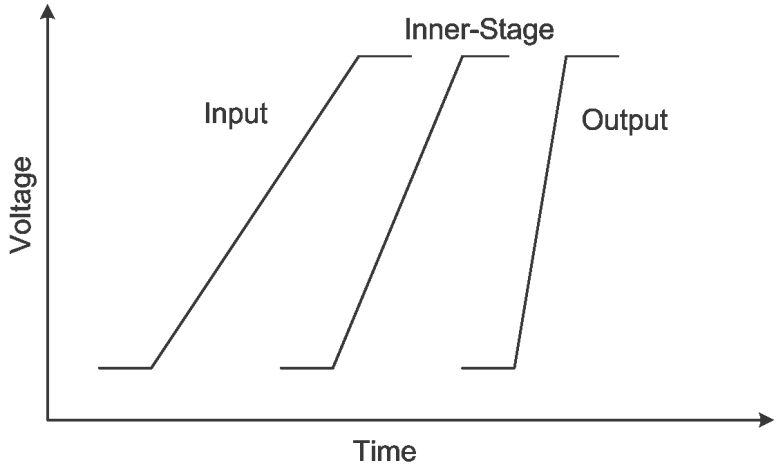


Figure 5.7: Representative pulse compression of an NLTL. Higher voltages travel at a faster velocity than the lower voltages, creating a step function rich in harmonics. The difference in velocity between the low voltage and high voltage along the line is the amount of pulse compression in time.

In small signal operation this change will be almost negligible. In large signal, when the capacitance change is large, the phase velocity change over many periodic elements will be significant. Higher voltages will travel faster down the artificial transmission line than lower voltages. This creates a voltage step function on the rising (or falling, depending on polarity of the varactor) edge of the the wave, as shown graphically in 5.7.

Fig. 5.7 is showing pulse compression for an ideal edge. In this thesis, the compression is focused on sinusoidal input waveforms. The center of the sinusoid easier to compression than the peak voltages due to a higher dv/dt edge rate. Therefore, biasing the NLTL is critical to optimum performance based on the number of stages within the NLTL. Biasing the center of the sinusoid around 0V results in the least amount of compression required to compress the sinusoid. Half the sinusoid is shunted to ground while the other half is compressed. In this situation, the line may be half as long. Using a longer line, reverse biasing the transmission line so that all or a majority of the sinusoid maintains the varactors in reverse bias allows optimal conversion efficiency

at the expense of more elements. The bias point of operation heavily affects the noise analysis of the transmission line.

5.3.4 Noise Analysis of Nonlinear Transmission Lines

The varactor diodes in an NLTL operate for up to half a period in forward conduction, depending on bias conditions. The remainder of the time is spent in reverse bias. Diode noise in forward conduction is well known and dominated by shot noise from the average current flow in the diode. In reverse bias, noise in varactor diodes at high microwave frequencies is comparatively unknown.

Noise measurements completed on varactor diodes at 5MHz in reverse bias are published in [8]. The measure of additional noise of a particular element is defined as the power spectral density of the change in value per value over offset frequency as shown in Fig. 5.8.

The data presented in Fig. 5.8 may be converted to phase noise with the knowledge of the phase shift across a particular element by the relations from [8]:

$$\phi = \arctan \frac{imX}{reX} \tag{5.5}$$

$$L_{\phi}(f)[dBc/Hz] = \frac{\Delta X}{X} + 20 \log 10 \frac{sin^2(2\phi)}{8} \tag{5.6}$$

For an NLTL with 8 stages with a 2.5pF mid reverse bias point for the varactors, the calculated phase noise assuming values taken for the hyperabrupt varactor is -180dBc/Hz at 100Hz offset from the carrier. This is below the measurement noise floor of the cross correlation system and orders of magnitude better than any available oscillator.

It will be discussed in the next section that reverse biasing the transmission line will lead to optimal conversion efficiency. The NLTL is inherently a voltage variable

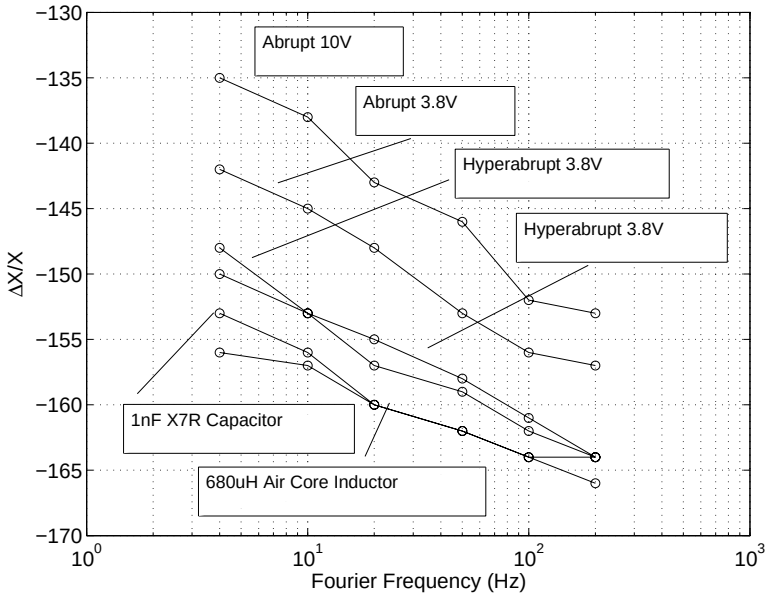


Figure 5.8: The power spectral density noise measurements of discrete fixed elements including varactors at various offset frequencies. What can be concluded from this is that varactors in reverse bias have noise levels relative to or only slightly higher than discrete capacitors and inductors. The noise of a varactor diode in forward conduction is orders of magnitude higher than the levels in reverse bias.

phase shifter. Therefore any noise resulting from reverse biasing the line will be directly converted to phase noise. The unbypassed equivalent resistance of the reverse bias circuitry will lead to a broadband noise around the carrier at the frequency of operation. The voltage noise of an equivalent resistance per Hz is:

$$V_N = \sqrt{4kTR} \tag{5.7}$$

The equivalent voltage noise of a 1Ω, 50Ω and 2kΩ resistor is -198dBV/Hz, -181dBV/Hz and -165dBV/Hz, respectively. Similarly to the phase detector, the phase shifter has a V/rad relation to the sensitivity to the applied reverse bias voltage that may be calculated at reverse bias midpoint for a first order analysis. The phase noise resulting from a particular equivalent resistance and phase shifter constant is:

$$L_\phi(f_m)[dBc/Hz] = 20\log 10(\sqrt{4kTR}) - 20\log 10(K_d) - 3dB \tag{5.8}$$

The NLTL designed in the following section has a pulse compression of 886ps between 1V and 3V reverse bias, resulting in a NLTL phase shifter constant of 0.557V/rad. The phase noise due to a 1Ω, 50Ω and 2kΩ equivalent bias resistance is -196dBc/Hz, -179dBc/Hz and -163dBc/Hz, respectively. It is obvious that a very low equivalent bias resistance is required to maintain low phase noise when reverse biasing an NLTL.

Phase noise due to shot noise is determined by calculating the equivalent shot noise from the power being shunted to ground in the diodes then converting that to voltage noise. The input must be determined as a voltage value, rather than power. Under large signal conditions, half the voltage minus the forward voltage drop of the diode is shunted to ground. The average current involved would be 0.707 times the calculated shunted voltage to ground in series with a 50Ω impedance. An NLTL that is biased (with a bias inductor) at ground will conduct the input power to ground slightly less than half the time. Assuming a 7V p-p input voltage, approximately 3V will be

shunted to ground in series with a 50Ω source impedance. The average current will be 0.707 times the shunted voltage divided by 2 because only half the sinusoidal cycle is flowing through the diode to ground, or approximately 20mA. This results in an average shot noise of 80pA/Hz. The NLTL is a distributed transmission line so the shorted diode sees and equivalent impedance of half the characteristic impedance or 25Ω. The equivalent voltage noise is 2nV/Hz. The resulting phase noise based on the NLTL phase shifter constant is -174dBc/Hz.

Measurements of NLTLs in which 50% of the duty cycle was in forward conduction exhibit a phase noise of -172dBc/Hz to -176dBc/Hz, consistent with the forward conduction analysis. Measurements of reverse biased NLTLs with bypassed supplies yielded a phase noise of -181dBc/Hz, at the limit of the measurement system and again consistent with the reverse bias noise analysis.

5.4 NLTL Design and Simulation

The generalized schematic of the uniform NLTL is shown in Fig. 5.9. The design uses identical inductors and varactors uniformly distributed along an artificial transmission line using surface mount components. It is based on the NLTL used for analog signal processing designed by Walsh in [75]. The frequency range is selected to be at 200MHz input and capable of creating harmonics past 2GHz. The design goal is to optimize for phase noise. An 8-stage NLTL is designed using hyper-abrupt varactors with zero bias capacitances of 9pF with a median capacitance of 4pF. A surface mount inductor of 10nH was used for optimal match across wide input voltage range. The characteristic impedance changes from 33Ωs to 100Ωs when not driven into forward conduction and will go below 10Ωs during forward conduction.

The first NLTLs explored for frequency generation used a bias inductor to ground. The goal was to mitigate the risk of any DC voltage noise from causing a voltage to phase conversion and add additional phase noise in the multiplication process. However,

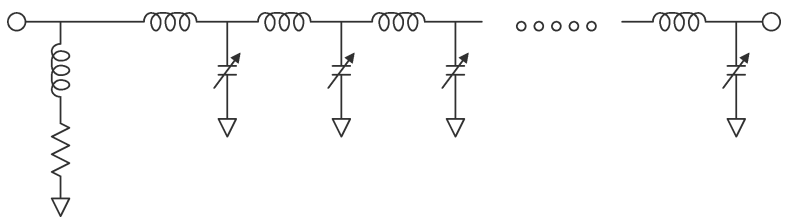


Figure 5.9: The schematic of a lumped element NLTL showing the input and output DC blocking capacitors and bias network. The diodes are varactors that create the nonlinear voltage dependent phase velocity relation.

using this method the diodes are kept in forward conduction for up to 50% of the duty cycle where shot noise is generated. The measured input-referred added phase noise is -172dBc/Hz to -176dBc/Hz and calculated to be -174dBc/Hz due to shot noise from forward conduction.

One method to keep the NLTL in reverse bias is to use a voltage source through a bias-T. While convenient, it is extremely difficult to create a DC voltage source with very low voltage noise. The NLTL acts as a phase shifter. DC voltage noise will appear as added phase noise at the frequency of operation at discussed in the previous section. Unless a battery is used, the voltage source will most likely not be clean enough and becomes impractical.

The rectification property of the diode was explored to create a reverse bias condition on the NLTL. It is observed that an NLTL without a DC return path, creates a natural reverse bias condition that biases the NLTL optimally for high conversion efficiency. The diode DC rectification current in parallel the equivalent resistance of the diode creates a reverse bias voltage. This condition is extremely sensitive to outside interference and fields, suggesting an extremely high equivalent resistance.

An external resistance in series with the bias inductor was used to observe the effect on conversion efficiency and include a lower resistance path to ground to reduce the NLTL sensitivity to the environment. Through simulation, an optimal value of between 500Ωs and 2kΩs was observed. Measurements confirmed the optimal value for

conversion efficiency to be 2kΩs. This value relates to what is known as the diode video resistance and is generally a few hundred ohms to several thousand ohms for most diodes. In older spectrum analyzers the diode detectors used a resistor to ground equivalent to the diode rectification equivalent resistance that drove the video amplifier for optimal sensitivity. NLTL output voltage and power comparing a bias inductor to ground and a 2k resistor is shown in Figs. 5.10, 5.11, 5.12 and 5.13. Improvements in output harmonics and conversion efficiency are observed with the higher bias resistance. A 5dB increase in the 10th harmonic output power is observed through optimal resistance selection without changing input power levels. The average DC rectification voltage with 2kΩs is approximately 1.1V.

The pulse compression in the NLTL occurs due to the voltage dependent phase velocity. Similarly, the characteristic impedance of the line is a function of voltage. The input voltage of the line from simulation is shown in Fig. 5.14. High harmonics are observed that have been reflected back to the input. Low voltages at the input are caused when the NLTL goes into weak forward conduction, producing a very low impedance. The drive amplifier must be reasonably stable over a variety of operating conditions for consistent operation. Provided the output is a good broadband match, there will not be any standing waves along the NLTL. However, if the NLTL is directly driving a reflective load, standing waves dependent upon the harmonic may occur and either constructively or destructively interfere with harmonic generation. Unlike the SRD, the NLTL should not produce excess noise under poor load conditions. The output harmonic power will be affected. An observation during measurements was the inductively biased NLTL was nearly immune to load conditions for proper operation while the high resistance biased line required a good broadband match or attenuator between the NLTL and filter.

In Fig. 5.15 the voltage on a varactor at the 7th stage of the 8-stage NLTL is shown. The voltage is 50% higher than the output due to the non-linear loading effects

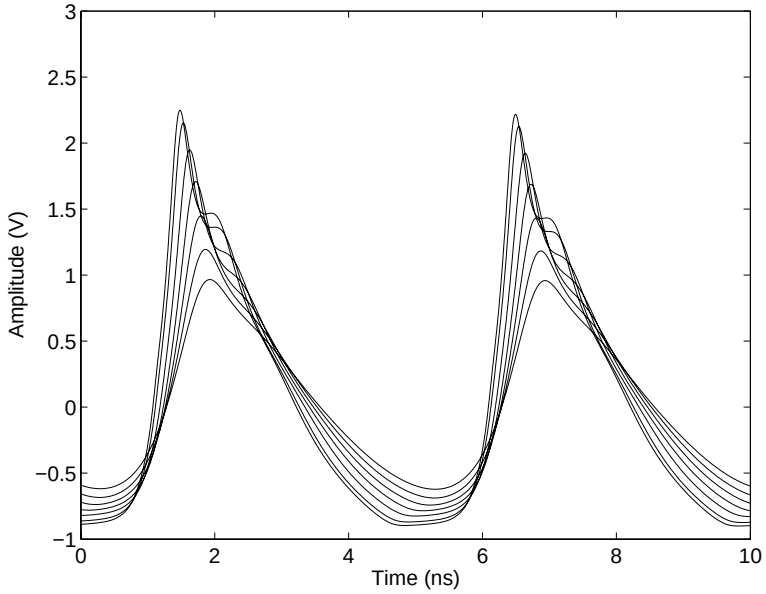


Figure 5.10: The ADS SPICE simulated output voltage waveforms of the 8-stage NLTL with an inductor bias to ground. The input power was swept from 10dBm to 22dBm in 2dB increments. The flat line at the bottom of the time domain outputs is where the NLTL is in hard forward conduction.

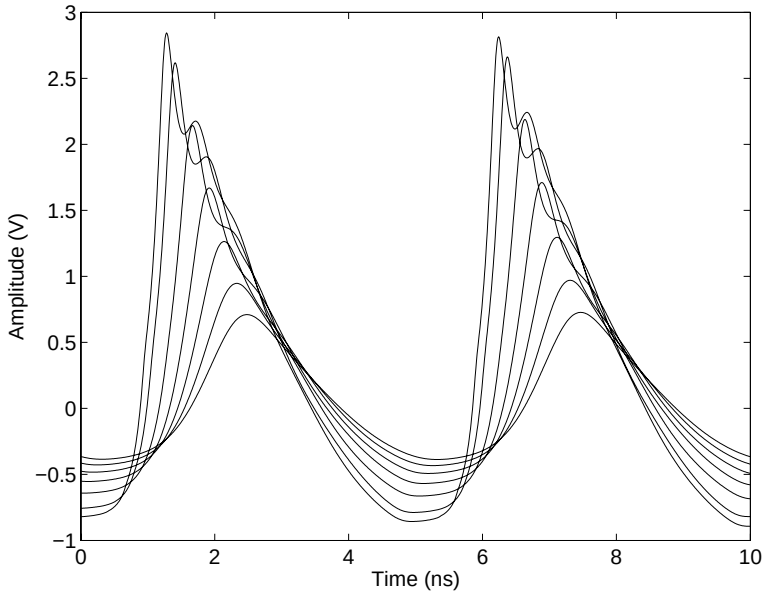


Figure 5.11: The ADS SPICE simulated output voltage waveforms of the 8-stage NLTL with a 2kΩ resistor bias to ground. The input power was swept from 10dBm to 22dBm in 2dB increments. The conversion efficiency improves with a higher resistance to ground. The diode rectification current in parallel with a resistor to ground creates a reverse bias proportional to input power. This provides a relatively easy way to optimally bias an NLTL without an external supply.

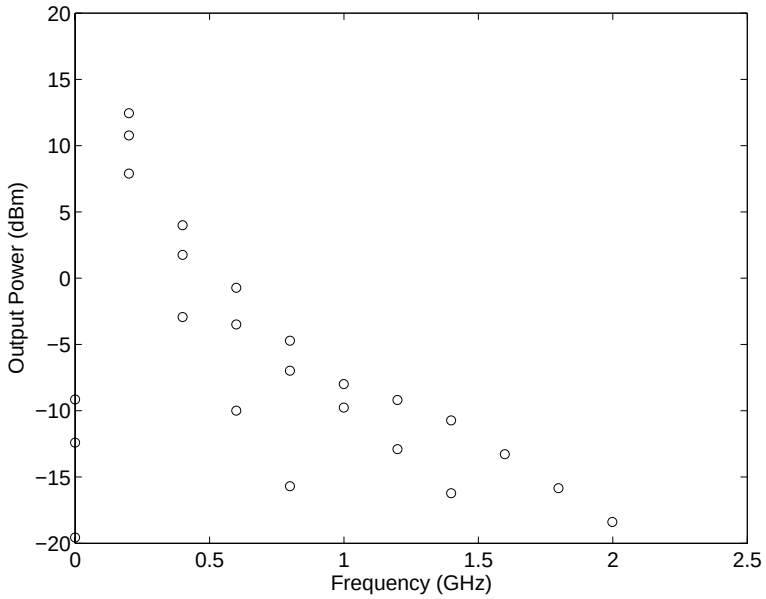


Figure 5.12: The harmonic output power calculated from the time domain simulation of the inductively biased NLTL. Power levels of 10dBm, 16dBm and 21dBm are shown.

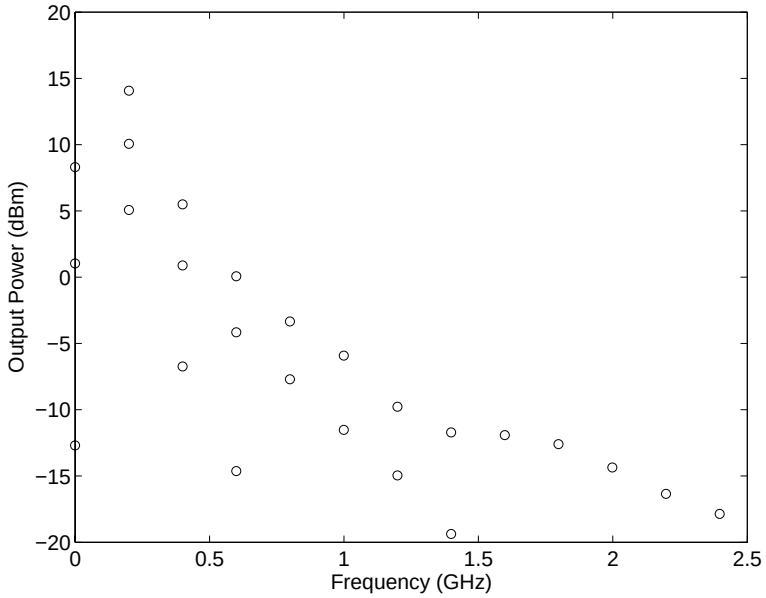


Figure 5.13: The harmonic output power calculated from the time domain simulation of the NLTL biased with a 2k resistor. Power levels of 10dBm, 16dBm and 21dBm are shown.

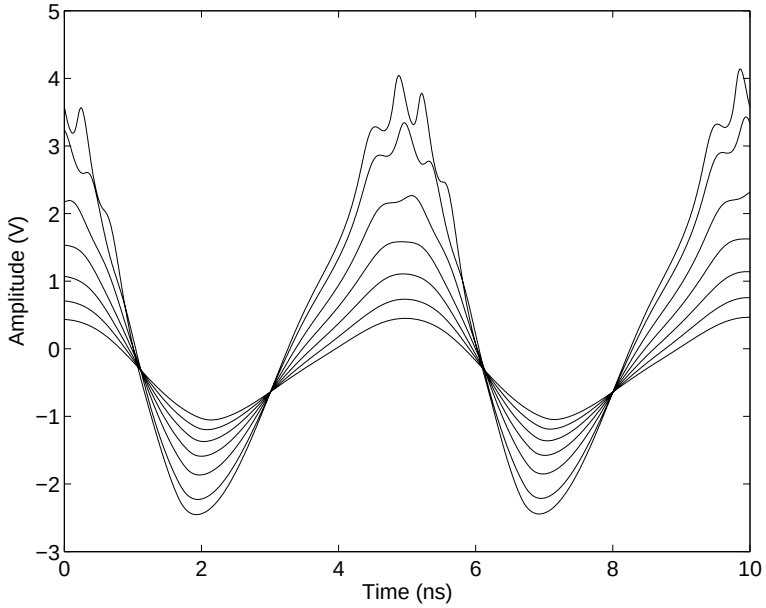


Figure 5.14: The time domain waveform seen at the input of the NLTL. As the voltage passes through the C-V curve of the diode, the line appears as a short circuit at negative voltage and an open-circuit at high voltages. This means that the driver amplifier must be stable of a wide variety of operating conditions. The input power is swept from 10dBm to 22dBm in 2dB increments.

of the NLTL. While the breakdown voltages of hyperabrupt varactors are high, the power cannot be increased arbitrarily without monitoring or simulating the voltage on the inner stages of the NLTL. Before breakdown, reverse current flow in the varactors may contribute noise that is difficult to diagnose. Above breakdown, the NLTL may be damaged, leading to long-term failures.

As discussed previously, a bias resistor of 2kΩ exhibits a voltage noise of 5.65nV/Hz. While much lower than most power supplies, the high voltage to phase conversion in an NLTL will contribute to additional phase noise. To this extent, the resistance must be bypassed sufficiently to reduce or eliminate this additional noise. A very low ESR capacitor must be used to create an RC time constant between the series resistance and the bypass capacitor that will be sufficient for the application. ADS is not capable of analyzing this effect sufficiently and is completed through measurements in Chapter 6. The analysis of the effects of bias condition and bypassing is presented as measurement in Chapter 6 and is in excellent agreement with the noise analysis in the previous section.

5.5 Chapter Summary

Designing NLTLs with uniform, linear and exponentially tapered lines has been covered extensively in literature. The work in this chapter presents a discussion of noise processes in frequency multipliers, specifically NLTLs. Techniques for designing NLTLs with improved harmonic output are presented. These same techniques are shown to improve additive phase noise as well when bypassed appropriately. Measurements in Chapter 6 prove that proper biasing is the most effective way to improve NLTL harmonic output and phase noise performance simultaneously and are consistent with the theory presented in this Chapter.

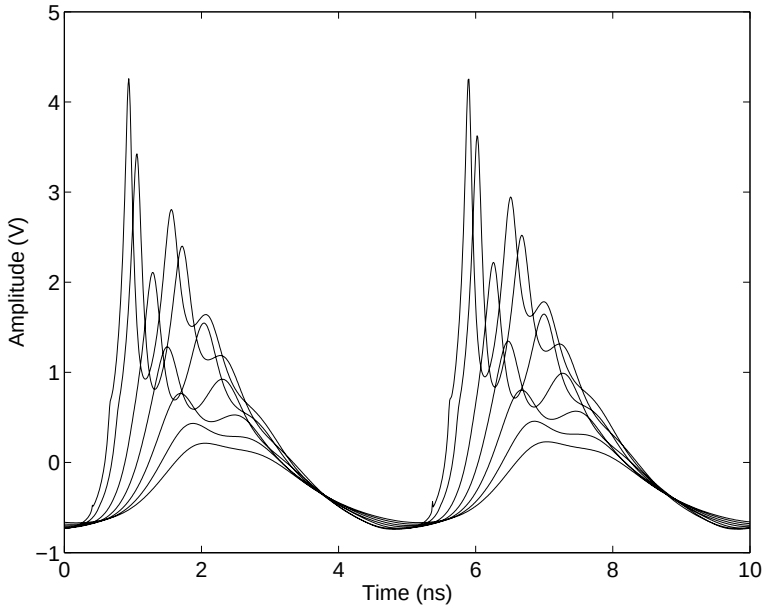


Figure 5.15: The time domain waveform seen at the input of the NLTL. The voltage at 7th stage of an 8-stage NLTL. Due to nonlinear impedance of the internal stages of the line, the voltages may be up to double the output voltage. This is a significant consideration if the output voltage comes with within half the breakdown voltage of the diode. At an internal stage, the breakdown voltage may be exceeded causing avalanche condition or breakdown thereby increasing noise in either case. The input power is swept from 10dBm to 22dBm in 2dB increments.

Chapter 6

NLTL's and Phase Noise Measurements

6.1 Introduction

The measurements presented in this Chapter are completed using the phase noise measurement systems described in Chapter 3 in conjunction with an equivalent time sampling oscilloscope. The NLTL multiplier research began with the measurement of Schottky-varactor based NLTLs designed at Picosecond Pulse Labs, models LPN7100 and LPN7110. The spectral purity of added noise is discovered to be much lower than that of SRD based multipliers with a direct measurement comparison as evidence.

The uniform, discrete NLTL designed in Chapter 5 is used to test bias conditions as a method to improve harmonic output power and phase noise. New bias methods are presented that optimize both parameters.

6.2 Diode Noise Measurements

To verify the theoretical basis that diode noise is dominated by shot noise, the forward and reverse noise characteristics across a PN junction silicon hyperabrupt varactor diode are measured. The schematic of the test setup is shown in Fig 6.1. A battery was used as a voltage source in series with the diode under test and a 50Ω resistor. Voltage fluctuations across the 50Ω resistor were measured using the baseband LNAs and audio card sampling circuit developed in Chapter 3.

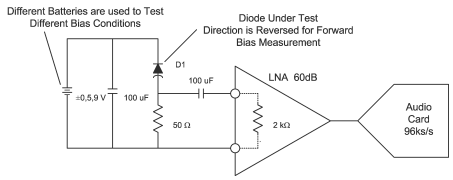


Figure 6.1: Diode voltage noise measurement setup. A 5V and 9V battery were used to forward and reverse bias the silicon hyperabrupt varactor in series with a 50ohm resistor. The AC-coupled noise across the 50ohm was measured using the LNA developed for the cross-correlation system and sampled with the 24-bit audio card.

Measurements in Fig. 6.2 demonstrate that voltage noise in a varactor is dominated by forward conduction current. The maximum specified current for the tested varactor is 100mA. While driving the diode with 150mA, significantly more voltage noise is observed than the shot noise equation would predict. This is evidence that reverse bias operation, as predicted in Chapter 5, is the optimum point of operation. Noise levels for very low levels of forward conduction, less than a few mA, are not expected to increase the phase noise dramatically.

6.3 Schottky Varactor NLTL Measurements

This research began with the design and measurement of Schottky varactor NLTLs at Picosecond Pulse Labs. Unique circuit architecture using patented GaAs Schottky fabrication techniques allow high pulse compression from low frequency and low power inputs, producing harmonics as high as 50GHz. The first generation of NLTLs, the LPN7100, generate harmonics to 20GHz from only 19dBm of CW input power. Higher frequency input devices such as the LPN7103 produce harmonics to 50GHz.

Time domain measurement of the NLTL using an equivalent time sampling scope is shown in Fig. 6.3. The power input to the NLTL is 19dBm. The comb generator is driven into forward compression for approximately 50% of the cycle. This was designed intentionally to eliminate voltage bias noise in the NLTL. Coincidentally, this design allowed placement of a reflective filter on the output of the NLTL without any attenu-

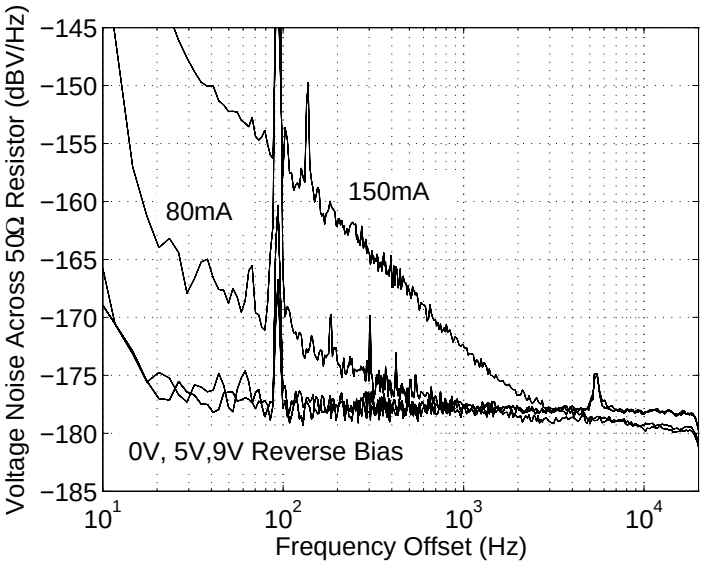


Figure 6.2: Baseband voltage noise measurements across a 50ohm resistor demonstrate the increased noise in forward conduction vs. reverse conduction. This verifies that it is imperative for low noise operation to keep the diode out of forward conduction. Additionally it is shown that for high current densities, slope is greater than 10dB/decade.

ation in between and without any degradation of output harmonic level or phase noise. This is a significant improvement over the SRD that is extremely load sensitive.

Power spectrum measurements over a wide variety of inputs is shown in Fig. 6.4. Above 19dBm, the NLTL is in a saturated state and no additional harmonics are generated. This property has the effect to reduce AM noise from an oscillator, similar to what a diode limiter accomplishes. AM noise reduction reduces any AM-PM conversion, a problem in SRD based multipliers.

The phase noise measurement system presented in Chapter 3 is capable of measuring to the 90th harmonic (18GHz) and is used to measure harmonics to 10GHz in Figs. 6.5- **??** with a 200MHz input. The goal of this measurement system is to measure very high harmonics where they can be amplified well above the noise floor with an extremely sensitive phase detector. While in practice this worked as expected, the measurement was limited by the low power of the NLTLs and additive phase noise of the required post-amplifiers. In all measurements, the additive noise of the NLTLs was nearly identical to the measured noise floor of the system. The results are encouraging with an input referred phase noise of at least -174dBc/Hz from the 10GHz, 50th harmonic measurements, significantly lower than SRD based comb generators. The NLTLs were measured with and without attenuation after the NLTL prior to the YIG-Tuned-Filter with absolutely no degradation in phase noise performance as seen in SRDs in [28]. The measurement results were confirmed independently at Picosecond Pulse Labs customer sites using a different measurement system.

6.4 High-Output Schottky Varactor NLTL Measurements and Comparison to the SRD

The second generation of NLTL based frequency multipliers from Picosecond Pulse Labs, the LPN7110, is designed for an input power up to 27dBm, creating a direct replacement for an SRD. The time domain output is shown in Fig. 6.10. The

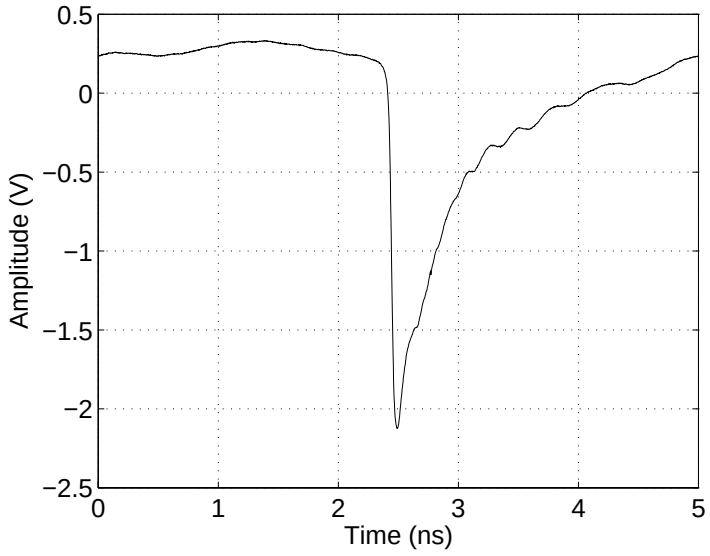


Figure 6.3: Time domain output of the LPN7100 low power NLTL from Picosecond Pulse Labs at 200MHz, 19dBm input.

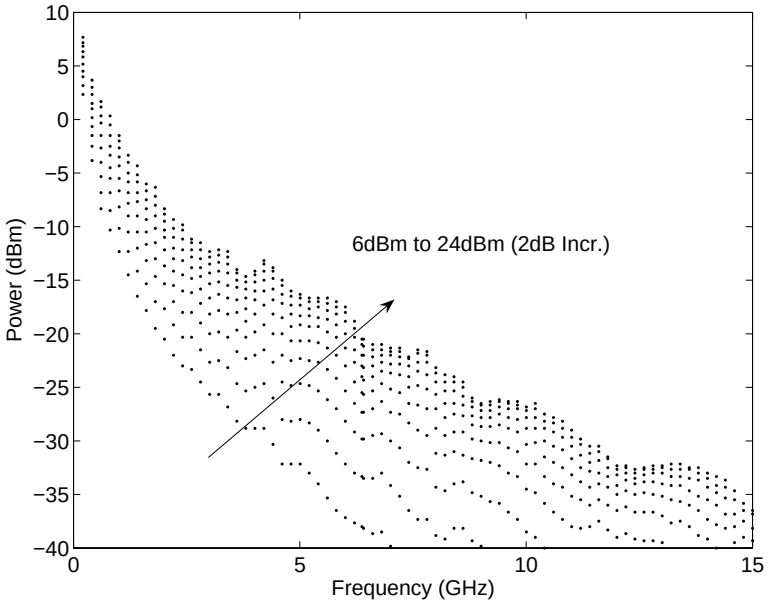


Figure 6.4: Harmonic content of the LPN7100 with 200MHz input with power swept from 6dBm to 24dBm in 2dB increments.

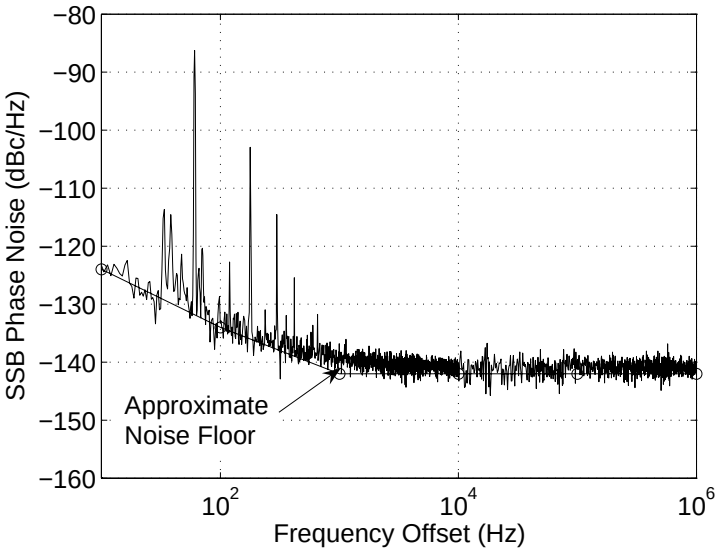


Figure 6.5: Phase noise measurements of a pair of LPN7100 (3dB subtracted for two devices) at 2GHz, the 10th harmonic. The measured phase noise and measurement noise floor were indistinguishable.

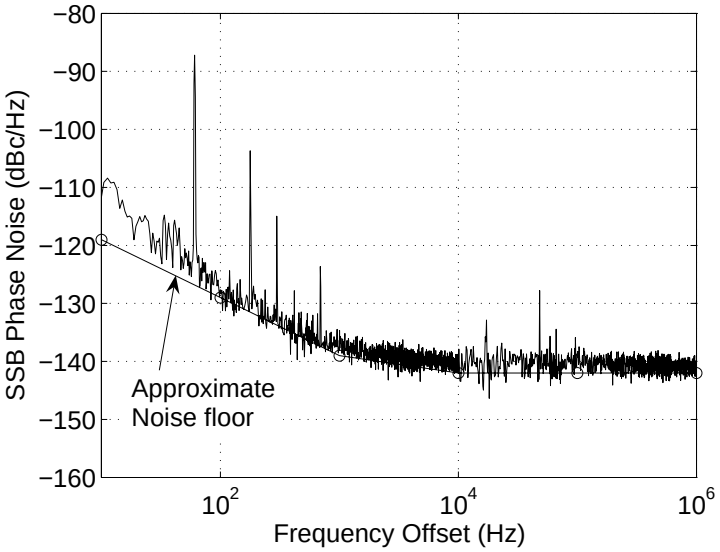


Figure 6.6: Phase noise measurements of a pair of LPN7100 (3dB subtracted for two devices) at 4GHz, the 20th harmonic. The measured phase noise and measurement noise floor were indistinguishable.

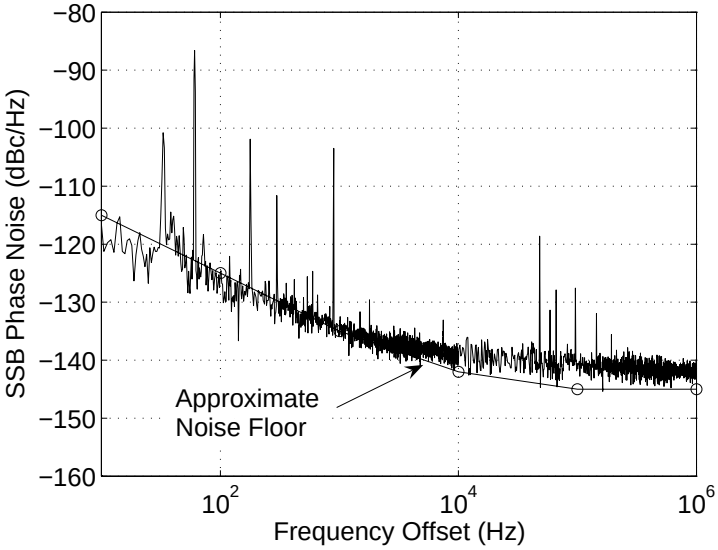


Figure 6.7: Phase noise measurements of a pair of LPN7100 (3dB subtracted for two devices) at 6GHz, the 30th harmonic. The measured phase noise and measurement noise floor were indistinguishable.

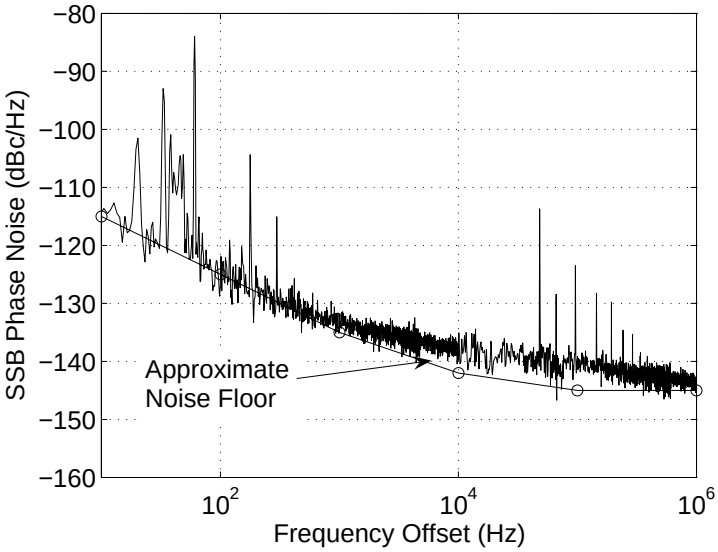


Figure 6.8: Phase noise measurements of a pair of LPN7100 (3dB subtracted for two devices) at 8GHz, the 40th harmonic. The measured phase noise and measurement noise floor were indistinguishable.

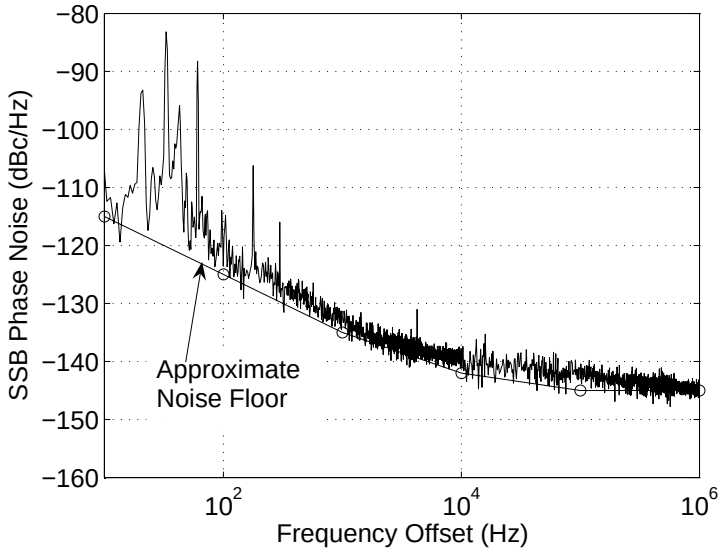


Figure 6.9: Measured phase noise at the 50th harmonic. The measurement was again indistinguishable from the measured noise floor. With a measured noise of -140dBc/Hz at 10kHz, the input referred phase noise is -20log10(50) or 34dB lower at -174dBc/Hz.

LPN7110 has a lower power output than the SRD, again due to bias conditions. The LPN7110 is able to be driven directly into a reflective filter without degradation of phase noise or loss in harmonic output.

A harmonic output comparison between the SRD and LPN7110 is shown in Fig. 6.11 and direct additive phase noise comparison of the SRD and LPN7110 is shown in Fig. 6.12. A Herotek GC200RC 200MHz SRD-based frequency multiplier is compared with the LPN7110 in an identical measurement system. Measurements of SRDs in literature have been completed at 8th and 11th harmonics. The noise is input referred based on a theoretical 20log 10N multiplication.

The additive phase noise measurement presented in Fig. 6.12 is at the fundamental and 10th harmonic, 200MHz and 2GHz, respectively. If near ideal multiplication is occurring within the device, the measured phase noise at the fundamental should be related by 20log 10N to the additive phase noise at the Nth harmonic or in this case, 20dB.

The results for the NLTL followed the expected 20log 10N when comparing the additive noise at 200MHz and 2GHz. This measurement, completed with several devices for verification, validates a hypothesis that NLTLs are near ideal 20log 10N multipliers and the noise at the fundamental is correlated with the noise at higher harmonics. This relation is extremely important for characterizing NLTLs in a timely fashion. Measurements at the fundamental only require a single device and are relatively quick to make. Measurements at the 10th harmonic require three devices and require significant setup. The consistent device behavior allow phase noise guarantees based on design rather than the sorting of devices through measurement.

The SRD exhibits a very unexpected effect. The noise of the SRD was nearly identical to that of the NLTL at 200MHz close to the carrier, and performed better at offsets greater than 10kHz. At 2GHz, the additive noise is a $40\log_{10}N$ relation instead of the expected $\log_{10}N$. SRD datasheets specify $20\log_{10}N$ behavior plus some additional

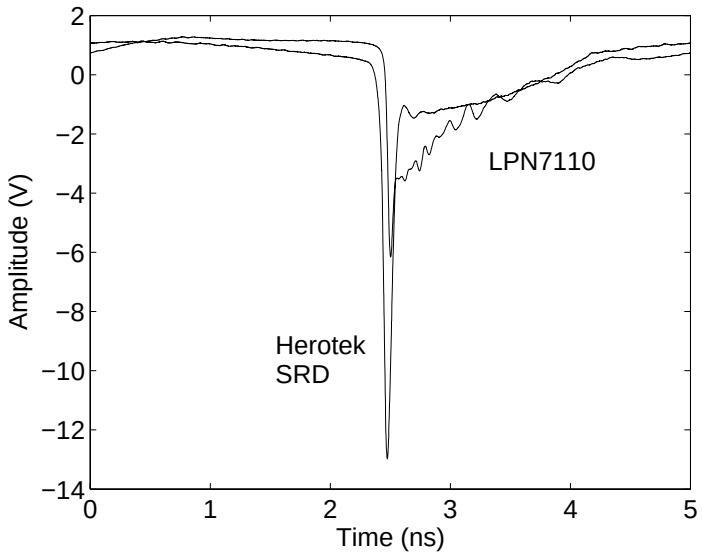


Figure 6.10: Time domain output of the LPN7110 high power NLTL from Picosecond Pulse Labs compared to the output of the Herotek GC200RC SRD. This is at 27dBm input for both devices. Step recovery diodes typically have higher output power than NLTLs. NLTLs are optimal for lower power input levels where SRDs no longer operate.

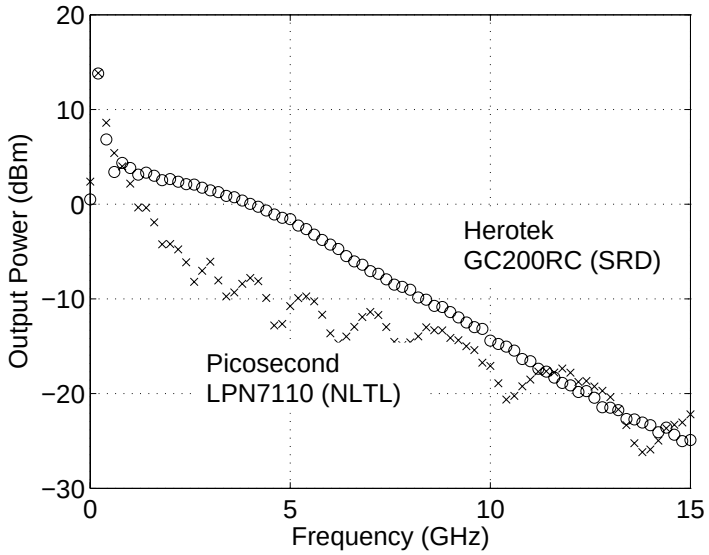


Figure 6.11: Harmonic spectrum calculated from time domain data of the SRD and NLTL. The SRD performs better in terms of output amplitude in the sub 10GHz range. Above 10GHz, NLTLs begin to surpass the SRD with the capability of having good harmonic content to 50GHz. SRDs are currently limited to about 20GHz.

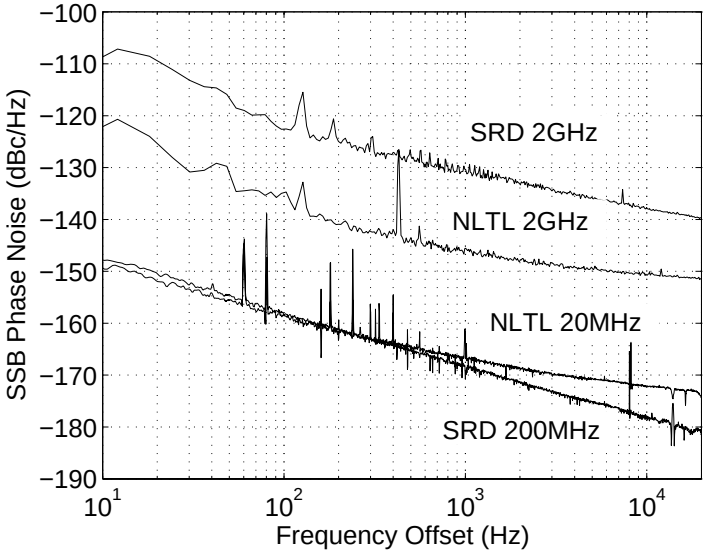


Figure 6.12: Phase noise comparison of the Herotek GC200RC and Picosecond LPN7110 with 24dBm input. Data is taken at the fundamental (200MHz) and at the X10 harmonic (2GHz). The NLTL demonstrates almost exact 20logN multiplication behavior, 20dB for a X10 device. The SRD is measured to have a 40dB increase for a X10 multiplication, or a $40\log_{10}$N relation.

noise, but data is given only at a single frequency under a specific conditions. What may be concluded from this measurement is SRDs may actually have a greater than $20\log_{10}N$ multiplication. If the relation is in fact a $40\log 10N$ relation, this implies a current noise multiplication processes internally in the SRD. Additional measurements with more devices would be required for confirmation. This is the first measurement that may identify the root cause of additional noise in SRD multipliers. It should be noted that the measurement setup can affect this result. However, the SRD in this situation was measured with a 6dB attenuator after the SRD and prior to the bandpass filter at 2GHz, providing a minimum of a 12dB match.

6.5 PN Junction Varactor NLTL Measurements

The phase noise measurements of the LPN7100 and LPN7110 exhibited superior phase noise of the NLTL as compared to the SRD at the 10th harmonic. Due to the proprietary nature of the Picosecond Pulse Lab parts, the uniformly distributed lumped element NLTL designed in Chapter 5 is used for the remainder of the NLTL characterizations.

The noise analysis from Chapter 5 suggests that high resistance biasing of the NLTL may improve the harmonic content of the NLTL for the same RF drive level as well as improve the additive phase noise if bypassed appropriately compared to a purely inductive bias to ground. The 8-stage uniform NLTL designed and simulated in Chapter 5 is used in the bias experimentation.

Time and frequency domain measurements of inductive bias to ground and a 2k resistance to ground are shown in Fig 6.13, 6.14, 6.15 and 6.16. Results show that the 2k bias has nearly twice the voltage out with harmonics improving by 15dB at 2GHz. The inductively biased and resistively biased line perform significantly better than the simulation results shown in Chapter 5. This is most likely due to a varactor model that was not created to operate near or in forward conduction, but reverse bias only.

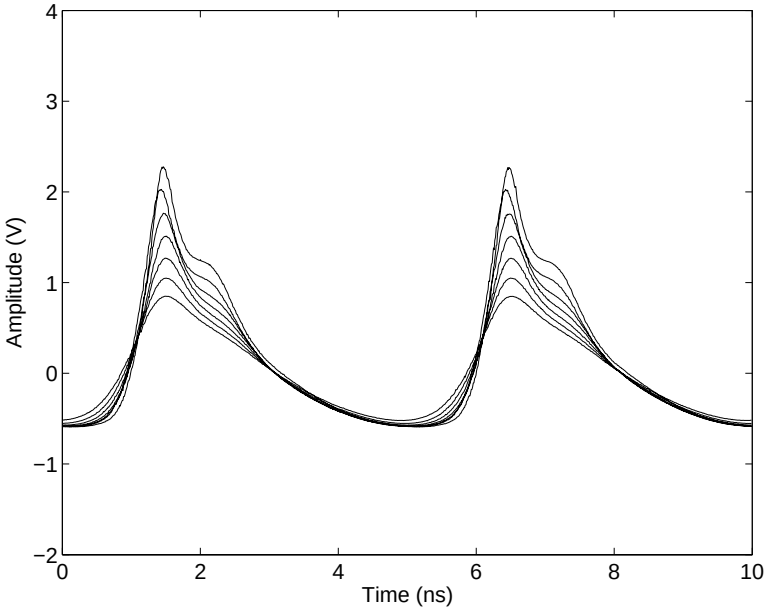


Figure 6.13: Time domain waveforms at the output of the 8-stage NLTL that is inductively biased. Input power is swept from 10dBm to 20dBm in 2dB increments and at 21dBm. The flat portion at the bottom of the trace is where the NLTL is in forward conduction.

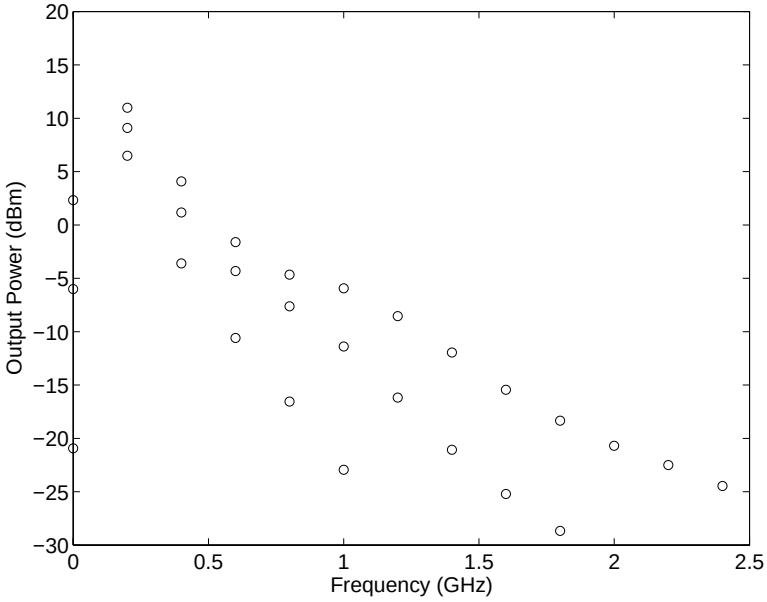


Figure 6.14: Calculated frequency domain harmonic power from the measured time domain data of the inductively biased NLTL. Data points are for power input levels of 10dBm, 16dBm and 21dBm. The inductively biased line is tolerant to driving reflective loads without adversely affecting the harmonic levels. The conversion efficiency is degraded, however.

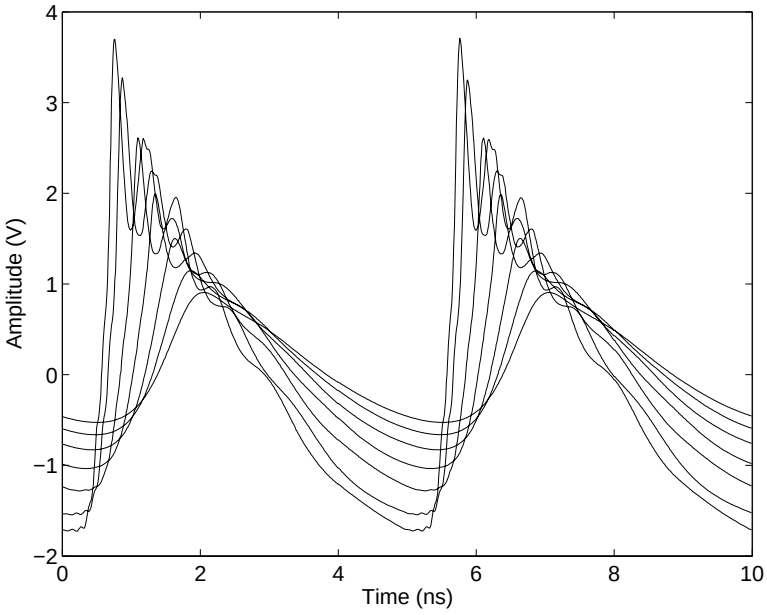


Figure 6.15: Time domain waveforms at the output of the 8-stage NLTL that is biased through a 2kΩ resistor. Input power is swept from 10dBm to 20dBm in 2dB increments and at 21dBm. The resistor bias uses the small rectification current to reverse bias the line and improve conversion efficiency. The NLTL is out of forward conduction a majority of the time. Forward conduction of the diodes is a dominant source of noise in the NLTL.

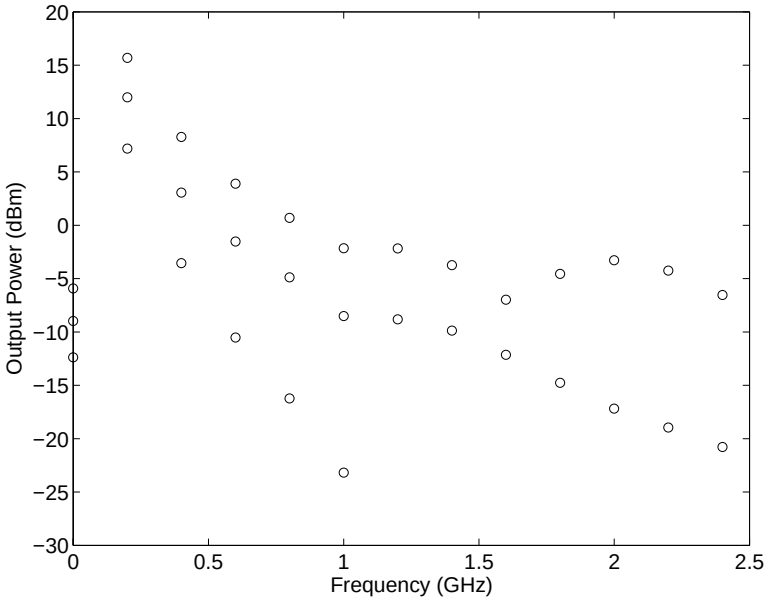


Figure 6.16: Calculated frequency domain harmonic power from the measured time domain data of the resistive biased NLTL. Data points are for power input levels of 10dBm, 16dBm and 21dBm. The dramatic increase in conversion efficiency to high harmonic power levels is apparent with a 15dB increase in the 10th harmonic level as compared to the inductively biased NLTL.

6.6 PN Junction Varactor NLTL Measurements

In this section, the effects of bias and phase noise at the fundamental are measured. The bias inductor on the line was terminated in following ways:

- open-circuit (self-biased line)
- short-circuit (inductor to ground)
- 2kΩ without bypassing
- 2kΩ with a 10uF ceramic capacitor
- 2kΩ with a 10uF ceramic capacitor in parallel with a 2200uF electrolytic
- 2kΩ with ten parallel 10uF ceramic capacitors

The data is discussed within the caption of each figure.

Comparison of the measured phase noise levels to that of the calculated values from Chapter 5 is as follows:

Parameter	Calculated Phase Noise	Measured Phase Noise
Inductively Biased NLTL	-174dBc/Hz	-177dBc/Hz
Unbypassed 2k Resistance	-163dBc/Hz	-163dBc/Hz
Bypassed 2k Resistance	-196dBc/Hz	-182dBc/Hz

Table 6.1: Calculated vs. Measured additive phase noise based on the bias parameter of interest. The calculations are from theory presented in Chapter 5. The measured noise floor of the inductively biased line and 2kΩ resisitively biased line are close to the calculated values. The bypassed 2kΩ line is limited by the noise floor of the system at -182dBc/Hz. The true noise floor is still unknown but lower than any previously published high order frequency multiplier. Improvements in the measurement system can improve the measurement sensitivity to approximately -190dBc/Hz

6.7 Chapter Summary

The additive phase noise measurements of the NLTL using the improved design techniques for biasing NLTLs is significantly better than any previously published. The

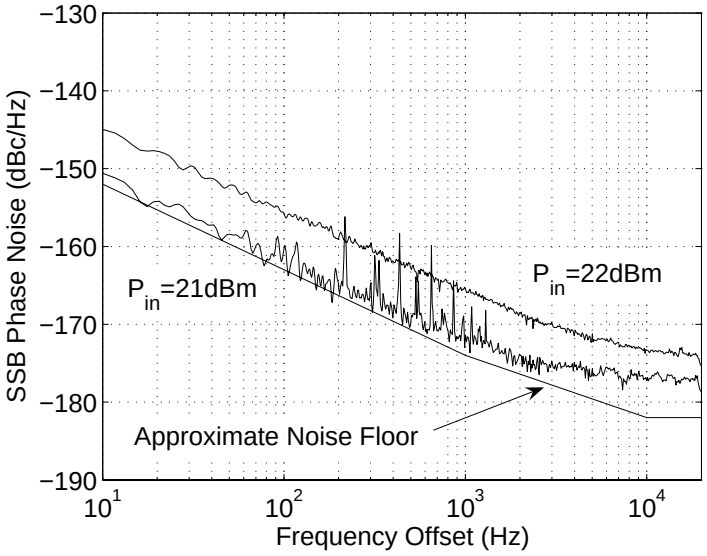


Figure 6.17: Additive phase noise measurements of the NLTL with inductor to ground biasing. Changing RF power levels can significantly change the flicker behavior of the device.

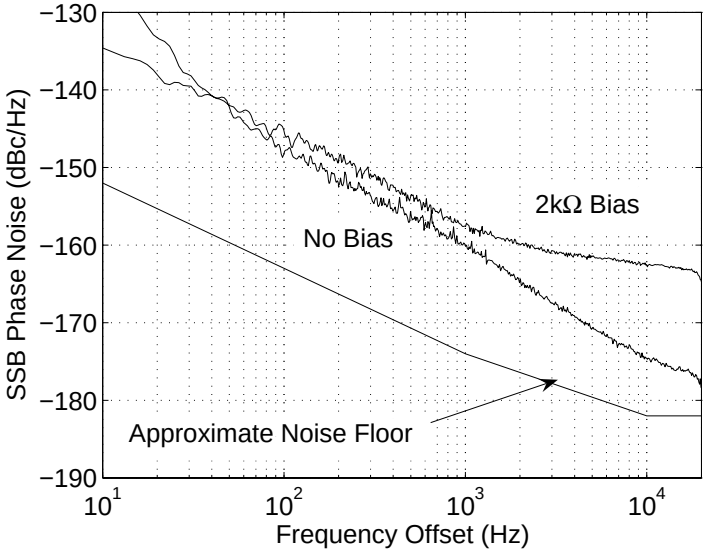


Figure 6.18: Additive phase noise measurements of the NLTL with no return path or self biased compared to being biased through an inductor and 2kΩ resistor to ground without bypassing. The resistor Johnson noise phase shifts the NLTL, causing excessive broadband phase noise.

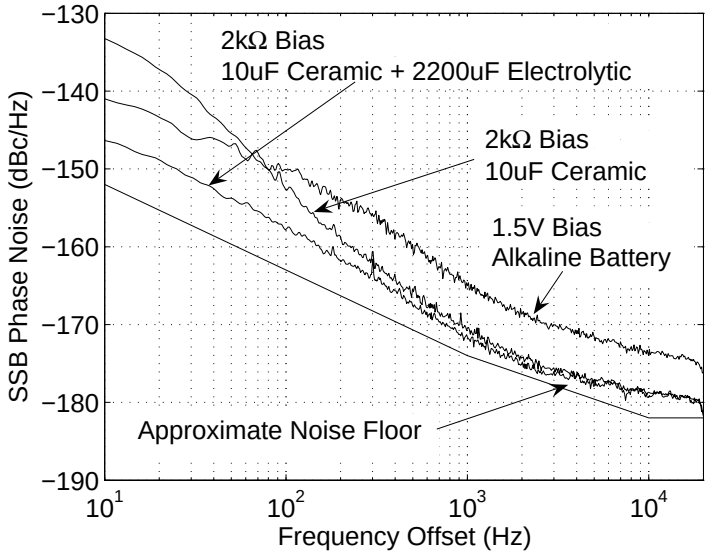


Figure 6.19: Additive phase noise measurements of the NLTL with bias through and inductor with bypassing in parallel with 2kΩ resistor to ground. The first case is a 10uF ceramic capacitor to ground. The cutoff frequency is 50Hz, where the phase noise begins to increase from modulation by the Johnson noise of the resistor. A 2200uF low voltage electrolytic capacitor was placed in parallel with the 10uF inductor, improving the close in phase noise but still showing more than 10dB decade phase noise degradation. This is most likely due to the high-ESR of the electrolytic capacitior, on the order of many ohms. The NLTL was also bias through the inductor, bypass with a 10uF resistor with a 1.5V alkaline battery. This is slightly higher than the 1.1V the line nominally self biases at and some noise was introduced. The origin is unknown.

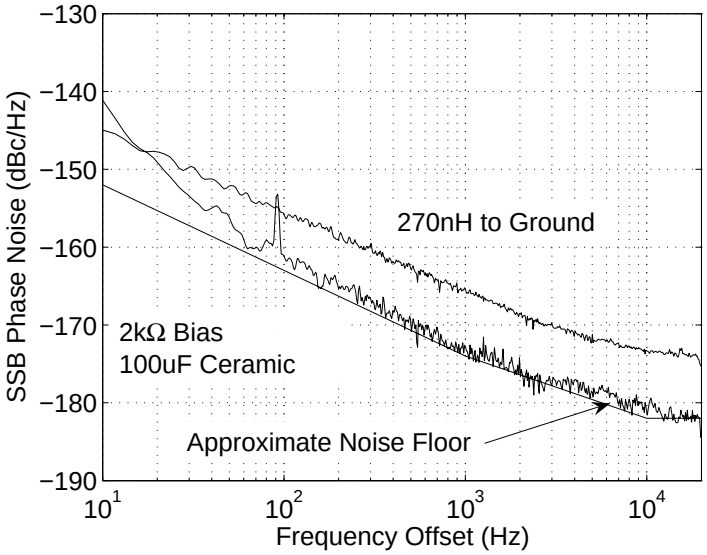


Figure 6.20: Additive phase noise measurements of the NLTL with inductor to ground biasing at 22dBm compared to an NLTL biased with an inductor and 2kΩ bypass with 10X 10uF ceramic capacitors for low ESR and 5Hz cutoff at 22dBm. This demonstrates that careful biasing can improve the fundamental signal to noise ratio.

design techniques to improve the efficiency improved the additive phase noise by using the rectified current as a reverse bias point. This significantly extends the state of the art in NLTL design as a frequency multiplier.

As the conclusive measurements to this thesis, the data presented in this chapter is evidence that NLTLs are as spectrally pure as diode doublers, exceeding the performance of SRDs while maintaining the useful qualities of high-order frequency multiplication. Optimization for harmonic output using a resistor and the diode's rectification current have been shown to be extremely effective at increasing the harmonic output of the diode and reducing phase noise when bypassed appropriately.

Chapter 7

Conclusions and Future Work

7.1 Thesis Summary

Three microwave components have been presented that extend the state of the art in low-phase noise source:

The miniature local oscillator presented in chapter 2 simultaneously decreases the size and power consumption while maintaining excellent phase noise compared with published and commercially available oscillators in the same frequency range.

Five measurement systems specific to characterizing phase noise in a variety of components are described in Chapter 3. Methods specific to measure frequency translation devices to very high harmonics and extremely low phase noise levels are designed, developed and characterized.

In Chapter 4, Class-E amplifiers are characterized for use as PAs in low-phase noise frequency sources. Correlation between AM-PM network measurements and additive phase noise are presented. The data leads to the conclusion that active devices may be specifically chosen based on linear parameters to achieve optimal additive phase noise in high-efficiency amplifiers. The optimization and characterization of a 48% efficient, ultra-low phase noise PA for driving frequency multipliers is included.

In Chapter 5 the noise contributions of three types of frequency multipliers, two-diode, SRD and NLTL are explained. Improvements to the NLTL harmonic output are simulated and discussed. The phase noise benefits of alternative bias for NLTLs is

hypothesized.

Extensive measurements on NLTLs and SRDs are shown in Chapter 6. Phase noise measurement results conclude that NLTLs are a superior alternative to step recovery diodes for low noise applications. Additionally, a noise multiplication phenomena was observed and quantified for the first time in the SRD multiplier and a hypothesis describing the source of this is presented. The phase noise contribution of bias conditions in NLTLs is proved. In Fig. 7.1 the phase noise contributions of the highest performing frequency multipliers are presented with the NLTLs measured in this work. Limited by the measurement system, the NLTLs exhibit phase noise comparable to the best frequency doubler measurement in literature. A 100MHz oscillator typically found in ultra-low phase noise multiplied sources is shown for reference. The NLTLs exceed SRDs significantly in phase noise, extending the state of the art.

7.2 Original Contributions

The author's original contributions throughout this work are:

- The adoption of the two port method for optimization of Q-factor in high-frequency, low-power and low-phase noise fundamental oscillator. The 4.6GHz oscillator has the best simultaneous size, phase noise, and DC power consumption in literature or commercially available.

- Quantified the noise added in class-E PAs as compared to class-A for MESFET and HBT devices. Network analyzer measurements of device AM-PM characteristics were shown to be proportional to the additive phase noise of the devices.

- A low-cost cross correlation system was developed for use in characterizing ultra-low added phase noise frequency multiplication circuits with a sensitivity of -186dBc/Hz. A measurement system capable of measuring the added phase noise

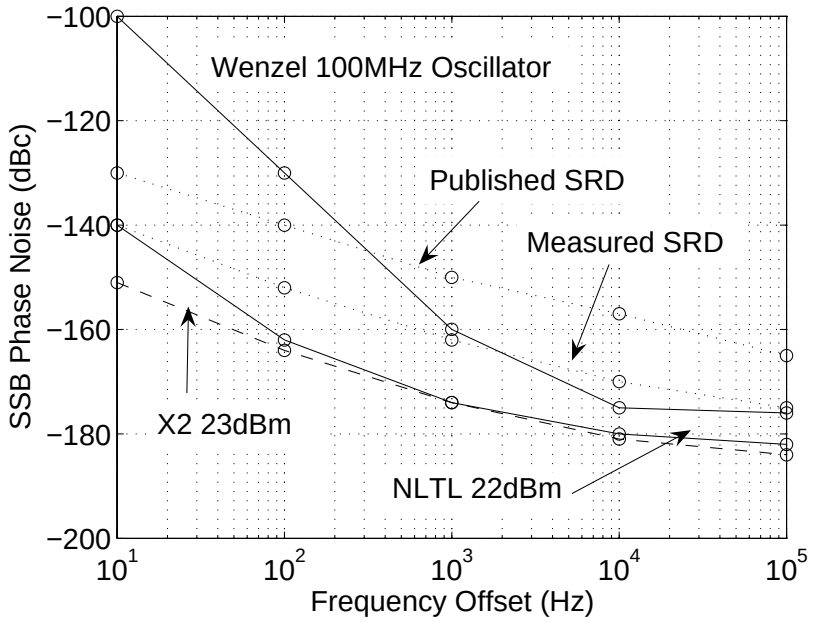


Figure 7.1: Input referred phase noise of state of the art multipliers with ultra-high spectral purity 100MHz Wenzel oscillator. NLTLs developed in this thesis are near the state of the high drive diode doublers and exceeding the performance of Step Recovery Diodes. Input referred phase noise of NLTLs is well below that of state of the art 100MHz references.

of a frequency multiplier at the 90th harmonic with input referred sensitivity of -175dBc/Hz.

- The noise theory of nonlinear transmission lines is presented for the first time with evidence of superior performance over step recovery diodes. Bias conditions are explored as a method to improve harmonic output power and phase noise simultaneously.

- Measured results of NLTL with optimal bias conditions is presented. Proof that NLTLs exhibit superior phase noise performance over SRD based multipliers is presented. NLTLs are measured to have spectral performance similar to a high level silicon diode frequency doubler with an input referred phase noise of -181dBc/Hz at 10kHz offset.

7.3 Proposed Future work

Proposed future work is listed as follows:

- Extensive characterization of alternative diodes for NLTL frequency multipliers. A joint microwave and device physics research project lead to improved noise prediction methods and the designs for optimum phase noise.

- Improved correlation between noise measured near DC of a single diode and the additive noise of an NLTL when used as a frequency multiplier.

- Optimization of the class-E PA design for improved phase noise.

- Combining load-pull measurements with added phase noise measurements to find optimal additive phase noise contours in addition to optimal efficiency contours, leading to a improved compromise between efficiency and phase noise.

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