Efficiency Enchancement Techniques for the Outphasing Power Amplifier

by

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Efficiency Enchancement Techniques for the Outphasing Power Amplifier

Thesis directed by Professor Zoya Popović

Modern communication and radar signals increasingly utilize signals with high peak-to-average power ratios to achieve spectral efficiency. Three power amplifier architectures have been developed to efficiently amplify such signals one of which is outphasing. At high frequencies, such as X-band, outphasing requires enhancement in the form of discrete supply modulation or rectification to achieve performance competitive with alternatives such as Doherty and envelope tracking. This thesis focuses on the development, theoretically and experimentally, of the outphasing power amplifier, including enhanced modes of operation.

A novel quasi-MMIC outphasing PA and measurement setup are developed to enable the direct measurement of power waves internal to the PA architecture, yielding internal PA performance and load modulation. Due to the flexibility of the PA prototype and measurement setup, both isolated and non-isolated combiners are utilized with and without discrete supply modulation. Insight into the dynamic operation of five outphasing variations is gained.

Two enhanced outphasing PAs are fully integrated on GaN MMICs. A power recycling LINC PA makes use of the duality between a high efficiency PA and rectifier to recover power wasted in the isolated combiner. A multi-level Chireix outphasing PA utilizes discrete supply modulation to minimize DC power consumption, thereby improving efficiency at back-off. Realistic testing with a GaN discrete supply modulator MMIC shows particular promise for the novel multi-level Chireix outphasing architecture.

Finally, the importance of the gain of power amplifiers internal to the outphasing architecture is substantiated in simulation and measurement. Highly efficient multi-stage power amplifiers are optimized through the development of harmonically terminated interstage matching networks.

Dedication

To my gracious God.

Acknowledgments

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Chapter 1

Introduction

Contents

The work presented in this thesis attempts to solve the challenge of efficiently amplifying a high peak-to-average ratio signal, through the application and development of the outphasing power amplifier architecture. The importance of this challenge corresponds to the critical role of the power amplifier (PA) in a wireless transmitter, shown in Fig. 1.1. As the final active element in the chain, the power amplifier is tasked with increasing the signal strength in order to overcome exponential free-space losses to reach the receiver.

In all applications, the efficiency of the PA has a significant effect. At high power levels, such as base stations (hundreds of watts) or ground-based radars (millions of watts), low PA efficiency means high power dissipation in the form of heat. Not only is this power lost, but power hungry cooling solutions must be provided to avoid hardware failure, compounding the issue. Even at low power levels, such as in cell phones (watts), low PA efficiency corresponds to shorter battery life.

Although the linearity of the PA significantly affects many wireless applications, such as the accurate transmission of data in communication systems, this thesis focuses on the efficiency of the PA. In this

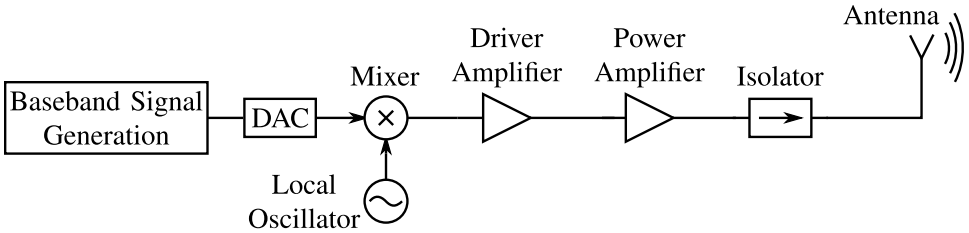


Figure 1.1: Wireless transmitter block diagram. The modulated signal is generated digitally at baseband for the desired application, before being converted to the analog domain. After it is upconverted to the carrier frequency, it is amplified by several linear gain stages and finally, the power amplifier, before it is converted to a free-space traveling wave by the antenna.

introductory chapter, Section 1.1 provides background information to understand the amplification challenges as well as motivation for the outphasing architecture. An outline of each chapter and corresponding contributions is given in Section 1.2.

1.1 Background and Motivation

1.1.1 Communication Signals

The development of modern communication signals has been driven by spectral efficiency, packing as much data into as little bandwidth as possible. The continued explosion of wireless electronics increases the demand on the wireless infrastructure [1, 2]. As the smart phone gets smarter, and an entourage of other devices are added to it, users demand increasing amounts of data.

Unfortunately, that data must be transmitted through a limited resource, the electromagnetic spectrum. In order to maintain the quality of transmission for all users, the Federal Communications Commission (FCC) allocates the spectrum and regulates the non-federal portion [3]. While the emission of a transmitter within its allocated channel is enforced, the emission in adjacent channels is more important and challenging. Spectral regulation is enforced by an emission mask, as demonstrated in Fig. 1.2b and Fig. 1.2a. The mask designates the required attenuation of emission outside of the allocated channel for a given application or transmission standard, such as LTE [4].

Modern communication signals are distinguished by their modulation schemes, corresponding to the parameter of variation for the encoding of data: amplitude, frequency, phase, or any combination thereof.

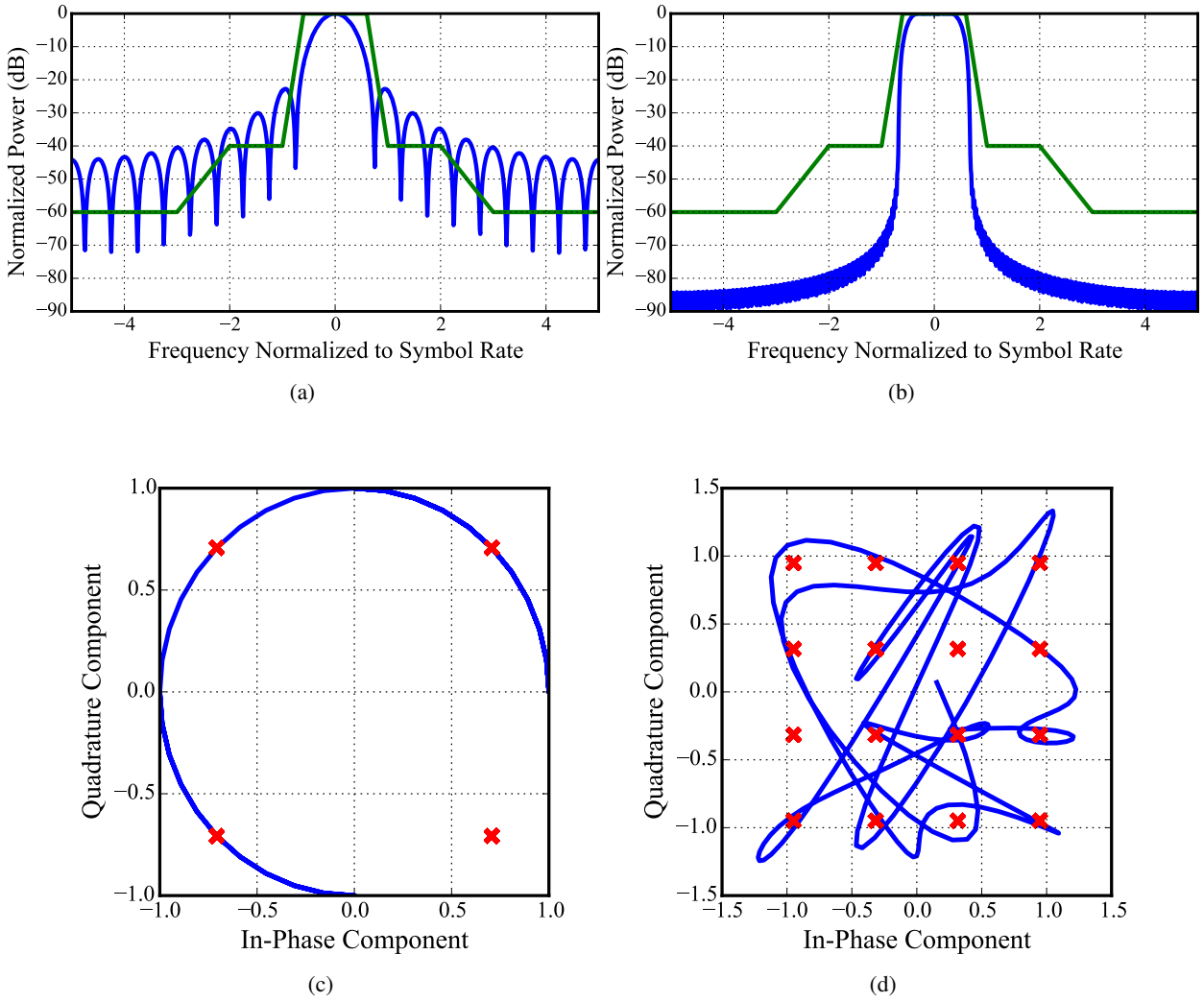


Figure 1.2: (a),(b) Spectra of MSK and QAM signals, respectively, with an example of an emission mask. (c), (d) Constellation diagrams (red x's) corresponding to 10 symbol MSK and QAM signals, respectively. The blue line represents a time Δt of the continuously received signals corresponding to 20 symbols.

Thus, the development of signals for the purpose of spectral efficiency involves finding the optimal modulation scheme for a given application. Development also includes various digital encoding schemes, as well as filtering.

A comparison of two signals in Fig. 1.2 will demonstrate the challenges of modern communication signals without going deeply into communication theory. In both cases, the signals are filtered with a root-raised cosine filter, with the rolloff parameter, α, set to 0.35. In (a) and (c), the spectrum and constellation are shown for the minimum-shift-keying (MSK) modulation scheme, in which the phase is continuously varied.

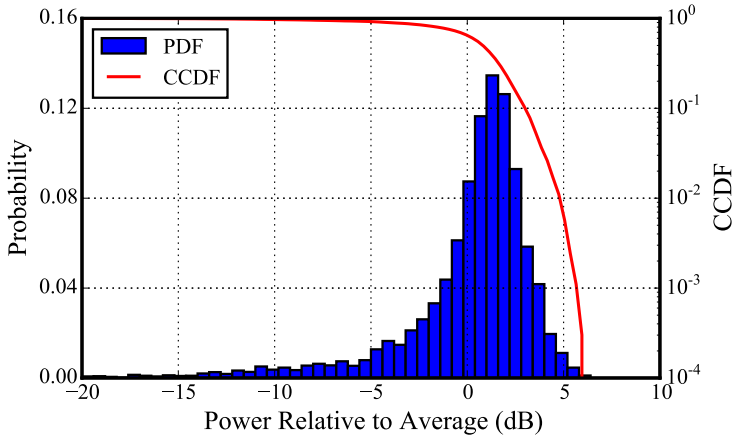


Figure 1.3: PDF and CCDF of a 4-QAM signal, demonstrating a 6 dB peak-to-average ratio.

A constellation diagram demonstrates the symbol or bit representation of the complex signal. The red x's denote symbols, which are encoded bit sequences. The received signal (blue) is sampled in the time domain, and the bits corresponding to the nearest symbol are received. As seen in the constellation diagram, an MSK signal has a constant amplitude and only four symbols. The MSK spectrum is unable to meet the mask requirements, demonstrating large side-lobes leading to significant emissions in adjacent channels. While applications for MSK exist, this modulation scheme is not spectrally efficient.

The quadrature-amplitude-modulation (QAM) scheme, on the other hand, has been developed for spectral efficiency. The spectrum and constellation for a 16-QAM signal are shown in Fig. 1.2b and Fig. 1.2d, respectively. In this case, the constellation diagram includes 16 uniquely encoded symbols, corresponding to a higher data rate. More importantly, the signal demonstrates both amplitude and phase variation. The combination of these two varying parameters enables the adherence to the emission mask due to a steep rolloff of the side-lobes.

The takeaway from the comparison of the MSK and QAM signals is that spectrally efficient signals have both amplitude and phase modulation. To understand the importance of these signal characteristics, the statistics of a signal are helpful. Fig. 1.3 shows the probability density function (PDF) and complementary cumulative distribution function (CCDF) for a 4-QAM signal. Both are measures of the probability that the signal will exhibit given amplitude. Importantly, the distributions show that the peak amplitude will be 6 dB

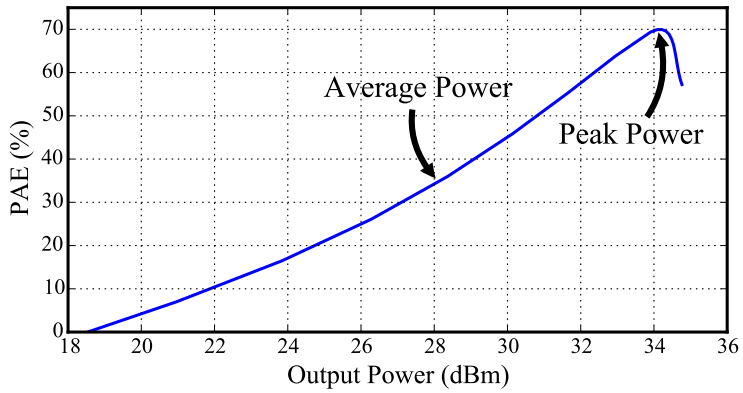


Figure 1.4: Non-ideal class-B GaN MMIC PA efficiency as a function of output power, demonstrating poor efficiency roll-off with output power typical of single ended PAs.

higher than the average. This metric is called the peak-to-average power ratio (PAR or PAPR). Therefore, spectrally efficient signals tend to have a large PAR. For example, an LTE signal will have a PAR between 11 and 12 dB.

The discussion on signals thus far has not considered the transmitting hardware, specifically the power amplifier. The amplitude variation described by the PDF of the signal, performs a weighting function on the efficiency characteristic of the PA, shown in Fig. 1.4 for the class-B GaN MMIC PA described in Section 2.2. Therefore, the PA will operate near the average power level at low efficiency for the majority of the time, and at peak power and efficiency a limited amount of time. In an average sense, the efficiency of traditional PA classes is low, because the efficiency decays rapidly with output power. The difference between any output power level and peak power is often used to describe reduced output power levels, using the term back-off. Thus, 0 dB back-off is peak power, while the average power level for a 6 dB PAR signal will be at 6 dB back-off. This normalized description of power aids in comparing performance for high PAR signals.

1.1.2 Radar Signals

Modern radars share the spectral efficiency challenge with communication systems, due to increasingly strict mask requirements described in the Radar Spectrum Engineering Criteria (RSEC) [5], and regulated by the National Telecommunications and Information Administration (NTIA). Traditionally, radars transmit rectangular pulses through a class-C amplifier to achieve high hardware efficiency due to the switching nature

of class-C operation [6]. From Fourier analysis, the rectangular pulse shape in the time-domain corresponds to a $\text{sinc}^2(x)$ frequency-domain response, leading to large out-of-band emissions [7]. In order to meet mask requirements, a different pulse shape can be selected [8,9]. The Gaussian pulse shape has been demonstrated in [10, 11] as a spectrally efficient envelope waveform. In adjusting the pulse shape for spectral efficiency, the signal develops amplitude modulation and thus a PAR, presenting the same problem as communication signals.

1.1.3 High Efficiency Power Amplifiers

Efficiency enhancement of power amplifiers has been and continues to be widely researched, due to the large percentage of total transmitter power consumed by the power amplifier. As such, resources that treat the topic more comprehensively than this brief introduction are available in [12–14]. Amplifier classes are defined uniquely by the voltage and current waveforms at the intrinsic drain, which is the current source node internal to the transistor model. The overlap of these waveforms corresponds to the power dissipated in the transistor, and thus should be minimized to maximize efficiency. The waveform definitions directly determine the required harmonic loading conditions at the output of the device.

Reduced conduction classes improve the efficiency by lowering the bias voltage, and subsequently the quiescent current. The intrinsic drain waveforms for classes B and C are shown in Fig. 1.5. Notice that the quiescent drain current, I_{DQ}, is lower in class-C compared to class-B, corresponding to a decreased power dissipation. The peak drain efficiency of class-B operation is 78.5%, with class-C reaching 100% theoretically [12]. Reduced conduction classes require a short circuit load at all harmonic frequencies.

Harmonic terminations other than a short circuit can be utilized to shape the intrinsic drain waveforms and improve efficiency. In Fig. 1.6 for example, class-F and inverse class-F PAs utilize open circuit terminations at the third and second harmonics, respectively, to square the voltage and current waveforms, respectively [12, 15]. In both cases, the non-square waveform is an approximate half-sinusoid. Theoretically, no power is dissipated in the transistor, and the drain efficiency peaks at 100%. Combinations of harmonic terminations can provide desired characteristics, as found when mixing class-E and inverse class-F operation [16].

The intrinsic drain waveforms, defining each PA class, are only defined at a single input power, typically

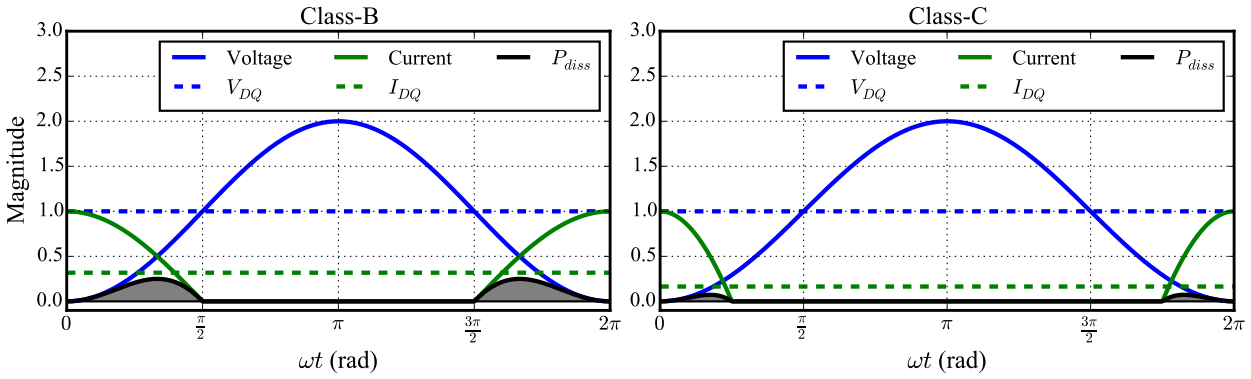


Figure 1.5: Intrinsic drain voltage and current waveforms, along with dissipated power for (a) class-B, and (b) class-C operation.

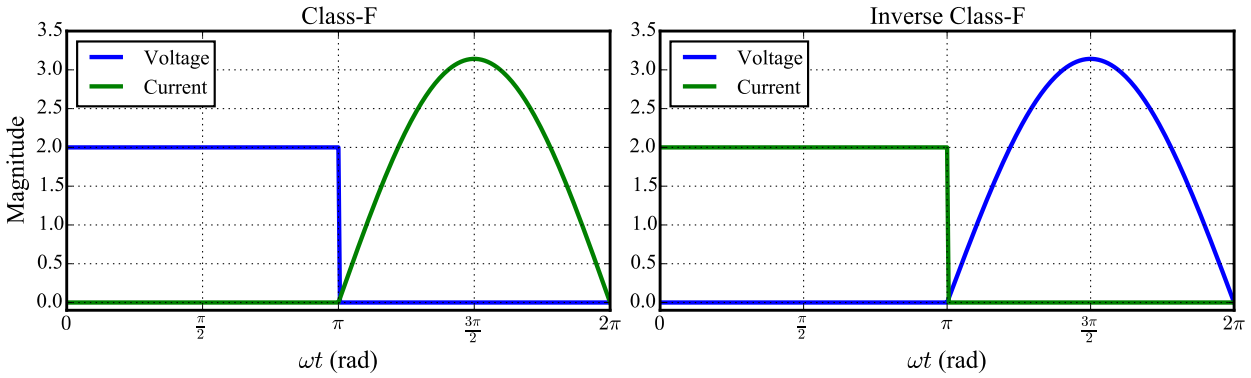


Figure 1.6: Intrinsic drain voltage and current waveforms for (a) class-F, and (b) inverse class-F operation.

enough to saturate the transistor. At lower input power levels, the optimum intrinsic drain waveforms are lost along with the efficiency improvement. Therefore, high efficiency PA classes do not, in and of themselves, efficiently amplify high PAR signals.

1.1.3a Efficiency Definitions

The following is a list of common PA efficiency definitions used in this thesis:

Drain Efficiency is the ratio of RF output power to DC supply power:

$$\eta_d = \frac{P_{out}}{P_{DC}} \tag{1.1}$$

This definition does not account for RF input power, which may be significant if the gain is low, as is often the case for high efficiency PAs that operate in saturation. Sometimes, this definition is referred to simply as "efficiency".

Power-Added Efficiency takes into account the RF input power:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{1.2}$$

PAE will always be less than drain efficiency, but as the gain increases the two definitions converge.

Total Efficiency is the ratio of the RF output power to the total input power, DC and RF:

$$\eta_{tot} = \frac{P_{out}}{P_{DC} + P_{in}} \tag{1.3}$$

Total efficiency also takes the RF input power into account. This definition is better suited for outphasing than PAE, because PAE becomes less than zero when $P_{out} > P_{in}$, which occurs in outphasing PAs.

Average Efficiency is required for modulated signals, which have varying output power and thus varying instantaneous efficiency. This definition is used in conjunction with one of the previously defined efficiencies, taking the average of the included powers. For example, the average drain efficiency is defined as:

$$\eta_{avg} = \frac{P_{out,avg}}{P_{DC,avg}} \tag{1.4}$$

ΔP_{out} is the output power range over which the efficiency remains within 10 points of its peak value. This definition is used solely in this work for the comparison of several outphasing PA architectures.

1.1.4 High Efficiency Power Amplifier Architectures

Instead of controlling the output power of the PA by modulating the input power, the input power can be fixed to saturate the PA, resulting in an equivalent circuit shown in Fig. 1.7. The transistor operates at high efficiency, and can be simplified to a switch. The output power of this circuit across the load is:

$$P_{out} = \frac{V_D^2}{2R_L} \tag{1.5}$$

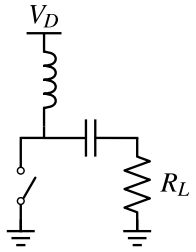


Figure 1.7: Simplified circuit for saturated power amplifier.

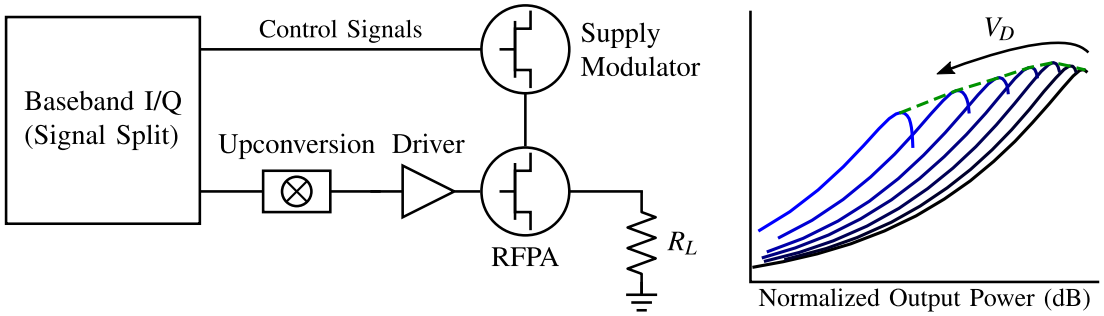


Figure 1.8: Supply modulation block diagram and efficiency. In this architecture, the modulated signal is split into high and low frequency paths. At low frequency (modulation bandwidth), the supply modulator varies the supply for the high frequency PA, to maintain efficient operation.

Two parameters can be modulated in order to control the output power: drain voltage, and load resistance. Three PA architectures have been developed to efficiently amplify high PAR signals by varying the supply or load: supply modulation [17], Doherty [18], and outphasing [19]. In all three cases, two amplifiers are required to modulated the desired parameter. Often, one or both of these amplifiers is chosen to operate in a high efficiency class. Thus, the term architecture is used to designate a system level combination of PAs.

A PA architecture based on the variation of the drain voltage is called supply modulation, shown in Fig. 1.8, where a low frequency amplifier modulates the bias point of the high frequency PA to which it is supplying power. Depending on the signal split between the high and low frequency paths, this architecture takes on various forms, including envelope elimination and restoration (EER) [17], envelope tracking [20], and polar [13,21,22]. The improvement in efficiency comes from reducing the power dissipated in the radio-frequency (RF) PA by minimizing the supplied power with the RF PA output power reduction, according to the dependence of the RF PA efficiency upon supply voltage, shown in Fig. 1.8. A continuous supply modulator (SM) follows the trajectory formed by the peaks of each replicated RF PA efficiency curve, thereby greatly

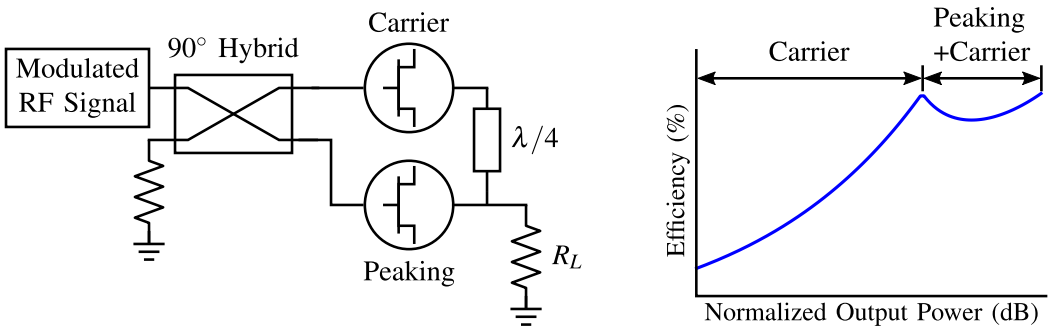


Figure 1.9: Doherty bock diagram and efficiency. This architecture combines two, asymmetric PAs. At low input powers, the peaking amplifier is off, and the carrier amplifier operates. As input power increases, the peaking amplifier turns on, modulating the loads of both PAs to maintain saturation and high efficiency.

improving the efficiency at back-off compared to a constant supply. This architecture can be as reconfigurable as its amplifiers. The bandwidth limitation often occurs for the continuous supply modulator, but techniques for assisting a highly efficient switching modulator with a cascode amplifier extend bandwidth [23, 24].

The Doherty PA architecture is dependent upon two asymmetric high frequency PAs, called the carrier and peaking amplifiers, which are traditionally biased in class-AB and C, respectively [25]. At low input powers, the input voltage swing is not enough to turn the peaking amplifier on, so it appears as an open circuit. Thus, the carrier amplifier provides class-AB amplification and efficiency into a nominal load, R. As the input power increases, the peaking amplifier turns on, causing its load to decrease from infinity toward $R/2$. The carrier amplifier load decreases toward $R/2$ as well, maintaining saturation and high efficiency, as shown in Fig. 1.9. The impedance inverter in the combiner causes the carrier amplifier load to decrease, as required, rather than increase [26]. The Doherty PA is an elegant solution, because it does not require upconversion, but has a high frequency input. The bandwidth of this architecture is limited by the frequency dependence of the quarter-wave transformers, but recent work has sought to overcome this limitation [27–30].

The PA architecture researched in this thesis is outphasing, which is dependent upon the interaction of two symmetric high frequency PAs through a non-isolated combiner. In this case, the input amplitude is held constant, and the load modulation is controlled by differential phase modulation of the input voltages. The common current in the non-isolated combiner causes the loading of the internal PAs to vary. The efficiency performance, specifically the peak at back-off, is dependent upon the design of the combining network. Because the loading is reactive in outphasing, as opposed to the real loading in the Doherty

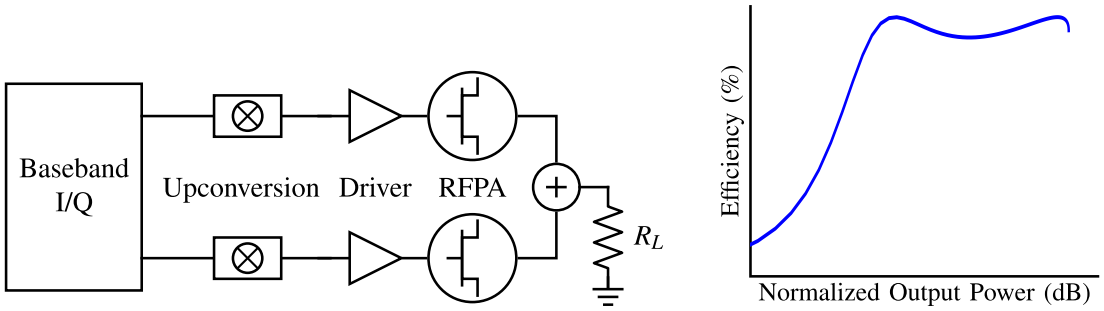


Figure 1.10: Outphasing block diagram. In this architecture, two symmetric high-frequency PAs interact through a non-isolated combiner. Differential phase modulation at the input controls the output power through the interaction between PAs.

PA, performance is best when reactive compensation is used in the combiner [19]. The phase modulator may be implemented digitally, in CMOS, as done in [31], where a 100 MHz LTE signal is modulated and upconverted to 10 GHz. Recently, the amplitude to phase modulation conversion has been incorporated into the input matching network at high frequency [32], yielding an elegant RF amplifier solution.

A variation of outphasing called LInear Amplification with Nonlinear Components (LINC) makes use of an isolated combiner at the output [33]. The LINC PA architecture was developed for linear, not efficient, amplification. Because the combiner isolates the internal PAs, load modulation is suppressed and does not control the output power. LINC is based on vector decomposition at the input, and vector combination at the output to reconstruct the signal envelope. The internal PAs do not contribute nonlinearities to the system, because they are driven at a constant input power.

1.1.5 DARPA Microscale Power Conversion Program

The majority of the work presented in this thesis was performed as a part of DARPA's Microscale Power Conversion program [34], which had two focuses. The first was the development of GaN-on-SiC transistors for both high efficiency RF power amplifiers and switching power electronics. This goal was tackled by the foundry at Qorvo (TriQuint at the time), as well as HRL. The second objective was the development of innovative X-band RF transmitters, with the goal of achieving 75% average efficiency with 500 MHz of modulation bandwidth at 5 W of output power. The author was fortunate to be a part of the Rockwell Collins team, focusing on the outphasing architecture.

1.2 Thesis Organization

The work presented in this thesis focuses on the understanding and development of five variations of the outphasing power amplifier architecture theoretically and experimentally. The content of each chapter is summarized by the following:

Chapter 2: The load modulation based operation of the Chireix outphasing power amplifier is examined both theoretically and experimentally at 10.1 GHz. A measurement setup is devised to directly measure the internal PA performance and load modulation within a Chireix outphasing PA. A hybrid Chireix outphasing PA is developed with GaN MMIC internal PAs and off-chip combining that includes bi-directional couplers to enable the measurement of power waves internal to the architecture. A brief introduction to the fundamentals of GaN MMIC design is presented, and the practical issues of designing a Chireix combiner for desired load modulation are discussed. A small signal analysis of the non-isolated combiner yields useful design equations.

Chapter 3: The linear amplification of the LINC PA architecture, a subset of the outphasing architecture, is the focus. The theoretical foundation for the input signal processing common to all outphasing amplifiers is presented. The internal PA performance and load modulation measurement setup developed in Chapter 2 is extended to the LINC PA through the use of an isolated combiner, highlighting the linear but inefficient amplification of the LINC PA.

Chapter 4: Discrete supply modulation is combined with the LINC PA architecture for significant efficiency improvement. The theoretical understanding of this combination is developed for symmetric and asymmetric supply modulation. The internal PA performance and load modulation measurement setup from Chapter 3 is extended through static variation in the drain voltage of each internal PA.

Chapter 5: Discrete supply modulation is combined with the Chireix outphasing PA architecture for the first time in literature. The internal PA performance and load modulation measurement setup from chapter 2 is extended to include static variation in the drain voltage. The combiner design equations

derived in Chapter 2 are shown to accurately predict load modulation distortion due to internal PA power imbalance. A supply modulated Chireix outphasing GaN MMIC PA is designed and measured at 9.7 GHz with a GaN discrete supply modulator.

Chapter 6: Microwave rectification is incorporated with the LINC PA architecture in order to recycle wasted RF power, improving efficiency. The duality between high efficiency power amplifiers and high efficiency, self-synchronous rectifiers is confirmed experimentally at 10.1 GHz on two GaN MMIC PAs described in [35] and leveraged for this architecture. The entire architecture is implemented on a GaN MMIC (internal PAs, rectifier, and isolated combiner) at X-band.

Chapter 7: Due to constant input power levels in the outphasing PA architecture, high efficiency, multi-stage PA design is investigated, since increased internal PA gain decreases the significance of the input power. The focus of this chapter is on the development of harmonically terminated interstage matching networks.

Chapter 8: Summarizes the contributions of this work and presents a path forward for future work.

Chapter 2

Chireix Outphasing

Contents

Outphasing was first introduced by Henri Chireix in 1935 [19] in order to reduce the operating costs of the PA in amplitude modulated (AM) broadcast stations, which had become the dominant expense as the power on carrier-wave operation exceeded 100 kilowatts. Aside from the fact that he was working with tube amplifiers at the time, Chireix brought up PA architectures still being discussed and researched today. He compared two approaches, corresponding to the node of the amplifier being varied for output power control. The grid can be modulated to control the output power, as in traditional power amplifier classes. Alternatively, the anode can be modulated by a low frequency, high power amplifier, as in popular envelope tracking techniques today. Although reduced conduction classes (B or C) as well as those incorporating harmonic shaping (F or F^{-1}) improve efficiency at peak output power, no efficiency improvement is achieved

at reduced input (grid) drive levels. Under supply (anode) modulation, the efficiency of the power stage remains high, but the envelope modulator must be able to supply high power while linearly tracking the amplitude variations in the signal. Therefore, Chireix proposed a new amplifier architecture based on load modulation called outphasing, whereby the output power is manipulated through variation in the differential phase between the two internal power amplifiers.

The outphasing architecture found commercial success when RCA chose to implement it in their Ampliphase AM broadcast transmitters in the 1950s and 1960s [36, 37]. It was reintroduced by D.C. Cox under the name LInear Amplification with Nonlinear Components (LINC) in 1974 [33]. Unfortunately, Chireix outphasing and LINC are commonly interchanged terms today, despite the drastic differences. The LINC amplifier was developed for linearity, not efficiency, as it utilizes an isolated combiner at the output, and does *not* operate by load modulation.

The outphasing technique has resurfaced in research today as modern signals have incorporated significant amplitude modulation, and signal processing capabilities have improved. The new efforts have mainly focused on the two RF components, the internal PAs and the combiner. A simulation-based study has been performed to evaluate various amplifier classes under load modulation during outphasing operation [38] by determining the PA classes that best approximate a voltage source, which exhibits constant output voltage swing with load variation. Voltage-mode class-D and class-F are good candidates, while current-mode class-D and inverse class-F are not. Class-E is mistakenly dismissed without evaluation. Chireix outphasing has been demonstrated with class-B [39–42], class-C [19], class-D [43, 44], class-E [45–50], class-F [51–53], and inverse class-F [54] internal power amplifiers, all of which operate at 2.14 GHz with up to 90 W of power, except for a single work at 5 GHz [51] with less than 1 W.

Although recent combiner innovations have utilized microelectromechanical systems (MEMs) [55], composite right/left handed (CRLH) transmission lines [56], tunable capacitances [57], and diodes [52], passive combiners with reactive compensation have remained most popular and effective [39, 40, 48, 51, 54, 58, 59], spurring many works on design optimization [39, 41, 60–63].

Understanding the interaction between the internal PAs and combiner during outphasing operation is critical, since it determines performance of the system. Unfortunately, the analyses describing these dynamics

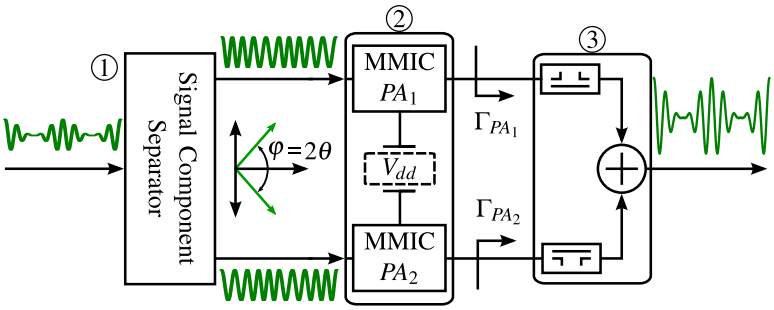


Figure 2.1: Flexible, MMIC-based outphasing block diagram with off-chip combiners that include bi-directional couplers for the direct measurement of power waves, enabling internal PA performance and load modulation measurement.

are very idealized, defining the load modulation without consideration for parasitics at the intrinsic drain reference plane, which is typically inaccessible in simulation or measurement. The purpose of the work presented in this chapter is to expand upon the theoretical understanding through direct measurement of load modulation in an outphasing PA as well as the performance of the internal PAs under load modulation.

In order to accomplish this purpose, a quasi-MMIC outphasing PA, shown in Fig. 2.1, is constructed from high efficiency GaN MMIC internal PAs and an off-chip combiner, which includes bi-directional couplers for the direct measurement of power waves internal to the outphasing PA. Section 2.1 details idealized theory of operation for Chireix outphasing. In Section 2.2, the design of a high efficiency GaN MMIC PA for use within several outphasing variations in this chapter and those following is detailed. The design of a Chireix combiner to enable measurements internal to the outphasing PA is described in Section 2.3. Finally, the internal PA performance and load modulation measurement setup and results are presented in Section 2.4.

2.1 Chireix Outphasing Theory

The simplest theoretical explanations of outphasing [12, 19], have been expanded to consider voltage source resistances [39, 42], ideal class-B internal PAs [64, 65], and ideal class-E internal PAs [66]. Outphasing operation based on load modulation is demonstrated theoretically in this section for the cases of simple (no reactive compensation) and Chireix outphasing (reactive compensation). Signal generation and drive is the same for all outphasing variations discussed in this thesis, and is described in Section 3.1 because LINC theory explains the generation of the differential phase from the amplitude modulation of the input signal

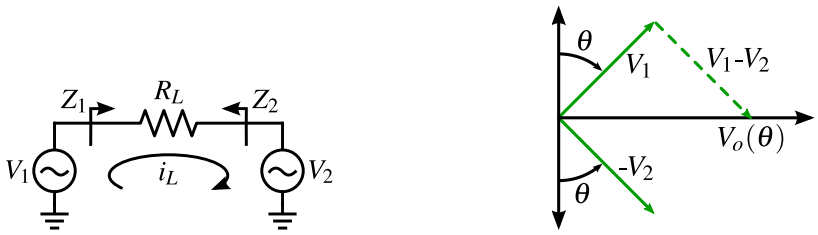


Figure 2.2: (a) Simple outphasing circuit diagram, and (b) vector representation of idealized voltage sources.

more clearly.

The simple outphasing circuit in Fig. 2.2a connects two PAs, idealized as voltage sources V_1 and V_2 and represented by the vectors defined in Fig. 2.2b, across a differential load. A critical component of the vector relationship is the outphasing angle, θ, which is the phase symmetrically added and subtracted from the common phase in each branch. The differential phase, φ, is the total phase between the two branches, or twice the outphasing angle. Phase control in simulation is usually done symmetrically (θ), while control in measurement is done asymetrically (φ), though both produce equivalent load modulation and results. Simple outphasing is the term used in [64] to describe non-isolated outphasing without reactive compensation. Note that the source V_2 is shown in negative form, because the load is differential and combines via subtraction. The voltage sources are defined in phasor form as:

$$V_1 = A_0(\sin\theta + j\cos\theta) \tag{2.1}$$

$$V_2 = A_0(-\sin\theta + j\cos\theta) \tag{2.2}$$

where A_0 is the amplitude of the voltage sources. The load voltage and current is:

$$V_L = V_1 - V_2 = 2A_0\sin\theta \tag{2.3}$$

$$i_L = \frac{V_L}{R_L} = \frac{2A_0\sin\theta}{R_L} \tag{2.4}$$

Now the impedances loading each voltage source (internal PA) can be found:

$$Z_1 = \frac{V_1}{i_L} = \frac{R_L}{2}(1 + j\cot\theta) \tag{2.5}$$

$$Z_2 = \frac{V_2}{-i_L} = \frac{R_L}{2}(1 - j\cot\theta) \tag{2.6}$$

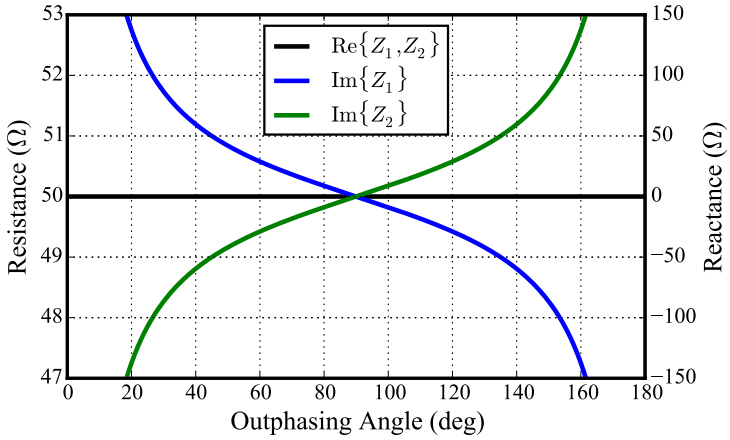


Figure 2.3: Load modulation for simple outphasing operation with R_L set to 100 Ω.

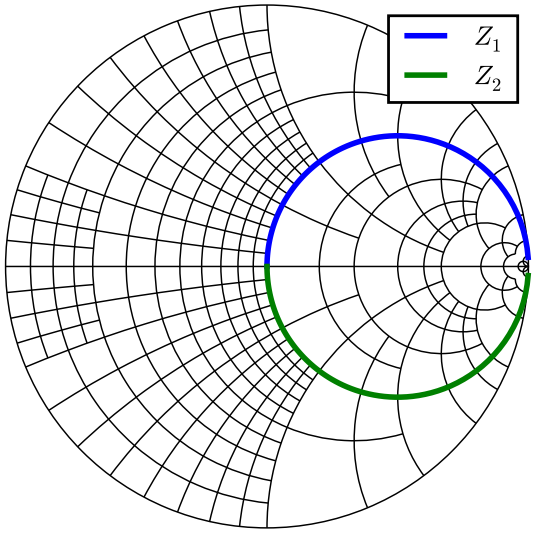


Figure 2.4: Load modulation for simple outphasing operation with R_L set to 100 Ω, demonstrating conjugate reactive loading. Smith chart normalized to 50 Ω.

In Fig. 2.3, the load modulation exhibits a constant real part, but a significant variation in the reactive part with swept outphasing angle. At 90°, a peak output power and efficiency are obtained as the load voltage is maximized and the load impedances are purely real. As θ approaches 0° or 180°, the load impedances become highly reactive an approach an infinite magnitude, minimizing the power generated by the voltage source and delivered to the load. Fig. 2.4 displays the load modulation on a 50 Ω Smith chart. For $0° < \theta < 90°$, Z_1 has a series inductance and Z_2 has a series capacitance. Notice that the load impedances of the voltage

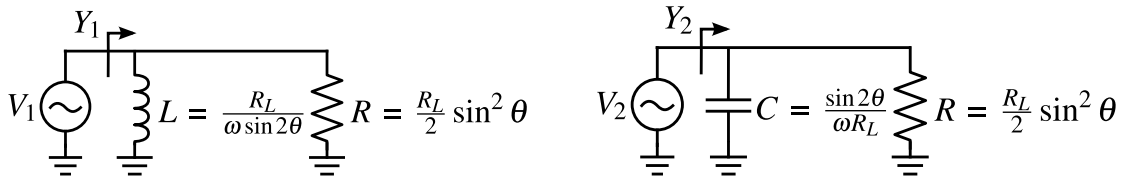


Figure 2.5: Equivalent shunt circuits demonstrating load modulation presented to (a) V_1, with an inductive shunt susceptance, and (b) V_2, with a capacitive shunt susceptance.

sources are conjugates. If the outphasing angle was swept from 90° to 180°, the load impedances seen by each voltage source would swap, therefore sweeping from 0° to 180°completes an entire load modulation circle for each voltage source. This will be more important when compensation is introduced.

The load modulation can be equivalently described in terms of the admittance, which is helpful for describing reactive compensation. Taking the inverse of Z_1 and Z_2 yields the load admittances:

$$Y_1 = \frac{i_L}{V_1} = \frac{2\sin^2\theta}{R_L}(1 - j\cot\theta) \tag{2.7}$$

$$Y_2 = \frac{i_L}{V_2} = \frac{2\sin^2\theta}{R_L}(1 + j\cot\theta) \tag{2.8}$$

which can be separated into real and imaginary parts to find the shunt susceptances and conductances:

$$Y_1 = G + jB_1 = \frac{2\sin^2\theta}{R_L} - j\frac{\sin 2\theta}{R_L} \tag{2.9}$$

$$Y_2 = G + jB_2 = \frac{2\sin^2\theta}{R_L} + j\frac{\sin 2\theta}{R_L} \tag{2.10}$$

Equivalent half-circuits are shown in Fig. 2.5, where both voltage sources are loaded with an outphasing angle dependent conductance. The load admittances are conjugate, where Y_1 is inductively loaded and Y_2 is capacitively loaded. In Fig. 2.6 the real and imaginary parts of Y_1 and Y_2 are plotted. The load admittances become purely real at 90°, corresponding to maximum output power. At 0° and 180°, the load admittances are purely real, but zero, corresponding to an infinite impedance and minimum output power.

The input power is the power generated by the voltage sources, which can be calculated as:

$$P_{in_1} = |V_1|^2|Y_1| = \frac{2A_0^2\sin\theta}{R_L} \tag{2.11}$$

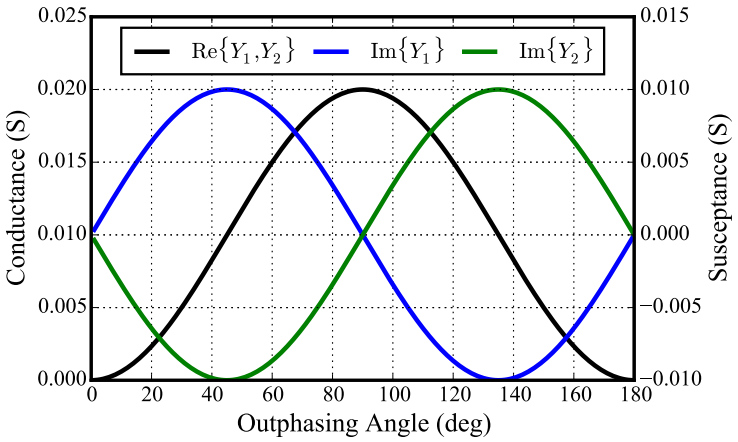


Figure 2.6: Load modulation in terms of admittance for simple outphasing operation with R_L set to 100 Ω.

similarly,

$$P_{in_2} = |V_2|^2 |Y_2| = \frac{2A_0^2 \sin\theta}{R_L} \tag{2.12}$$

Thus, the total input power is:

$$P_{in} = P_{in_1} + P_{in_2} = \frac{4A_0^2 \sin\theta}{R_L} \tag{2.13}$$

The total output power can be calculated as:

$$P_{out} = \frac{|V_1|^2}{R} + \frac{|V_2|^2}{R} = \frac{4A_0^2 \sin^2\theta}{R_L} \tag{2.14}$$

The efficiency is the ratio of the output power to the input power:

$$\eta = \frac{P_{out}}{P_{in}} = \sin\theta \tag{2.15}$$

Fig. 2.7 shows the variation of input and output power with outphasing angle. The voltage source amplitude is set to normalize the peak output power to 1 W. Fig. 2.8a demonstrates the efficiency of simple outphasing with respect to outphasing angle. Fig. 2.8b shows the degradation of the efficiency at back-off. Simple outphasing with class-B internal PAs has the same efficiency roll-off as a single ended class-B PA.

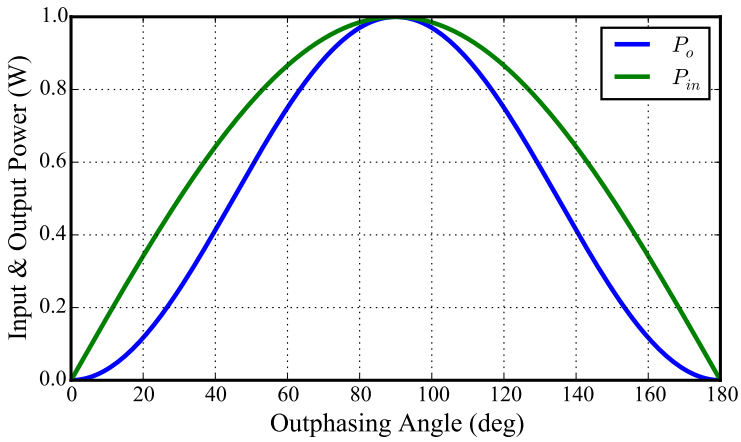
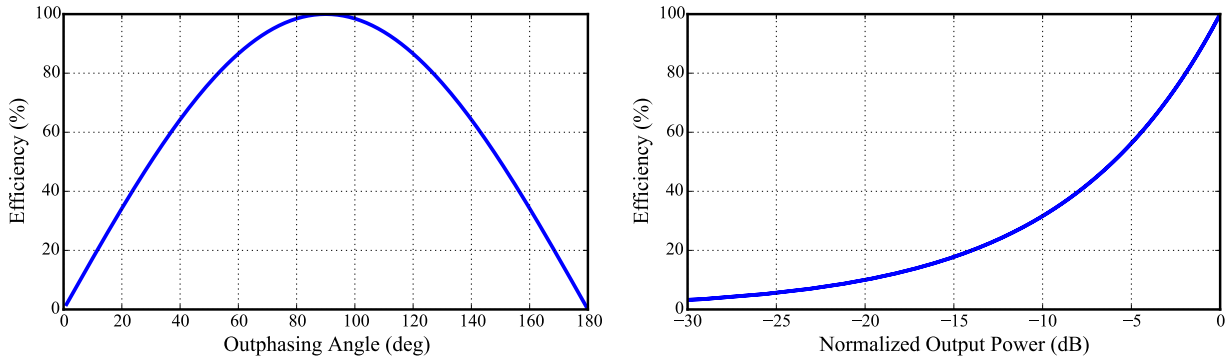


Figure 2.7: Input and output power as a function of outphasing angle, demonstrating the system effect of load modulation in simple outphasing.



(a) (b)

Figure 2.8: Efficiency of simple outphasing as a function of (a) outphasing angle, and (b) normalized output power.

Theoretically, simple outphasing does not provide any efficiency benefit, which is why Chireix proposed reactive compensation in the combiner. The additional elements are shown in the equivalent half-circuits in Fig. 2.9. The compensation susceptance, B_C, can be solved to cancel the reactive loading at a single outphasing angle and corresponding output power level, making the load purely real and peaking the efficiency. This topology has been named the Chireix combiner, and can be implemented with transmission lines, lumped element approximations, or tunable elements such as capacitances [57], MEMs [55], and diodes [52].

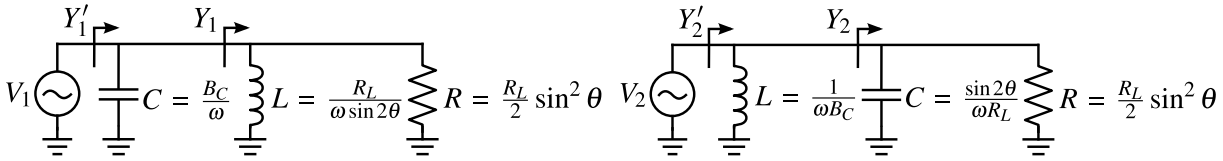


Figure 2.9: Equivalent shunt circuits with (a) capacitive and (b) inductive compensation, canceling the reactive part of the load at a single output power in addition to peak output power.

Examining the reactively compensated half-circuits, new expressions for the load admittances are found:

$$Y_1' = G + j(B_1 + B_C) = \frac{2\sin^2\theta}{R_L}\left[1 - j\frac{1}{2}\left(\frac{\sin 2\theta - R_L B_C}{\sin^2\theta}\right)\right] \tag{2.16}$$

$$Y_2' = G + j(B_2 + B_C) = \frac{2\sin^2\theta}{R_L}\left[1 + j\frac{1}{2}\left(\frac{\sin 2\theta - R_L B_C}{\sin^2\theta}\right)\right] \tag{2.17}$$

The input power can be recalculated:

$$P_{in_1} = |V_1|^2|Y_1'| = \frac{2A_0^2\sin^2\theta}{R_L}\sqrt{1 + \frac{1}{4}\left(\frac{\sin 2\theta - R_L B_C}{\sin^2\theta}\right)^2} \tag{2.18}$$

$$P_{in_2} = |V_2|^2|Y_2'| = \frac{2A_0^2\sin^2\theta}{R_L}\sqrt{1 + \frac{1}{4}\left(\frac{\sin 2\theta - R_L B_C}{\sin^2\theta}\right)^2} \tag{2.19}$$

with the total input power being:

$$P_{in} = P_{in_1} + P_{in_2} = \frac{4A_0^2\sin^2\theta}{R_L}\sqrt{1 + \frac{1}{4}\left(\frac{\sin 2\theta - R_L B_C}{\sin^2\theta}\right)^2} \tag{2.20}$$

Since the load resistance remains unchanged, the output power stays the same, and the efficiency becomes:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{1}{\sqrt{1 + \frac{1}{4}\left(\frac{\sin 2\theta - R_L B_C}{\sin^2\theta}\right)^2}} \tag{2.21}$$

Notice that the efficiency is maximum when the second part of the denominator is zero:

$$\sin 2\theta - R_L B_C = 0 \tag{2.22}$$

Solving for the outphasing angle gives the value of $R_L B_C$ corresponding to a second purely real load and thus a second peak in efficiency:

$$\theta = \frac{1}{2}\arcsin\left(R_L B_C\right) \tag{2.23}$$

To understand the choice of outphasing angle to reactively compensate, the relationship between outphasing angle and normalized output power must be defined. The output power is normalized to 1 W at $\theta = 90°$, yielding the following relationship between the voltage source amplitude and load resistance:

$$R_L = 4A_0^2 \tag{2.24}$$

Substituting (2.24) into (2.14) yields:

$$P_{out} = \sin^2\theta \tag{2.25}$$

Taking the power logarithm of both sides yields the normalized output power with respect to the outphasing angle:

$$P_{out,n} = 20\log(\sin\theta) \tag{2.26}$$

which can be written in terms of the normalized output power:

$$\theta = \arcsin\left(10^{P_{out,n}/20}\right) \tag{2.27}$$

The designer can optimize average efficiency for a high PAR signal by choosing the compensated normalized output power to be the PAR of the input signal. Then, the corresponding outphasing angle could be found from (2.27), and the compensation susceptance from (2.23), which can be rewritten as:

$$B_C = \frac{\sin 2\theta}{R_L} \tag{2.28}$$

Fig. 2.10 shows the admittance variation when compensation is incorporated at 9 dB back-off (P_{out} = -9 dB). Notice the asymmetry about 90°, and the decreased magnitude of the susceptance for $\theta < 90°$. These observations can be explained by the load modulation visualized on a 50Ω Smith chart in Fig. 2.11. The compensated load modulation is shown in green as compared to the uncompensated case in blue, with the dashed and solid lines designating the loading on V_1 and V_2, respectively. Reactive compensation moves the load modulation closer to the real axis, which has also moved the first intersection (purely real load, and efficiency peak) slightly away from peak power. As the compensation is increased, the two real loads move closer to each other until the load modulation circles are tangential to each other on the real axis when $R_L B_C$ reaches 1.0. As stated previously, sweeping the outphasing angle up to 180° completes a full circle of

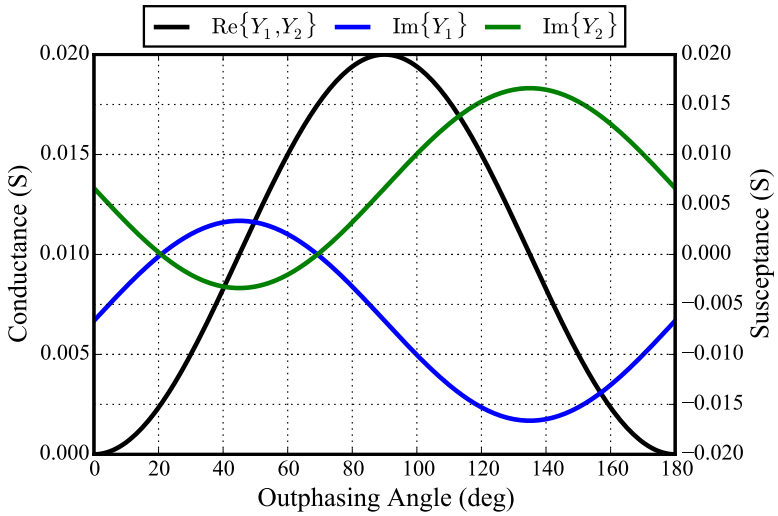


Figure 2.10: Compensated load modulation under outphasing operation with R_L set to 100 Ω for $R_L B_C$ = 0.66.

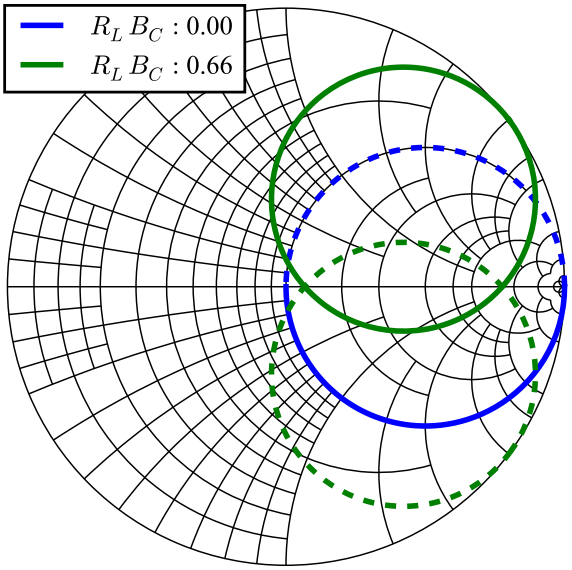


Figure 2.11: Load modulation comparison with R_L set to 100 Ω for $R_L B_C = 0, 0.66$. Dashed and solid lines are the loading presented to V_1 and V_2 respectively. Smith chart normalized to 50 Ω.

load modulation. In the uncompensated case, the two circles overlap, so the power, efficiency and loading are symmetric. When compensation is utilized, two distinct paths from peak power near the center of the Smith chart to minimum power at the edge are realized: the inner trajectory along the real axis, and the outer trajectory. The difference in the loading conditions along these trajectories corresponds to the asymmetry in Fig. 2.10.

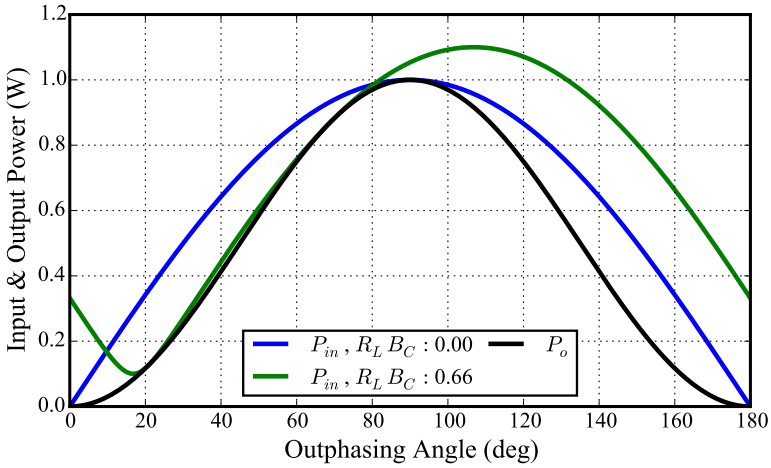
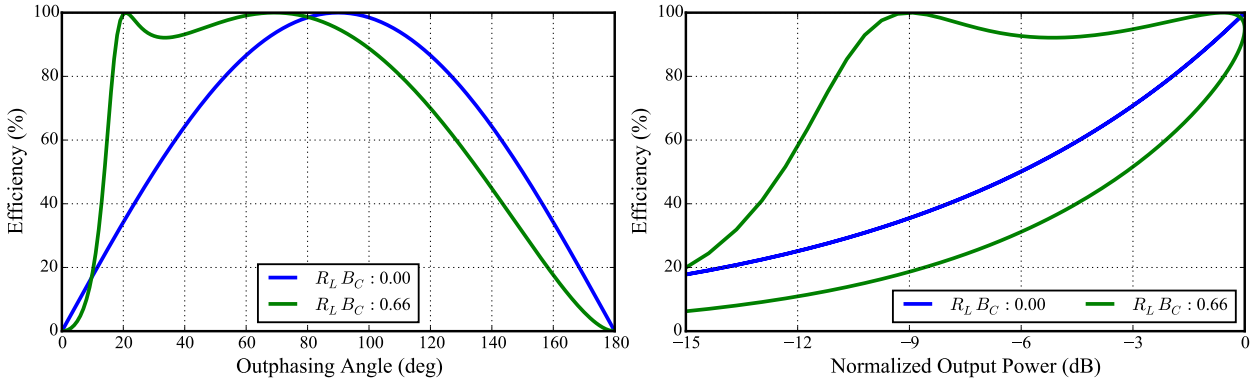


Figure 2.12: Input and output power as a function of outphasing angle for $R_L B_C = 0$ and 0.66. Asymmetry has been introduced to the input power of the compensated circuit due to its loading conditions, moving it closer to the output power, and therefore improving efficiency.



(a) (b)

Figure 2.13: Efficiency as a function of (a) outphasing angle, and (b) normalized output power for $R_L B_C = 0$ and 0.66, demonstrating significant improvement with compensation.

The asymmetric loading conditions induce asymmetry in the input power, shown in Fig. 2.12, moving it closer to the unchanged output power, thus improving efficiency, as shown in Fig. 2.13. The efficiency remains high for a large range of outphasing angles, corresponding to 9 dB of output power range. The efficiency has the appearance of hysteresis when plotted against normalized output power due to the difference in efficiency between the two outphasing trajectories or load modulation paths. Of course, the worse trajectory need not be used at all. The efficiency enhancement in outphasing is dependent upon Chireix's proposed reactive compensation and offers improvements on par with Doherty and envelope tracking architectures.

By assuming the internal PAs to operate as voltage sources, the presented theory equates the system efficiency with the power factor of the combiner. This assumption holds for linear branch amplifiers, like the class-B [64], but not for switch-mode PAs that achieve higher efficiencies, such as class-E [48]. In that case, the system efficiency is a function of both the internal PA and the combiner. The system drain efficiency can be defined as the ratio of the total RF power at the fundamental to the total DC power drawn by the sources:

$$\eta_d = \frac{\sum_{n=1}^{N} P_{rf_n}}{\sum_{n=1}^{N} P_{DC_n}} \tag{2.29}$$

where the total powers are summed up to N sources, or the number of internal PAs. Most often N is two, but it may be higher, as in four-way outphasing [59, 67]. The RF and DC powers contributed and consumed by the n^{th} source can be calculated by:

$$P_{rf_n} = \frac{1}{2}\,\mathrm{Re}\{v_n i_n^*\} = \frac{1}{2}|v_n|^2\mathrm{Re}\{Y_n\} \tag{2.30}$$

$$P_{DC_n} = V_{DC_n} I_{DC_n} = \left(\frac{V_{DC_n}}{|v_n|}\frac{I_{DC_n}}{|i_n|}\right)|v_n|^2|Y_n| \tag{2.31}$$

since $|i_n| = |v_n||Y_n|$. Assuming identical sources, substituting (2.30) and (2.31) into (2.29) yields:

$$\eta_d = \eta_s \mathrm{PF}_N \tag{2.32}$$

$$\eta_s = \frac{1}{2}\frac{|v_n|}{V_{DC_n}}\frac{|i_n|}{I_{DC_n}} \tag{2.33}$$

$$\mathrm{PF}_N = \frac{\sum_{n=1}^{N}\mathrm{Re}\{Y_n\}}{\sum_{n=1}^{N}|Y_n|} \tag{2.34}$$

Now the system drain efficiency is the multiplication of the apparent efficiency of the source, η_s, and the power factor of the load, PF_N. The apparent efficiency does not consider any phase difference between the load voltage and current, and therefore could be greater than unity. In any case, this additional theory shows that the system efficiency must consider the efficiency of both the internal PA and combiner.

2.2 High Efficiency GaN MMIC PA Design

A monolithic microwave integrated circuit (MMIC) is an active or passive microwave circuit formed in situ on a semiconductor substrate by a combination of deposition techniques including diffusion, evaporation,

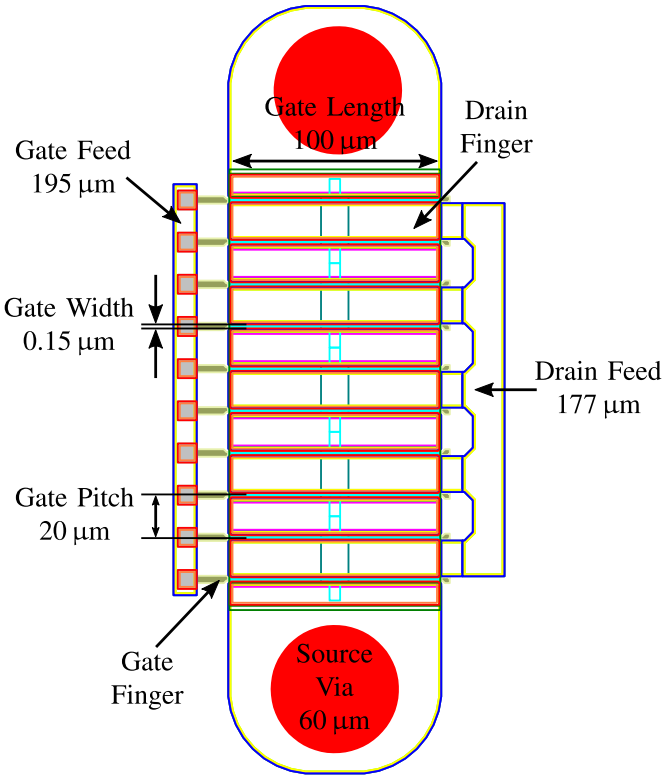


Figure 2.14: Layout of a pHEMT from Qorvo's 0.15 µm GaN process.

epitaxy, implantation and other means [68]. After failed attempts to develop MMICs using semi-insulating silicon substrates, research on the three-five compound gallium arsenide (GaAs) showed it to be a good insulator and able to function as a base material. The first GaAs MMIC was an X-band amplifier [69]. Although GaAs is still the most widely used substrate, a new three-five compound gallium nitride (GaN) has emerged recently. GaN is a wide-bandgap semiconductor, which means the transistors fabricated on such substrates can operate at a higher voltage, frequency, and temperature. Increased output impedance is enabled by high voltage operation, resulting in a lower impedance transformation ratio in the matching network, not only decreasing loss but improving bandwidth capabilities. Additionally, GaN transistors have large current densities, which improves the power density beyond other semiconductors. Although research and development of GaN started in the late 1990s, a handful of foundries have commercially released processes today [70].

The crux of a semiconductor process is the transistor. An example layout is shown in Fig. 2.14, where the gate, drain, and source fingers are all interlaced. The source is grounded by end-vias, while the gate and

drain fingers are combined by a feed or bus. The gate width largely determines the maximum frequency of operation and is typically used to distinguish process technologies. The gate periphery is the total size of the transistor (ignoring the gate width), found by multiplying the number of fingers by the gate length. Often, a process technology will define the expected power as a function of gate periphery, in mm. For example, GaN processes can produce 5-7 W/mm of power density. If a transistor has 10 fingers which are 100 µm long, the total gate periphery is 1 mm, and the expected output power would be 5-7 W. A tradeoff between number of fingers and gate length exists for a desired output power. Shorter gate fingers will have more gain, but require a larger number to achieve the same output power. Too many fingers can cause heating issues in the center of the device, especially if the vias are on the end.

2.2.1 Qorvo 0.15 µm GaN Process

All MMICs presented in this thesis are fabricated in a 0.15 µm gate length process with an AlGaN/GaN epitaxial layer on 100 µm SiC on 100 mm diameter wafers. Typical DC characteristics of these pseudomorphic high electron mobility transistors (pHEMTs) are I_{max}=1.15 A/mm, transconductance $g_{m,max}$=380 mS/mm, and 3.5 V pinch-off at V_{ds}=10 V. Device breakdown voltage exceeds 50 V at I_{gd}=1 mA/mm. Non-linear device models were extracted for 4×75 µm, 8×75 µm, and 10×90 µm devices (number of gate fingers by gate width) at 10 GHz. To support supply modulation applications, the models were fit to S-parameter and load-pull data measured at low drain current over a wide range of drain bias voltages. Load-pull results for a PAE of 62% at 10 GHz and 20 V drain bias demonstrated 3.4 W/mm output power density with associated gain of 14 dB [35]. The models are de-embedded to the fingers, and do not include the source vias, gate feed, or drain feed, which must be accounted for in simulation. They are delivered as "black box" models, meaning the internal ports (intrinsic drain) and parameters are inaccessible.

In this 3 Metal Interconnect (3MI) process [71], any combination metal layers can be utilized to form microstrip lines of varying RF losses and DC current handling capabilities. For example, type 7 lines utilize all three metal layers (M0, M1, and M2) to handle a maximum DC current density of 16.0 mA/µm while type 9 lines utilized only M1 and M2 to handle a maximum DC current density of 14.4 mA/µm. Nitride and MIM layers provide insulation between the metal layers and are used for creating capacitors with densities

of 240 pF/mm^2, 300 pF/mm^2, and 1200 pF/mm^2, all of which have different voltage handling capabilities.

2.2.2 MMIC Design

Circuit design forms the foundation for all MMICs, which is simply a realization of a circuit concept. Resources have been published concerning MMIC design, giving many examples [72, 73] and a detailed design methodology for multi-stage, power combined PAs [74]. This section will *concisely* describe a simple, high efficiency, single-stage MMIC PA design.

The device size is selected to meet design specifications, which are maximum efficiency at 10 GHz with more than 1 W output power. Specification sheets or load-pull characterization in simulation or measurement should be used to inform this decision in other cases. Since our nonlinear models are scalable to an extent, the largest transistor size with model integrity is chosen. Scaling the number of fingers has a higher risk for inaccuracy than scaling the gate width, so the 10×90 µm device model is scaled up to 10×100 µm. The choice of bias conditions (gate and drain) are dependent upon the design goals and desired class of operation. The supply voltage (drain) must be chosen such that the output voltage swing does not exceed the breakdown voltage of the transistor, while the bias voltage (gate) will dictate key operational characteristics. For this design, the device is biased at pinch-off (V_G = -4.0 V, I_{DQ}=5 mA) with a supply voltage of 20 V. In general, source- and load-pull simulations can be performed over varying bias conditions, input power, and frequencies. This characterization provides the impedances that should be presented to the device by the matching networks in order to obtain the desired performance.

2.2.2a Gate Bias Tee

Once the device has been properly characterized, the bias tees are designed. This part of the matching network is of utmost importance, since it provides the low frequency (baseband) termination of the transistor, which significantly affects linearity [75, 76] and more importantly, stability [12]. The bias tee may be utilized as a matching element, or have no effect on RF matching, which would be referred to as an RF choke. In either case, the bias tee must provide a low-loss DC path to the device, while properly terminating the baseband impedance for stability.

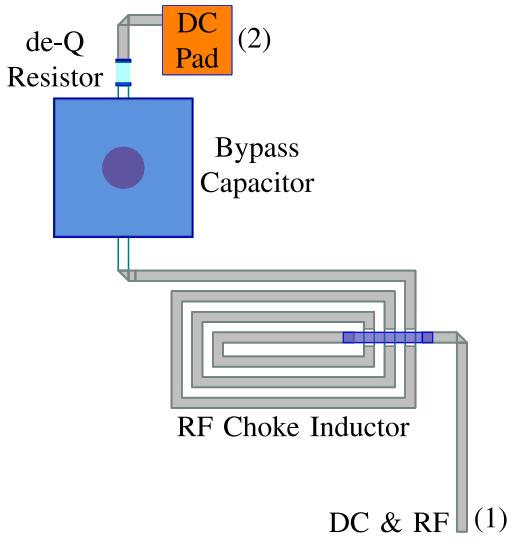


Figure 2.15: Layout of gate bias tee.

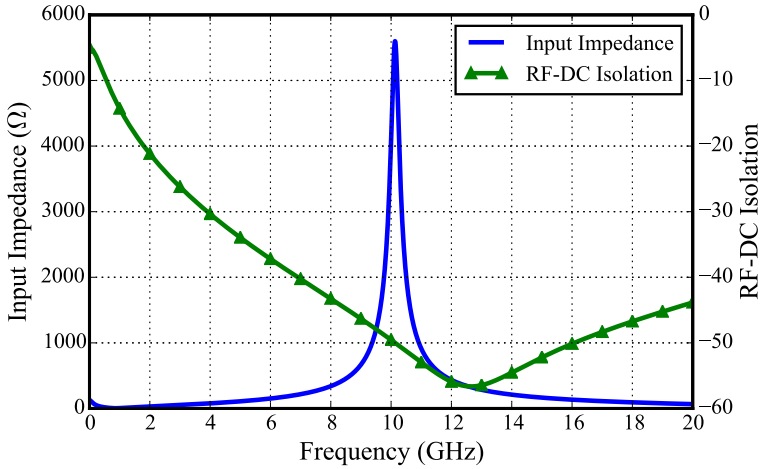


Figure 2.16: Simulation of gate bias tee, demonstrating high input impedance and isolation.

In this design, the gate bias tee functions as an RF choke, presenting a high impedance to the matching network at the fundamental frequency so as to reduce its effect on matching. The layout is shown in Fig. 2.15, with the corresponding simulation in Fig. 2.16. The bias tee is simulated as a two-port network, where port 1 is connected to the RF path, and does not include the DC blocking capacitor. Note that the simulation should include off-chip components, such as bond wires, bypass capacitors, and inductance in the long cable connected to the power supply. Because the DC bond wire connects two shunt capacitors, possibly forming a resonant circuit, a resistor is placed between the on-chip capacitor and bonding pad. It is called a de-Q resistor because it reduces the quality factor of any resonance formed by the bond wire and capacitors.

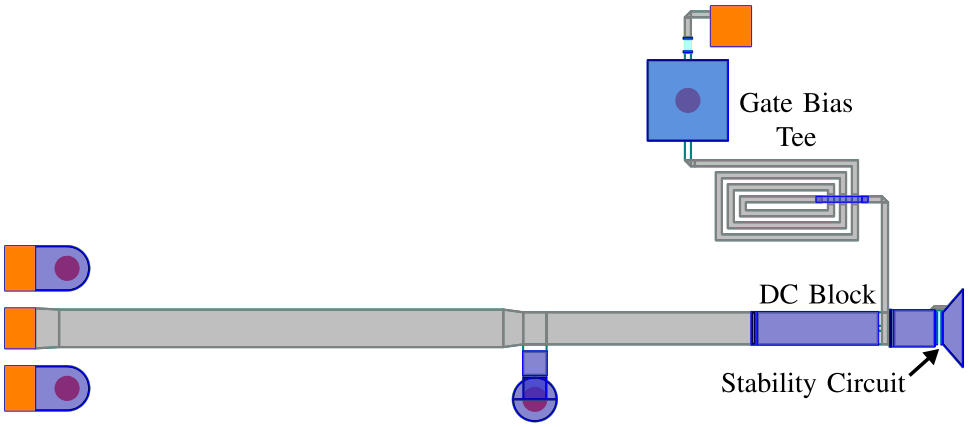


Figure 2.17: Layout of input matching network.

The bypass capacitor is implemented as a capacitor-over-via (COV), meaning its bottom layer is directly connected to a via. It's size is sufficiently large to provide a very low impedance at baseband frequencies above DC, which dictates the RF-DC isolation (S_{21} simulation). The inductor transforms the short circuit of the COV into a high impedance at RF, approximately 5 kΩ.

2.2.2B Input Matching Network

The input matching network (IMN) must transform the 50 Ω generator impedance into that desired by the transistor, as found in the source-pull characterization. An accurate simulation of matching networks should include the RF probe pad as well as expected RF bond wires. The layout in Fig. 2.17 demonstrates a narrowband matching network, with a simple shunt capacitor and series transmission line topology. The long line extending from the RF pad to the shunt capacitor does not perform any matching, and is only necessary to reach the chip edge, since the chip size was much larger than needed for this design. The DC blocking capacitor is integrated into the transmission line by feeding the element on the bottom metal layer (M0) and connecting only the top metal layer (M2) to the bias tee junction.

In addition to baseband impedance termination, RF loading conditions can cause instability in most transistors. Stability circles can be generated to describe regions of the Smith chart where the device will oscillate [77]. These circles can be manipulated at the gate of the transistor, and kept from overlapping with the passive Smith chart with enough series resistance, ensuring stability (unconditional) for any passive

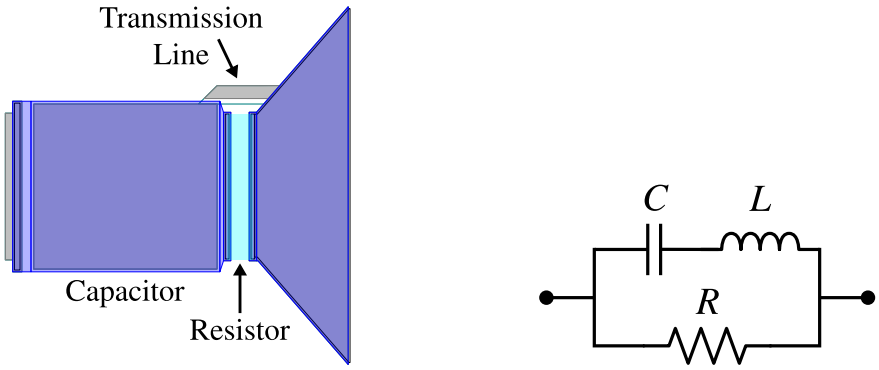


Figure 2.18: (a) Layout and (b) equivalent circuit for stability circuit at the input of the transistor.

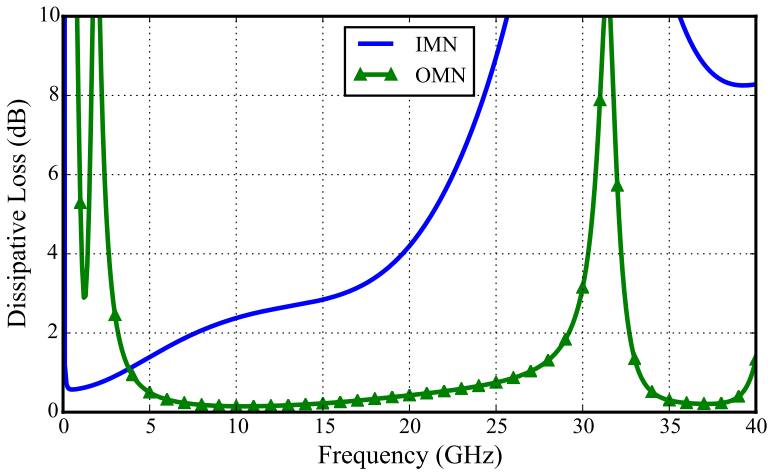


Figure 2.19: Simulated dissipative loss in the input and output matching networks.

load. Of course, a series resistance will incur loss at the fundamental, so other combinations of resistors, capacitors, and inductors can be utilized to stabilize the transistor without affect RF performance. One implementation is shown in Fig. 2.18. In this circuit, the inductance formed by the transmission line and the capacitance are chosen to resonate at the fundamental frequency, providing a low-loss path, while all other frequencies are forced through an additional resistance.

The losses in the input and output matching network are shown in Fig. 2.19, where the dissipative loss is defined as:

$$\text{Dissipative Loss (dB)} = -10\log\left(\frac{|S_{21}|^2}{1-|S_{11}|^2}\right) \tag{2.35}$$

which defines the losses related to dissipation or radiation in the network, and excluding mismatch at the

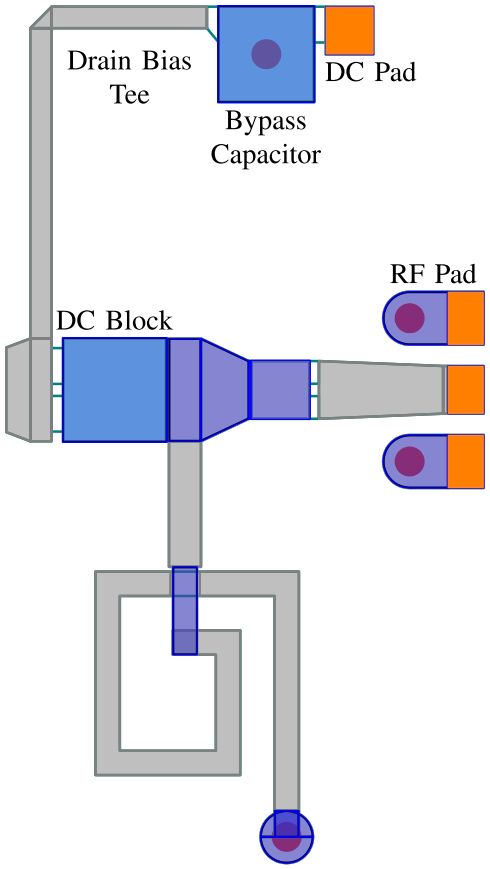
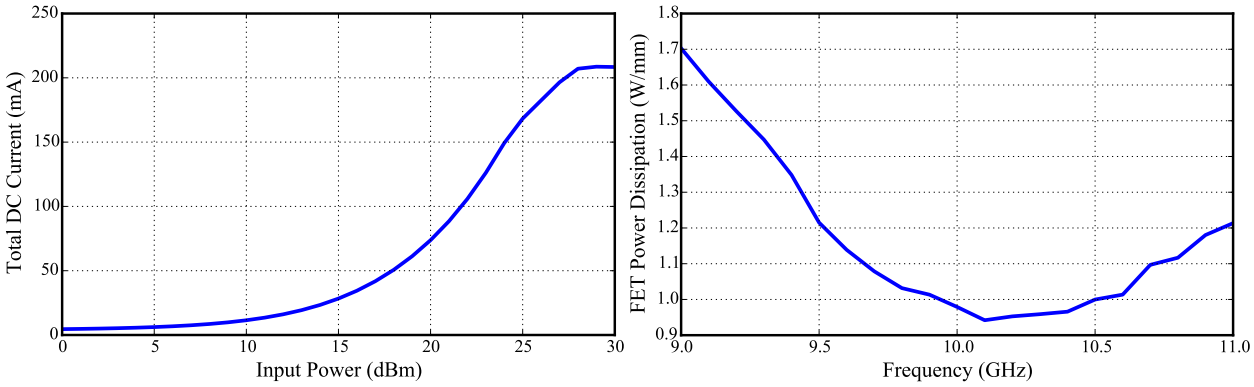


Figure 2.20: Layout of output matching network.

input [78]. Essentially it is the ratio of the power delivered to the load to the power transferred into the network. The input matching network incurs a loss of 2.38 dB. Though this seems high, it affects the efficiency much less than loss at the output and helps to stabilize the transistor.

2.2.2c Output Matching Network

The output matching network (OMN) is designed for the fundamental frequency only, without any intentional harmonic termination. However, during the optimization for efficiency, a high third harmonic impedance is realized, contributing to the high efficiency achieved in this design. The OMN layout is shown in Fig. 2.20. In this case, the bias tee is utilized as a shunt matching stub, which is effectively terminated in a short circuit by the bypass capacitor. The drain bias tee utilizes a 45 µm wide, type 9 transmission line to carry a maximum of 648 mA of DC current. For an estimated output power of 4 W and a minimum expected efficiency of 50%, the transistor would only draw 400 mA. Notice that the air bridges to the bypass capacitor



(a) (b)

Figure 2.21: (a) Simulated total DC current drawn by the PA at 10 GHz. (b) Simulated power dissipated in the transistor under saturation.

are made wider due to their limited current handling capability. As implemented for the IMN, the DC block is integrated into the series transmission line, and the RF pad and bond wire are considered in simulation. For the OMN, port 1 is at the transistor and port 2 is at the output. Therefore, S_{12} and S_{22} replace S_{21} and S_{11}, respectively, in (2.35). The entire OMN incurs a dissipative loss of only 0.15 dB.

2.2.2D Final Simulations

The PA can now be formed by the designed IMN and OMN, and adjusted slightly for efficiency. Fig. 2.21a shows the total (gate and drain) DC current drawn at 10 GHz for swept input power. It is important to be aware of the saturated current, which is 210 mA in this case, especially for setting supply limits during measurement. For thermal considerations, the power dissipated in the transistor per unit gate periphery is plotted in Fig. 2.21b. According to thermal simulation at Qorvo, a power dissipation of 3.4 W/mm will raise the temperature of fingers internal to an 8x75 µm pHEMT cell to 160° C. Therefore, this design should be safe from thermal issues, since transistor power dissipation remains below 1.7 W/mm across the operating frequency range.

The output power, efficiency, and gain are characterized over swept input power in Fig. 2.22a and swept frequency in Fig. 2.22b. A peak power-added efficiency (PAE) of 63% is achieved with an output power of 34.7 dBm at an input power of 27 dBm at 10 GHz. The saturated gain is 7.7 dB. The peak PAE remains

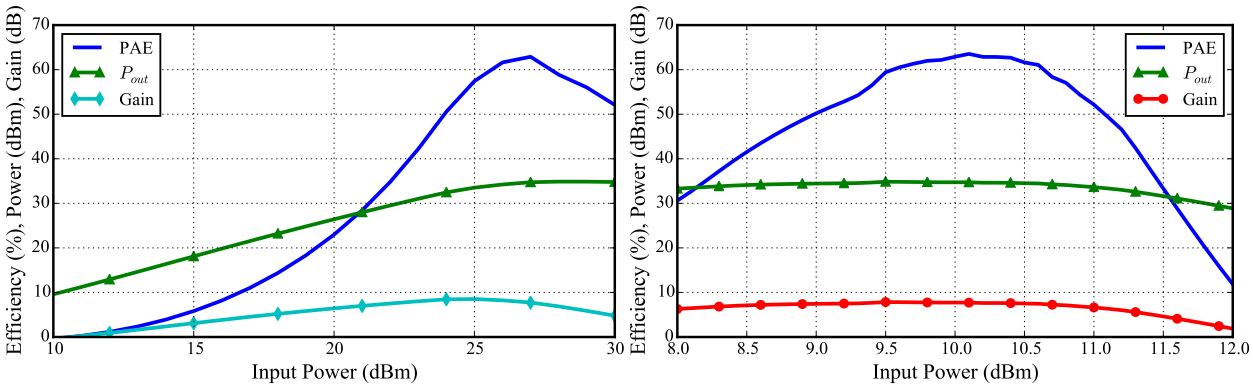


Figure 2.22: Simulated output power, efficiency, and gain (a) at 10 GHz, and (b) across frequency under saturation.

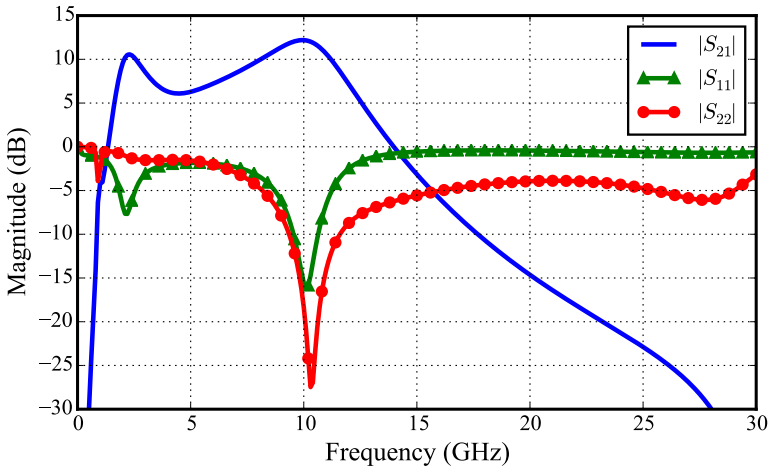


Figure 2.23: Simulated power amplifier S-parameters across frequency.

above 50% for 2 GHz of bandwidth. The S-parameters of the amplifier, simulated over a broad bandwidth are shown in Fig. 2.23. A small-signal gain of 12.2 dB is achieved at 10 GHz, with an input return loss of 15.6 dB and an output return loss of 18.4 dB. It is important to view the S-parameters over a large frequency range to check for indications of instability, such as $|S_{11}|$ or $|S_{22}|$ greater than zero. In this design, a slight match and gain peak around 2.5 GHz occurs, but does not indicate any stability issue according the Rollet factor, k, used to analyze stability for this single-stage amplifier [77].

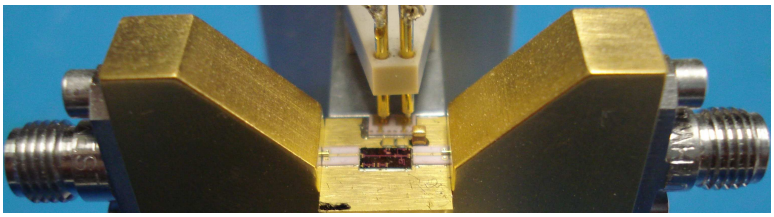


Figure 2.24: Photograph of fixtured MMIC PA.

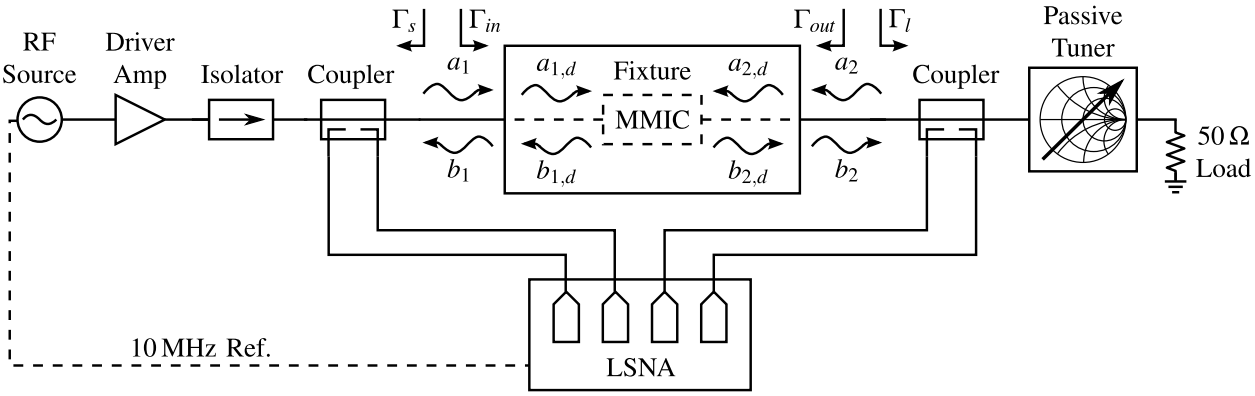


Figure 2.25: Load-pull measurement setup utilizing a LSNA and single frequency mechanical tuner.

2.2.3 Measurement Setup and Calibration

As discussed at the end of the theory in Section 2.1, the system efficiency is dictated by both the internal PAs and combiner. In order to inform the design of the combiner, the internal PA must be characterized by load-pull, which is done over several supply voltages in preparation for the inclusion of discrete supply modulation. Prior to measurement, the MMICs are mounted on 40 mil thick CuMo carrier plates. The RF input and output bond pads are connected to 10 mil thick alumina de-embedding lines with two short bond wires. The DC pads are bonded to off-chip capacitors and pads on which spring loaded DC connectors are landed. The carrier assembly is inserted into an aluminum test fixture. The opposite ends of the alumina de-embedding lines are contacted with connectorized launchers. A photograph is shown in Fig. 2.24.

The load-pull measurement setup, shown in Fig. 2.25, is based on a large-signal network analyzer (LSNA) [79], which has four time-domain receivers to make this two-port measurement. Bi-directional couplers are utilized to acquire absolute incident and reflected waves at the calibrated reference planes which are at the coaxial launchers of the MMIC fixture as the passive tuner varies the load impedance. In

post-processing, the measurements are de-embedded to the MMIC bond wire using the test-fixture error terms extracted from a TRL calibration measurement. Calibration combines a relative SOLT method with an absolute power calibration using a power meter [80], and an absolute phase calibration performed during the reverse "Thru" measurement as explained in [81], yielding an eight-term error matrix:

$$\begin{pmatrix} v_1 \\ i_1 \\ v_2 \\ i_2 \end{pmatrix} = \begin{bmatrix} \alpha_1 & \beta_1 & 0 & 0 \\ \gamma_1 & \delta_1 & 0 & 0 \\ 0 & 0 & \alpha_2 & \beta_2 \\ 0 & 0 & \gamma_2 & \delta_2 \end{bmatrix} . \begin{pmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{pmatrix} \tag{2.36}$$

where r_i is the raw-data acquired on the ADCs, and v_i and i_i are the RF voltages and currents respectively. PA performance can be directly calculated from the calibrated voltage and current measurements. The RF powers at the input and output of the DUT, in watts, are:

$$P_{in} = \frac{1}{2}\,\mathrm{Re}\{v_1 i_1^*\} \tag{2.37}$$

$$P_{out} = -\frac{1}{2}\,\mathrm{Re}\{v_2 i_2^*\} \tag{2.38}$$

which include the fundamental and harmonic powers. The negative sign corresponds to the direction of power flow. The DC powers at the input (port 1) and output (port 2) of the DUT, in watts, are:

$$P_{DC_1} = v_1 i_1 \tag{2.39}$$

$$P_{DC_2} = v_2 i_2 \tag{2.40}$$

Now, the gain and efficiency can be calculated. To obtain the reflection coefficients being presented to and by the DUT, the absolute power waves must be calculated from the calibrated RF voltage and current waves:

$$a_1 = \frac{1}{2}(v_1 + Z_0 i_1) \tag{2.41}$$

$$b_1 = \frac{1}{2}(v_1 - Z_0 i_1) \tag{2.42}$$

$$a_2 = \frac{1}{2}(v_2 + Z_0 i_2) \tag{2.43}$$

$$b_2 = \frac{1}{2}(v_2 - Z_0 i_2) \tag{2.44}$$

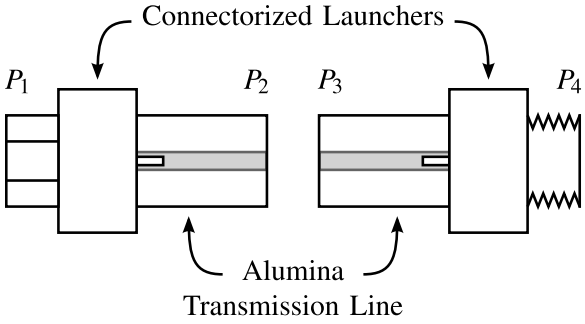


Figure 2.26: Test fixture with connectorized launchers landing on alumina transmission lines which are bonded to the MMIC, placed in between ports 2 and 3. Two-port S-parameters of each side of the fixture are measured using the TRL calibration method, which designates these two networks as the error boxes for calibration.

where the characteristic impedance, Z_0, is calibrated to $50\,\Omega$. These waves are initially found at the coaxial calibrated reference plane, as shown in Fig. 2.25. The reflection coefficients at the input, Γ_{in}, and output, Γ_{out}, of the DUT can be found by:

$$\Gamma_{in} = \frac{b_1}{a_1} \tag{2.45}$$

$$\Gamma_{out} = \frac{b_2}{a_2} \tag{2.46}$$

The reflection coefficients being presented to the input, Γ_s, and output, Γ_l, of the DUT are found by:

$$\Gamma_s = \frac{a_1}{b_1} \tag{2.47}$$

$$\Gamma_l = \frac{a_2}{b_2} \tag{2.48}$$

The TRL calibration method is used to measure the S-parameters, $[S]$, of the test fixture, which is shown schematically in Fig. 2.26. To find the unknown S-parameters of the test fixture each side treated as an error box in calibration language. The TRL method utilizes the measurement of three standards: Thru, Reflect, and Line. A TRL kit containing these three standards has been fabricated and measured. Knowing the S-parameters of the fixture, the absolute power waves can be de-embedded from the coaxial connector to the MMIC bond wire, internal to the test fixture:

$$b_{1,d} = \frac{1}{S_{12}}(b_1 - S_{11}a_1) \tag{2.49}$$

$$a_{1,d} = S_{21}a_1 + S_{22}b_{1,d} \tag{2.50}$$

$$b_{2,d} = \frac{1}{S_{43}}(b_2 - S_{44}a_2) \tag{2.51}$$

$$a_{2,d} = S_{34}a_2 + S_{33}b_{2,d} \tag{2.52}$$

The de-embedded voltages and currents can be calculated from the de-embedded absolute power waves as:

$$v_{1,d} = a_{1,d} + b_{1,d} \tag{2.53}$$

$$i_{1,d} = \frac{1}{Z_0}(a_{1,d} - b_{1,d}) \tag{2.54}$$

$$v_{1,d} = a_{2,d} + b_{2,d} \tag{2.55}$$

$$i_{1,d} = \frac{1}{Z_0}(a_{2,d} - b_{2,d}) \tag{2.56}$$

Now the powers at the input and output of the MMIC, de-embedded to the bond wires, can be calculated from the de-embedded voltages and currents as:

$$P_{in,d} = \frac{1}{2}\,\mathrm{Re}\{v_{1,d}i_{1,d}^*\} \tag{2.57}$$

$$P_{out,d} = -\frac{1}{2}\,\mathrm{Re}\{v_{2,d}i_{2,d}^*\} \tag{2.58}$$

Again, these powers contain the fundamental and harmonic frequencies, enabling the calculation of any performance parameter for the MMIC PA. The load-pull tuner can be set to 50 Ω for a traditional power and frequency swept PA measurement, or it can be swept to synthesize load impedances covering a large portion of the Smith chart. In either case, the calibration must only be performed once.

2.2.4 MMIC Measurements

The fabricated MMIC is 3.8×2.3 mm^2, as shown in Fig. 2.27. As stated previously, it is mounted and measured in a fixture, which is de-embedded in post-processing. The power and frequency swept measurements are shown in Fig. 2.28. A peak PAE of 69.9% is achieved with a drain efficiency of 86.3% at an output power of 34.2 dBm. This optimum occurs for a bias voltage of -4.4 V, corresponding to a quiescent drain current of 0.45 mA, and a supply voltage of 20 V at 10.2 GHz and 27 dBm of input power, yielding a saturated gain of 7.2 dB. To peak the efficiency the transistor is biased in deep pinch-off, which decreases the saturated gain. The PAE remains above 60% for approximately 1 GHz of bandwidth, and above 50% for nearly 2 GHz.

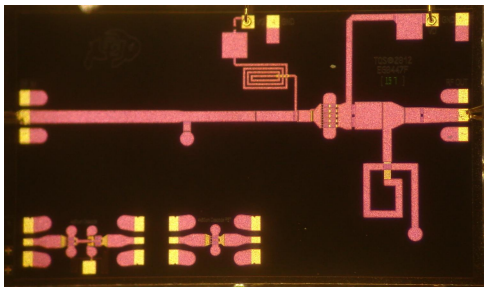
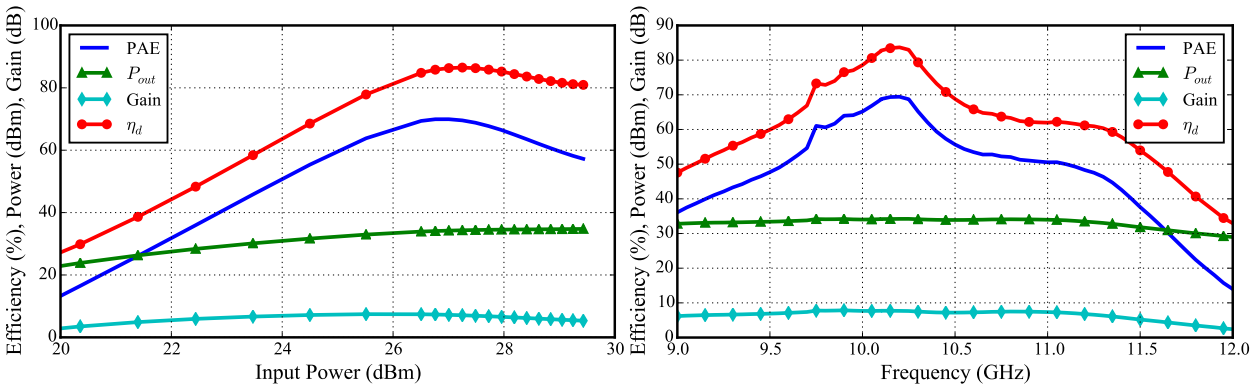
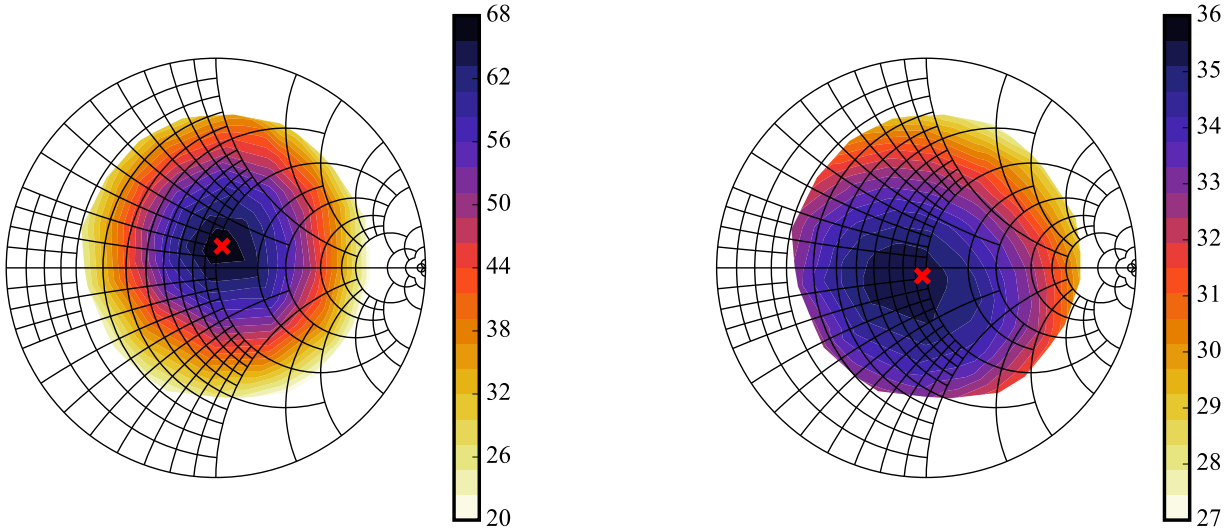


Figure 2.27: Photograph of MMIC PA, which is 3.8×2.3 mm^2. Test devices fill the empty space.



(a) (b)

Figure 2.28: Measured output power, efficiency, and gain (a) at 10.2 GHz, and (b) across frequency under saturation.



(a) (b)

Figure 2.29: Measured load-pull contours for (a) PAE, and (b) output power.

The measured load-pull contours are shown in Fig. 2.29 for PAE and output power at 10.1 GHz. A peak PAE of 68% is measured at a load impedance of $51.9 + j10.8\,\Omega$, while a peak output power of 35.4 dBm is measured at a load impedance of $48 - j3.75\,\Omega$.

2.3 Chireix Combiner Design

The combiner facilitates the vital interaction between the internal PAs, and its design centers on realizing the desired load modulation, which will dictate the system performance for a given internal PA. The load modulation intersections can be chosen specifically for each design application, but in all cases it is important to load the internal PAs for balanced output power. To aid visually in the combiner design, the axis of power symmetry demonstrates a straight trajectory from peak output power toward peak efficiency, over which the internal PA loading should be balanced if the load modulation is symmetric about the axis. Imbalanced loading of the internal PAs causes distortion in the load modulation. Referring to Fig. 2.11, one circle would shrink while the other expands. Not only does this ruin performance, but it could lead to instability as well. Therefore, the reference plane at which the combiner is designed must match that of the internal PA characterization. If the theoretical load modulation referenced to the intrinsic drain is presented at the output of this GaN MMIC, poor performance and instability would ensue. Again, this is because the theoretical load modulation is referenced to the intrinsic drain of a device, not the output of a PA.

In order to measure the load modulation, as well as internal PA performance, it is necessary to include low-loss (0.2 dB) bi-directional couplers [82] in the combiner topology. Since the load-pull characterization of the internal PAs is performed at the MMIC bond wire plane, the combiner is designed at this plane as well. As such, the fixture transition and bi-directional couplers are measured and included in the combiner design, as detailed in Fig. 2.30. The SMA connector transition onto the PCB is also measured via TRL, so the design comes down to the microstrip circuit. It is worth noting that the off-chip combining adds significant loss (1 dB), but enables internal measurements as well as valuable comparison of several outphasing architectures described in the subsequent chapters.

Small-signal analysis has been applied to the lossless, non-isolated, three-port combiner to predict the

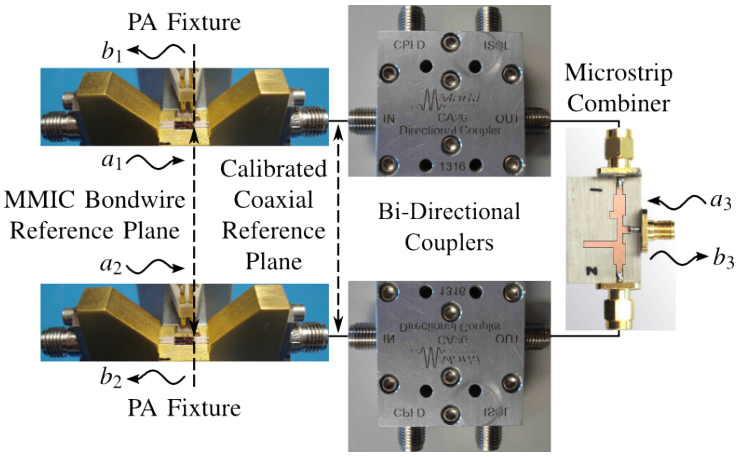


Figure 2.30: Detail of PA-combiner assembly. All internal measurements are de-embedded to the MMIC bond wire reference plane. The microstrip circuit is designed to provide load modulation.

load modulation at the fundamental frequency, yielding equations useful for designing load modulation circles. Because combiner design is done manually and visually, the speed of tuning is important. Being able to simulate without harmonic balance greatly improves the responsiveness to tuning. The reflected waves at the internal PA ports (1 and 2) are defined at the combiner reference plane in Fig. 2.30 as:

$$b_1 = S_{11}a_1 + S_{12}a_2 + S_{13}a_3 \tag{2.59}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 + S_{23}a_3 \tag{2.60}$$

In outphasing, the input power waves at the PA ports are symmetrically and oppositely phase shifted (θ) and possibly scaled (x) versions of each other:

$$a_1 = xa_2e^{j2\theta} \tag{2.61}$$

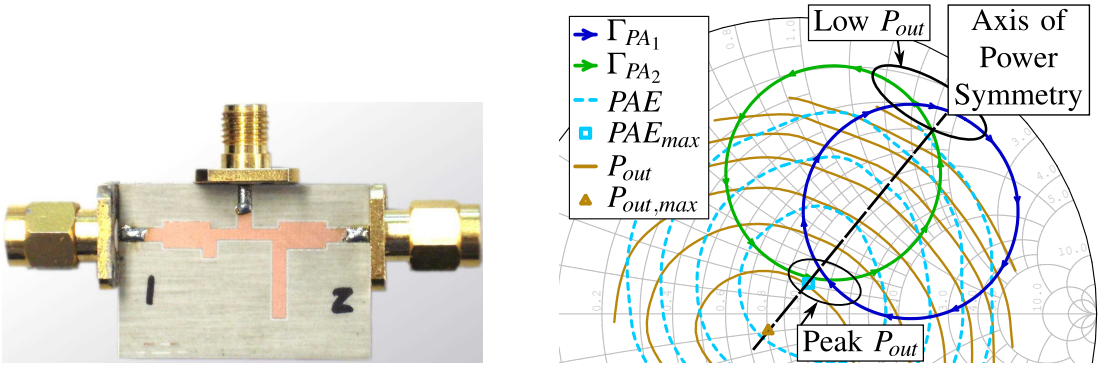
$$a_2 = \frac{1}{x}a_1e^{-j2\theta} \tag{2.62}$$

$$a_3 = 0 \tag{2.63}$$

Port 3 is assumed to be matched, x predicts the effect of PA output power imbalance, and θ is the outphasing angle. Substituting these excitations into (2.59) and (2.60), the reflected waves become:

$$b_1 = S_{11}a_1 + S_{12}\frac{1}{x}a_1e^{-j2\theta} \tag{2.64}$$

$$b_2 = S_{21}xa_2e^{j2\theta} + S_{22}a_2 \tag{2.65}$$



(a) (b)

Figure 2.31: (a) Photograph of Chireix combiner fabricated on 30 mil Ro4350B substrate. (b) P_{out} and PAE load-pull contours measured at 10.1 GHz, with the axis of power symmetry shown for design, and load modulation predicted by (2.66), (2.67). PAE contours are shown from 30% to 60% in 10 point increments and P_{out} contours are traced from 28 to 35 dBm in 1 dB steps. Smith chart is normalized to 50 Ω.

The reflection coefficients at each input port of the combiner, corresponding to the load modulation at the output of each internal PA, are found:

$$\Gamma_{PA1} = \frac{b_1}{a_1} = S_{11} + \frac{1}{x} S_{12}\, e^{-j2\theta} \tag{2.66}$$

$$\Gamma_{PA2} = \frac{b_2}{a_2} = S_{22} + x\, S_{21}\, e^{j2\theta} \tag{2.67}$$

With the aid of the small-signal analysis for quick and responsive simulation, the combiner can be designed. The microstrip circuit shown in Fig. 2.31a is based on a tee-junction topology and optimized with conjugate susceptances in the form of shunt stubs. The reactive compensation can also be realized by adding and subtracting the same electrical length from each branch in the tee-junction [61]. The calculated load modulation circles are overlaid on the measured load-pull characterization to visually analyze performance and provide immediate feedback for combiner tuning, as demonstrated in Fig. 2.31b.

This combiner design intersects the load modulation circles, Γ_{PA_1} and Γ_{PA_2}, at the measured peak efficiency at the same outphasing angle and remain in the highest efficiency impedance region possible, while balancing over the axis of power symmetry. A peak output power is achieved near peak efficiency due to the proximity to the maximum power load. The minimum output power is achieved when the loads reach the edge of the Smith chart.

2.4 Internal PA Performance and Load Modulation Measurements

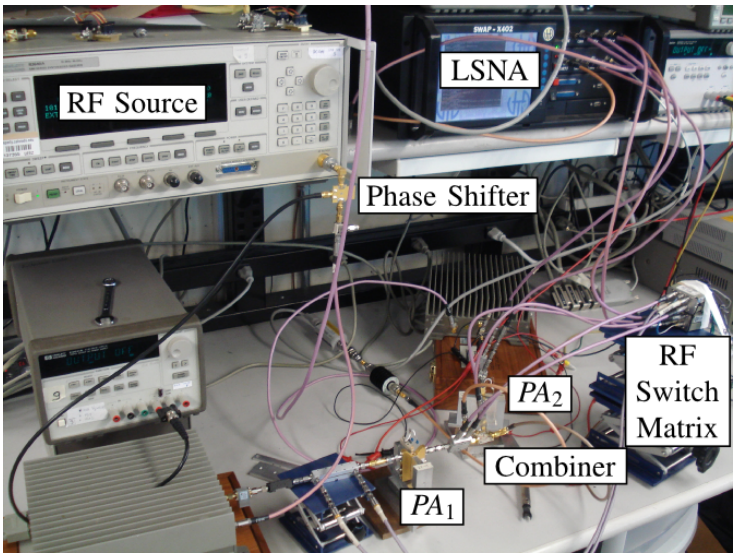
2.4.1 Measurement Setup and Calibration

A dedicated outphasing measurement setup is established for both internal PA and system measurements of various outphasing PAs [83]. An alternative is a near-field method used to measure internal interactions in a Doherty PA in [84], which requires specialized equipment (field probe, 3-D positioner) and continuous numerical simulation (HFSS). In this work, the absolute RF voltage and current waves of the internal PAs, within the outphasing system, are not only measured at the input, as done in [81], but also at the output through the inclusion of bi-directional couplers in the output combiner.

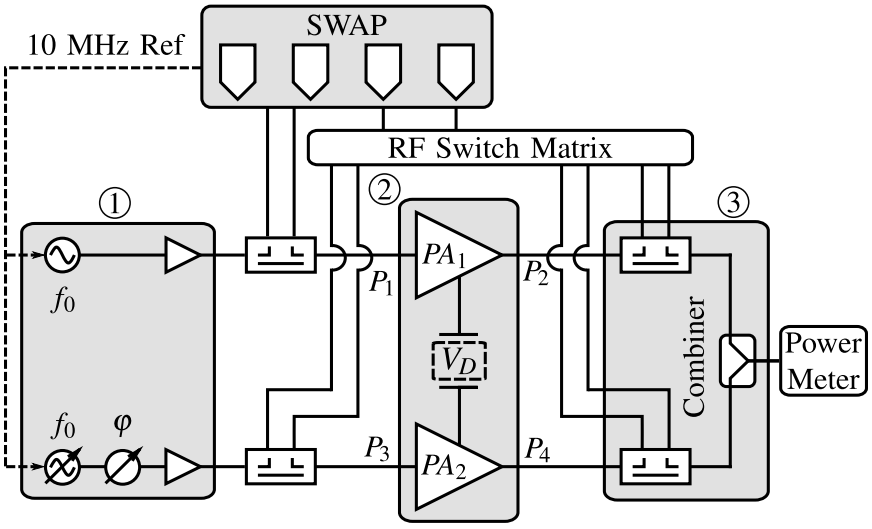
The measurement setup in Fig. 2.32 is an extension of the setup used to measure the internal PA MMICs in subsection 2.2.3. This work can be done with a VNA in receiver mode as shown in [85]. Typically, a four-channel, time-domain receiver is used to measure two-port devices under test (DUTs), but here it is extended to measure two two-port DUTs (internal PAs) with the use of an RF switch matrix, which includes four RF single pole, double throw (SPDT) switches (Agilent 8762C). The calibrated coaxial reference planes are denoted P_1, P_2, P_3, and P_4, which are at the coaxial launchers of the MMIC fixture. In this setup, port P_1 is measured continuously to provide a phase reference for the other three ports, which are measured sequentially using the RF switch matrix. Sequential measurements are aligned in the time-domain by adding a delay to force the phase of the fundamental voltage at port P_1 to 0°. Taking the input voltage as a phase reference is not an issue in outphasing, because the input power level remains constant and large.

The calibration of this system consists of three sequential two-port calibrations (P_1-P_2, P_1-P_3, P_1-P_4) corresponding to the three switch configurations. Each two-port calibration is the same as that presented in subsection 2.2.3, and uses a VNA SOLT method along with an absolute power calibration on port P_1 in forward mode with a power meter and an absolute phase calibration performed during the reverse "Thru" measurement. De-embedding of the MMIC fixture is done as described previously, so all following internal measurements are referenced to the MMIC bond wire plane at both the input and output.

During the outphasing measurements, the RF power applied to port P_1, the input of PA_1, is set for peak



(a)



(b)

Figure 2.32: (a) Photo and (b) diagram of the measurement setup, based on a 4-port LSNA. The two output couplers are included in the combiner, enabling measurement of internal load modulation and internal PA performance. A phase shifter sweeps the differential phase (φ), while the source for that branch varies amplitude to maintain a balanced input power level which saturates both PAs.

efficiency of the internal PA. A phase-shifter is placed after the second source and applied to port P_2, the input of PA_2, to sweep the differential phase between the internal PAs at the fundamental frequency, defined as:

$$\varphi = \angle \frac{v_2}{v_1} \tag{2.68}$$

The amplitude of the second source is adjusted for each phase to compensate for the variable loss in the

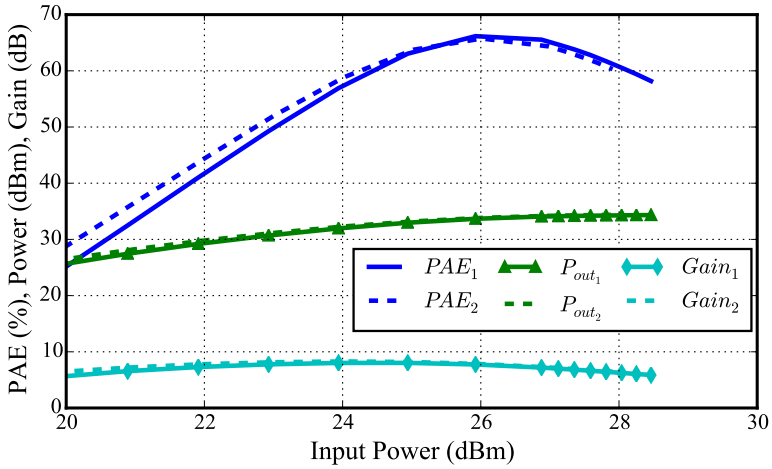


Figure 2.33: Performance comparison of the two internal MMIC PAs at 10.1 GHz, -4.2 V gate bias, and 20 V drain supply.

phase-shifter, and maintain input amplitude balance. In addition to constant bias outphasing measurements, the drain supply of each internal PA can be varied during measurement with this setup.

The two internal PA MMICs are chosen from a pool of measured chips to match as well as possible in terms of gain, output power, and efficiency in saturation at 10.1 GHz. Measurements of the two chips with 50 Ω loads are shown in Fig. 2.33. The two chips are chosen to operate at 26.0 dBm input power and -4 V gate bias, since they exhibit small differences in PAE, output power, and gain of 1.06 points, 0.21 dB, and 0.1 dB, respectively. Although the peak efficiency often occurs at 10.2 GHz for these MMICs, the small sacrifice in peak efficiency is worthwhile to achieve gain and output power balance. Differences in the load-pull characteristic of the two chips are unknown.

2.4.2 Measurement Results

The load modulation is measured for the first time in literature, and presented in Fig. 2.34, for which a differential phase sweep from -180° to 180° is performed. The peak PAE is obtained at the intersection of the load circles near the center of the Smith chart, as designed. The peak output power is achieved near that of the PAE due to the proximity of the load circles to the peak power impedance. The minimum output power occurs at the edge of the Smith chart.

Comparatively, the measured and designed (Fig. 2.31b) load modulation are very close, but the measured

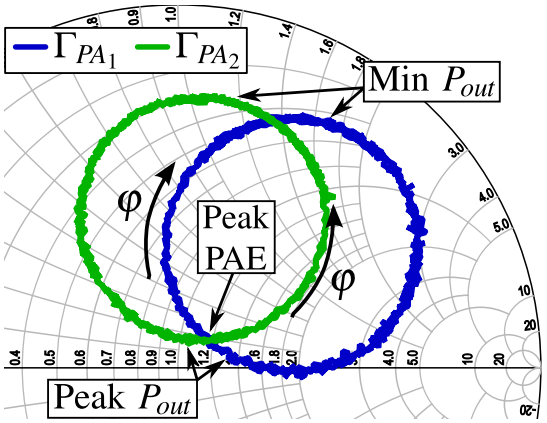


Figure 2.34: Measurement of load modulation presented to internal PAs (MMIC bond wire plane) when loaded with the non-isolated combiner from Fig. 2.31a.

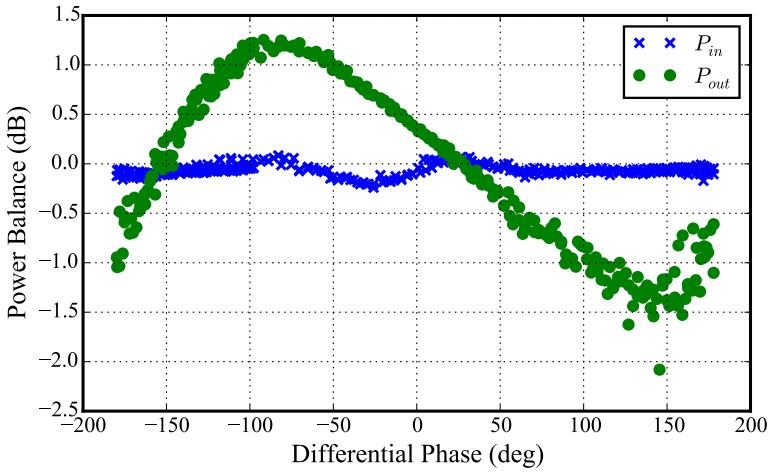


Figure 2.35: Measured power balance at the input and output of the internal MMIC PAs.

circles show a slight counterclockwise rotation as well as a slight enlargeing of the Γ_{PA_2} circle. This slight distortion is most likely induced by the combiner, since the internal PAs exhibit extremely small imbalances under 50 Ω loading. Fig. 2.35 demonstrates the power imbalance increase from the input of the internal PAs to the output. The available input power balance is maintained between -0.25 dB and 0.2 dB. A much larger variation, from -2 dB to 1.3 dB, is measured at the output of the internal PAs, which must be induced by the combiner, since the internal PA gain imbalance only contributes 0.1 dB. Differences in the internal PA load-pull characterization interact with imbalanced load modulation, resulting in internal PA output power imbalance and some load modulation distortion.

The performance of the internal PAs is shown in Fig. 2.36 for a 20 V supply voltage. The efficiency

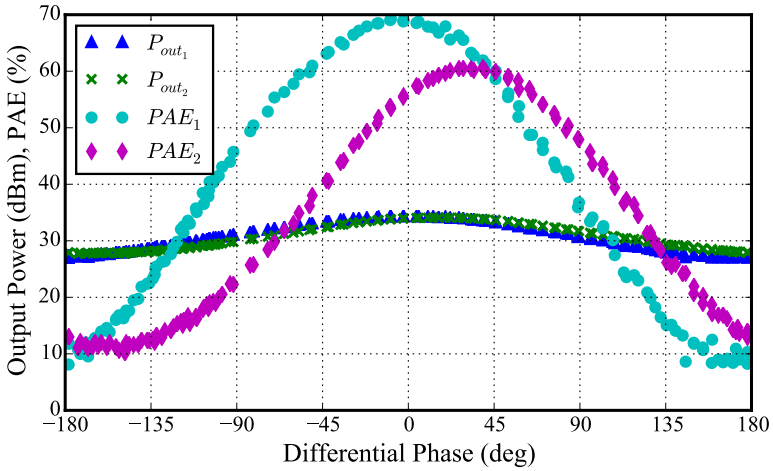


Figure 2.36: Measured internal PA output powers and efficiencies at 10.1 GHz with 26.5 dB input power and 20 V supply..

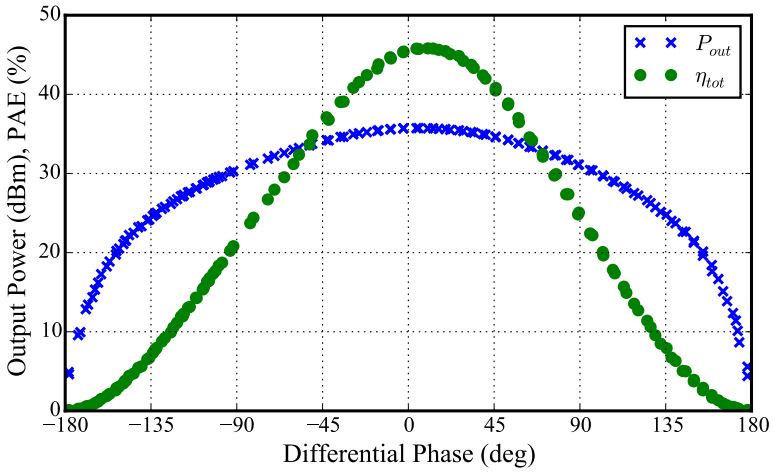


Figure 2.37: Measured system output power and efficiency.

of each MMIC PA varies significantly with differential phase due to the load modulation. The internal PA power imbalance induced by the combiner and available input power imbalance separates the efficiency traces. The internal PA efficiencies are equal when the power imbalance is zero, at about 45°. The combiner was designed based on the load-pull characterization of only one of the internal MMIC PAs, so the designed load modulation may have adversely affected the other. The output power imbalance can be taken into account in the load modulation analysis, (2.66) and (2.67), through the variable x.

Finally the system performance is shown in Fig. 2.37 as a function of outphasing angle, and in Fig. 2.38 as a function of normalized output power, which is helpful when considering efficiency for high PAR signals.

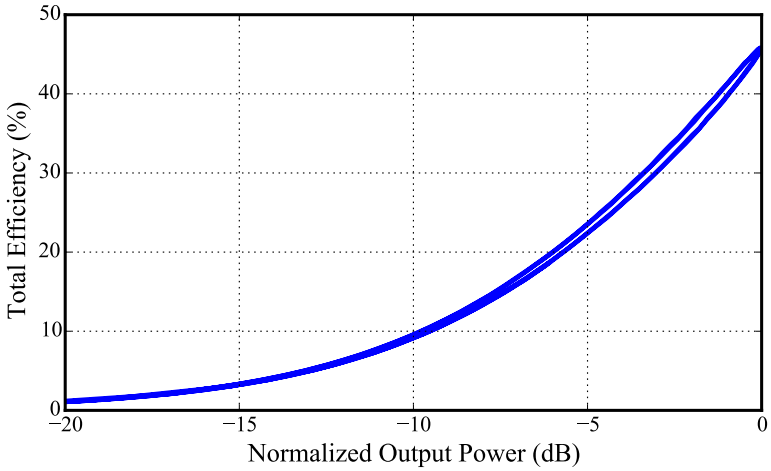


Figure 2.38: Measured system efficiency as a function of normalized output power.

Table 2.1: Chireix outphasing PA Performance

Architecture	Peak P_{out} (dBm)	Peak η_{tot} (%)	ΔP_{out} (dB)	Dynamic Range (dB)
Chireix	35.7	47.0	1.94	32.1

The system achieves a peak output power of 35.7 dBm at a differential phase of 5.4°, and a peak total efficiency of 47% at 10.3°. The ΔP_{out} (defined in subsubsection 1.1.3a) achieved for Chireix outphasing is 1.9 dB, and a dynamic range of 32.1 dB is measured, as summarized in Table 2.1.

2.4.3 Linearity Issues and Indicators

Although specific linearity measurements (two-tone test, ACLR, EVM) are not performed, linearity indicators can be ascertained from CW characterization. Sources of nonlinearity in traditional PAs, such as AM/AM and AM/PM, are not present in outphasing PAs, because the input amplitude is constant. Outphasing has different sources of nonlinearity entirely. Gain and phase imbalances between the branches are key contributors to nonlinearity in all outphasing PAs [86], and are caused by imbalances in the internal PAs and/or the combiner [87, 88]. Branch imbalances restrict the cancellation of the wide bandwidth quadrature signal component in LINC PAs, leading to residue in adjacent channels [89]. The maximum measured gain and phase imbalances are listed in Table 2.2. The gain imbalances measured under outphasing operation must stem from combiner imbalance and input power imbalance, since the internal MMIC PAs demonstrate

Table 2.2: Measured gain and phase imbalance

Architecture	Max Gain Imbalance (dB)	Max Phase Imbalance (deg)	Max Encoding Distortion (deg)
Chireix	2.01	25.01	5.39

less than 0.1 dB gain imbalance. In [90], the phase imbalance is shown to be more dependent on the gain imbalance than branch electrical length imbalance, which explains the measured phase imbalances without significant branch length differences.

An additional source of nonlinearity in outphasing PAs is the nonlinear phase transformation [87, 91], which can be separated into encoding and clipping distortions [42]. The encoding distortion is a phase offset that shifts the peak output power from $\theta = 0°$, which is visible in Fig. 2.37. In the LINC PA, encoding distortion is caused by branch imbalances, and imperfect combiner summing and subtracting in terms of phase. In Chireix outphasing, encoding distortion is inherent due to the impedance mismatching between the internal PAs and combiner [92], and arises theoretically when source impedance, R_S, is taken into account [39, 42]. In which case, the voltage across the differential load becomes [42]:

$$V_L = A_0 \frac{2j\sqrt{1 + B_C^2 R_S^2}}{2\frac{R_S}{R_L} + B_C^2 R_S^2 + 1} \sin(\theta + \alpha) \tag{2.69}$$

and the encoding distortion is:

$$\alpha = \arctan(B_C R_S) \tag{2.70}$$

After subtracting this offset, the clipping distortion is examined using two representations from measurements. First, the theoretical and measured differential phases are compared in Fig. 2.39 using the relationship between outphasing angle and normalized output power in [39] and in Equation 3.22:

$$\varphi = 2\arccos(10^{P_{out,n}/20}) \tag{2.71}$$

Chireix outphasing demonstrates up to 25° of deviation from the theoretical phase.

Second, the relationship between the outphasing angle and normalized output power is compared directly between theory and measurement in Fig. 2.40. Nearly 2.7 dB of deviation from the theoretical relationship occurs. In both cases, the solid blue trace shows the ideal (linear) characteristic. Although measurements

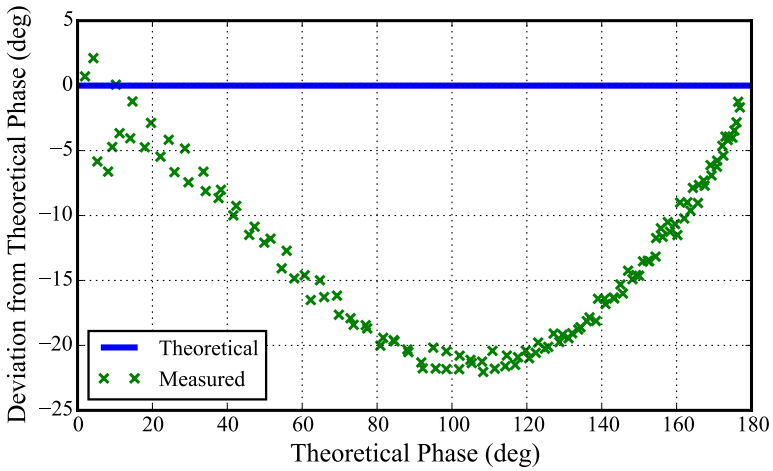


Figure 2.39: Measured differential phase deviation, showing up to 25° deviation from ideal operation.

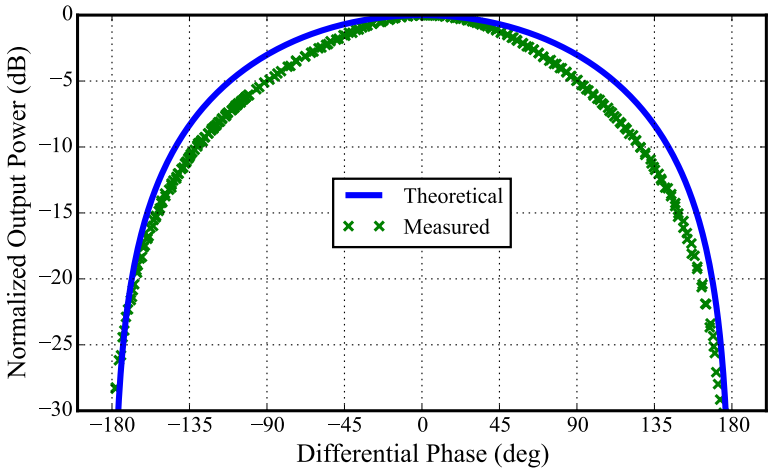


Figure 2.40: Measured output power with respect to differential phase, showing up to 2.7 dB deviation from ideal operation.

show concerning deviation from ideal operation, [48,91] have shown that Chireix outphasing can be linearized sufficiently for communication applications.

2.5 Conclusion

This chapter formed the foundation for the following three chapters by introducing a measurement setup devised to measure the internal PA performance and load modulation within an outphasing architecture. The flexible, MMIC-based outphasing PA utilized high efficiency GaN MMIC PAs and various off-chip

combiners, which enabled the internal measurements through the inclusion of bi-directional couplers. The load modulation within a Chireix outphasing PA was measured for the first time in literature. An approach to Chireix combiner design was discussed and aided by small-signal analysis, providing equations for predicting load modulation. Finally, the linearity issues common to all outphasing architectures were discussed, and the indicators of linearity found in static measurements of the Chireix outphasing PA prototype were described. The measurement setup, performance metrics of ΔP_{out} and dynamic range, and linearity indicators presented in this chapter are the foundation for comparison with the outphasing architectures presented in the next three chapters. Original contributions in this chapter include the following:

- The design and measurement of a 70% efficient (PAE) GaN MMIC PA with 2.7 W of output power [35].
- The derivation of equations predicting the load modulation of a three-port combiner under outphasing excitation with small-signal analysis to aid in Chireix combiner design [83].
- The development of an internal PA performance and load modulation measurement setup at 10.1 GHz, along with a hybrid Chireix outphasing PA enabling the measurement of absolute power waves internal to the architecture [83, 93, 94].
- The extension of the upper frequency of any outphasing PA implementation from 5 GHz [51] to 10.1 GHz [83, 93, 94].
- The measurement of load modulation internal to a Chireix outphasing PA for the first time in literature [83, 93, 94], demonstrating the variation of internal PA power and efficiency.

Chapter 3

LINC

Contents

LInear Amplification with Nonlinear Components (LINC) is a variation of outphasing proposed Cox in 1974 [33]. Although LINC shares the same outphasing modulated drive signal as its predecessor, Chireix outphasing, it operates in a fundamentally different way at the output. Chireix outphasing controls the output amplitude with load modulation, facilitated through a non-isolated combiner. LINC achieves output power control by vector addition with an isolated combiner. Chireix outphasing was developed for high efficiency amplification, while LINC was developed for linear amplification. Therefore, the choice between isolated (LINC) and non-isolated (Chireix) combining is a trade-off between linearity and efficiency [58, 95].

In this chapter, the internal PA performance and load modulation measurements from Section 2.4 are extended to the LINC PA by utilizing an isolated off-chip combiner. The theoretical foundation for LINC, including the details of input signal generation and drive, is presented in Section 3.1. Section 3.2 describes the design of the isolated combiner, as well as the measurement results.

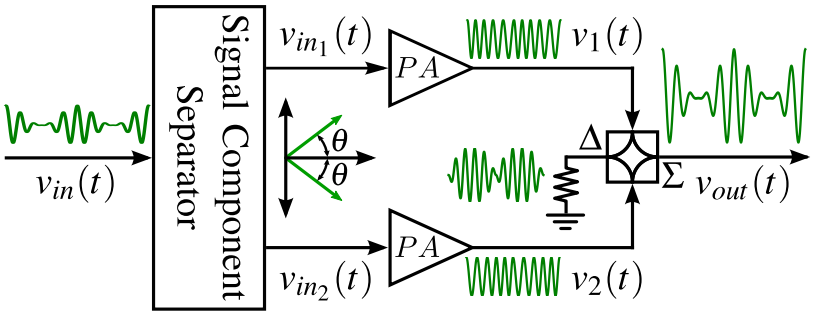


Figure 3.1: Block diagram of LINC power amplifier architecture.

3.1 LINC Theory

The original LINC theory presented in [33] has only been extended to consider the sources of linearity distortion in [86, 87]. The narrow focus is due to the minimal influence that the internal PA class has on system performance, only setting the peak efficiency, while branch gain and phase imbalances contribute significantly.

The LINC block diagram in Fig. 3.1 demonstrates the outphasing modulation common to all outphasing variations, as well as isolated combining at the output. The signal component separator converts the amplitude modulation of an amplitude and phase modulated signal into additional differential phase modulation, $\theta(t)$. In absence of amplitude modulation, the internal PAs are driven with a constant envelope signal, such that they operate at peak efficiency in saturation. Because the internal PAs operate in CW, they do not exhibit AM/AM or AM/PM distortion. At the output, an isolated combiner performs a vector addition of the amplified signals to reconstruct the envelope.

An amplitude and phase modulated signal at the input can be written in the time domain as:

$$v_{in}(t) = I(t)\cos(\omega t) + Q(t)\sin(\omega t) \tag{3.1}$$

$$v_{in}(t) = A(t)\cos[\omega t + \phi(t)] \tag{3.2}$$

where the signal components can be defined in Cartesian form as in-phase and quadrature components, $I(t)$ and $Q(t)$, or in polar form as amplitude and phase components, $A(t)$ and $\phi(t)$, respectively, and ω is the RF carrier frequency. The signal component separator decomposes the input signal into two branch signals such

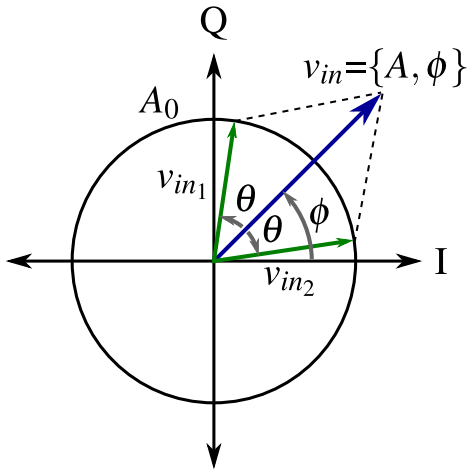


Figure 3.2: LINC vector diagram of input voltages as defined in Fig. 3.1

that:

$$v_{in}(t) = v_{in_1}(t) + v_{in_2}(t) \tag{3.3}$$

where the input voltage signals in each branch are defined from Fig. 3.2:

$$v_{in_1}(t) = A_0 \cos[\omega t + \phi(t) + \theta(t)] \tag{3.4}$$

$$v_{in_2}(t) = A_0 \cos[\omega t + \phi(t) - \theta(t)] \tag{3.5}$$

The amplitude constant is set as:

$$A_0 = \frac{A_{max}}{2} \tag{3.6}$$

where

$$A_{max} = \max|A(t)| \tag{3.7}$$

To be clear, the signals $v_{in_1}(t)$ and $v_{in_2}(t)$ are used to drive the internal PAs in LINC and Chireix outphasing.

Signal decomposition is based on the trigonometric identity:

$$\cos(A) + \cos(B) = 2\cos\left(\frac{A+B}{2}\right)\cos\left(\frac{A-B}{2}\right) \tag{3.8}$$

Applying this identity to the sum of $v_{in_1}(t)$ and $v_{in_2}(t)$:

$$v_{in_1}(t) + v_{in_2}(t) = 2\,\frac{A_{max}}{2}\cos[\omega t + \phi(t)]\cos[\theta(t)] \tag{3.9}$$

Substituting (3.9) into (3.3) yields:

$$A(t)\cos[wt + \phi(t)] = A_{max}\cos[\omega t + \phi(t)]\cos[\theta(t)] \tag{3.10}$$

which can be solved for the outphasing angle:

$$\theta(t) = \arccos\left[\frac{A(t)}{A_{max}}\right] \tag{3.11}$$

This is the key relationship for signal decomposition, representing how the amplitude modulation is transformed to differential phase modulation. When the amplitude of the input signal is maximum, then the two signals are driven in-phase, or θ is 0°. This differs from Chireix outphasing theory in Section 2.1, which makes use of a differential load rather than a summing combiner. When the amplitude is minimum, then the two signals are driven to be out-of-phase, or θ is 90°, so that a differential phase of 180° is achieved.

Now the output of the LINC PA can be examined mathematically to show how linear amplification is achieved. The output voltage of each PA is related to the input voltage by the voltage gain:

$$v_1(t) = G\, v_{in_1}(t) \tag{3.12}$$

$$v_2(t) = G\, v_{in_2}(t) \tag{3.13}$$

If the combiner is lossless, matched, and perfectly isolated, it will perform a perfect vector addition and subtraction. The output voltage can be taken as either, but in this case is taken as the sum:

$$v_\Sigma(t) = v_1(t) + v_2(t) = G\,[v_{in_1}(t) + v_{in_2}(t)] = G\, v_{in}(t) \tag{3.14}$$

since the branch voltage signals are decomposed so that their sum is equivalent to the input voltage signal. Because the internal PAs are operated at a constant input power level, their gain, G, is constant. Therefore, the relationship between the input and output voltages demonstrates linear amplification.

The voltage signal at the difference port of the isolated combiner will subtract the internal PA output voltages based on a complimentary trigonometric identity:

$$\cos(A) - \cos(B) = -2\sin\left(\frac{A+B}{2}\right)\sin\left(\frac{A-B}{2}\right) \tag{3.15}$$

which leads to the isolated port signal:

$$v_{\Delta}(t) = v_1(t) - v_2(t) = -GA_{max} \sin[\omega t + \phi(t)] \sin[\theta(t)] \tag{3.16}$$

Ignoring the high frequency term in the output voltages, the sum and difference powers can be written as a function of the outphasing angle modulation:

$$P_{\Sigma} = 2P_{out,PA} \cos^2 \theta \tag{3.17}$$

$$P_{\Delta} = 2P_{out,PA} \sin^2 \theta \tag{3.18}$$

Normalizing the output power on the sum port yields:

$$P_{out,n} = \cos^2 \theta \tag{3.19}$$

and converting to the logarithmic scale:

$$P_{out,n}\,(dB) = 10 \log(\cos^2 \theta) \tag{3.20}$$

Solving for the outphasing angle yields:

$$\theta = \arccos(10^{P_{out,n}/20}) \tag{3.21}$$

Or, in terms of differential phase:

$$\varphi = 2 \arccos(10^{P_{out,n}/20}) \tag{3.22}$$

To find the efficiency, the total DC power consumed by the internal PAs must be defined:

$$P_{DC,tot} = \frac{2P_{out,PA}}{\eta_{d,PA}} \tag{3.23}$$

The drain efficiency can then be defined:

$$\eta_d = \frac{P_{\Sigma}}{P_{DC,tot}} = \eta_{d,PA} \cos^2 \theta \tag{3.24}$$

The theoretical efficiency of a LINC PA is directly proportional to the output power delivered to a matched load, as shown in Fig. 3.3. This leads to a poor roll-off in efficiency, which drops to 50% at 3 dB power

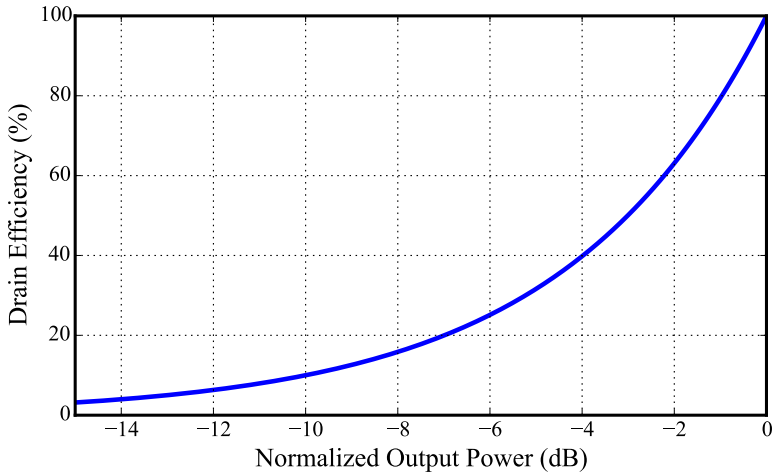


Figure 3.3: Theoretical efficiency of the LINC PA with the internal PA efficiencies set to 100%.

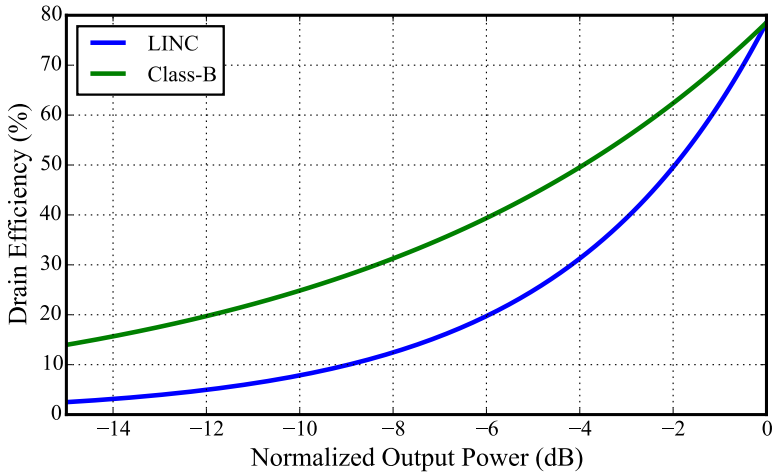
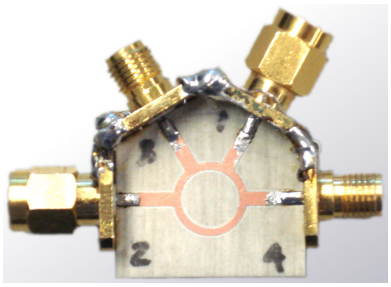
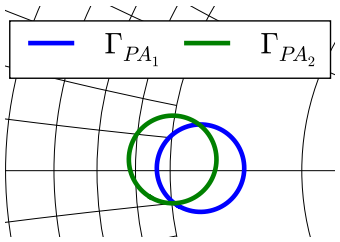


Figure 3.4: Comparison between the theoretical efficiencies of a LINC PA with optimum class-B internal amplifiers operating and a single-ended class-B PA.

backoff (50% output power) and 25% at 6 dB power backoff (25% output power). Note that the internal PA efficiencies are set to 100%, leading to a peak system efficiency of 100%. If the internal PA efficiencies are set to the maximum theoretical efficiency of the class-B amplifier, 78.7%, then a direct comparison can be made with a single-ended, class-B PA in Fig. 3.4. Class-B shows a better efficiency roll-off with power backoff than LINC. This serves to stress the point that LINC provides linear, not efficient, amplification.



(a)



(b)

Figure 3.5: (a) Photograph of rat-race combiner fabricated on 30 mil Rogers 4350B substrate for operation centered at 10.1 GHz. (b) Load modulation predicted by (2.66), (2.67) utilizing measured rat-race S-parameters. The Smith chart is normalized to 50 Ω and shown for $0.6 < r_L < 1.4$.

3.2 Internal PA Performance and Load Modulation Measurements

The internal PA performance and load modulation measurements presented in this section utilize the same setup as presented in Section 2.4, except a second power meter is placed at the isolated port of the combiner. The subsequent sections will discuss the combiner design, internal and system measurements, as well as linearity indicators.

3.2.1 Rat-Race Combiner

The rat-race combiner is chosen to isolate the two internal PAs at 10.1 GHz. A Wilkinson combiner is often used in LINC, but does not provide access to the isolated power at X-band. The combiner, shown in Fig. 3.5a, is implemented in a standard microstrip form, and fabricated on 30 mil Rogers 4350B substrate. In a perfectly power balanced simulation, nonzero load modulation is predicted by (2.66) and (2.67), as shown in Fig. 3.5b, leaving only the finite isolation of the combiner (24 dB) to be responsible. Fig. 3.6 shows the through loss from each of the PA input ports (1,2) to the output port (3) and the difference port (4), which varies between 0.6 and 0.8 dB at 10.1 GHz.

The phase between the internal PAs and the output ($\angle S_{31}$, $\angle S_{32}$) as well as the difference port ($\angle S_{41}$, $\angle S_{42}$) and more importantly the difference between those paths ($\angle S_{32} - \angle S_{31}$, $\angle S_{42} - \angle S_{41}$) are shown in Fig. 3.7. At 10.1 GHz the phase difference between the internal PAs and the output is 4.55°, while the phase difference

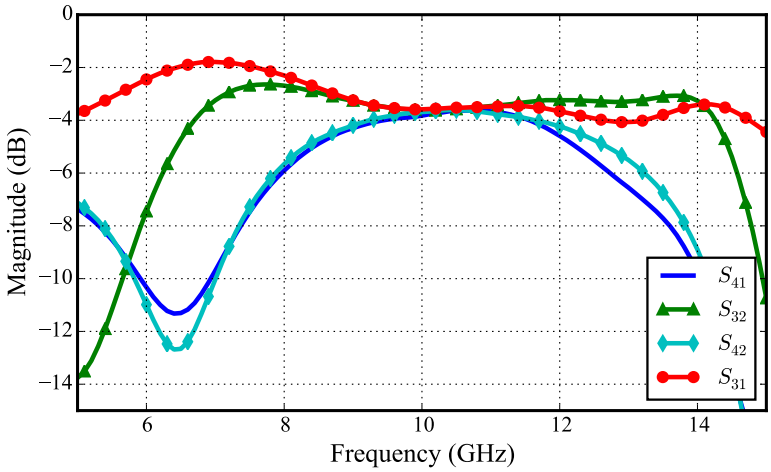


Figure 3.6: Measured through loss from each of the PA input ports (1,2) to the output port (3) and the isolated port (4).

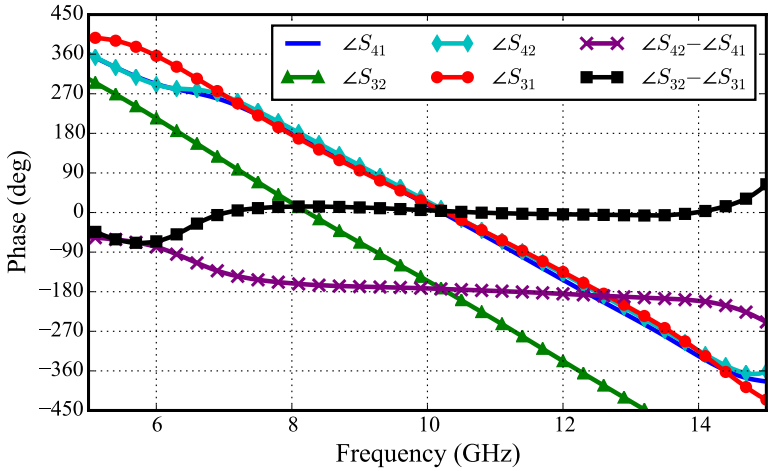


Figure 3.7: Measured phase between the input and output ports, and the difference between those paths.

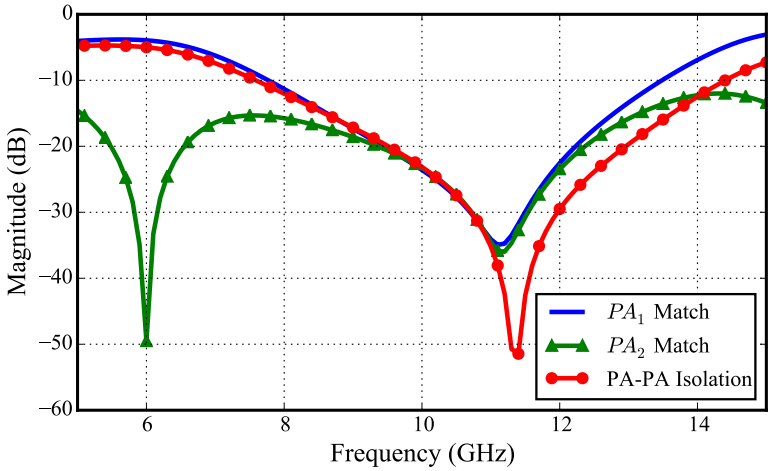


Figure 3.8: Measured input match and isolation between inputs.

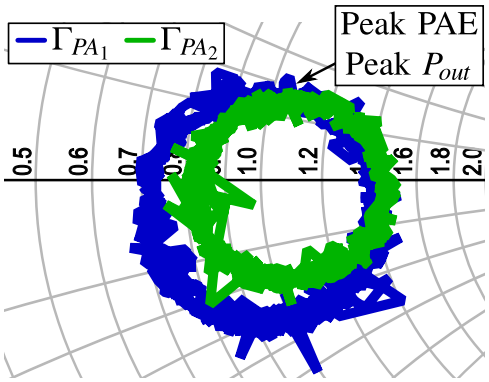


Figure 3.9: Measurement of load modulation presented to internal PAs (MMIC bond wire plane) when loaded with the isolated combiner from Fig. 3.5a.

between the internal PAs and the isolated port is -173.06°. Therefore, the internal PAs will sum at the output and subtract at the isolated port as desired. At 10.1 GHz, the match presented to each of the internal PAs is better than 24 dB, and the isolation between them is 24 dB, as shown in Fig. 3.8.

3.2.2 Measurement Results

The load modulation is measured for a differential phase sweep from -180° to 180° and shown in Fig. 3.9. As predicted in Fig. 3.5b, the limited isolation in this rat-race combiner (24 dB) allows for unintentional load modulation, which is a much smaller amount than observed for Chireix outphasing. Peak power and efficiency occur at the intersection of the load modulation circles. An infinitely isolated combiner would completely suppress load modulation.

The available input power balance is maintained between 0.05 dB and 0.7 dB. Internal PA output power balance shows a larger variation, from 0.4 dB to 1.7 dB. The previously measured internal MMIC PA gain imbalance only contributes 0.1 dB from the input to the output, so the remaining 0.9 dB must be induced by the combiner. In simulation, with balanced input power and identical internal PAs, up to 0.7 dB internal PA output power is induced by the measured combiner. Phase imbalances between the branches are not shown to affect the amplitude of measured power imbalances.

The performance of the internal PAs is shown in Fig. 3.10 for a 20 V supply voltage. The load variation is small enough to flatten out the efficiency response of the internal PAs with respect to differential phase,

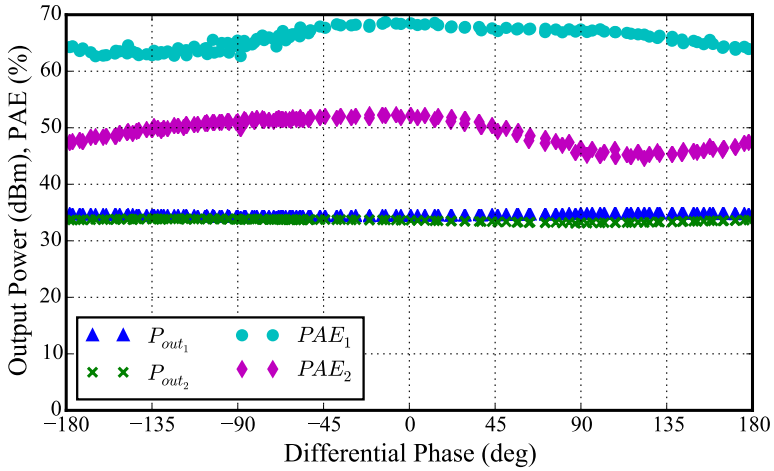


Figure 3.10: Measured internal PA output powers and efficiencies at 10.1 GHz with 26.5 dB input power and 20 V supply.

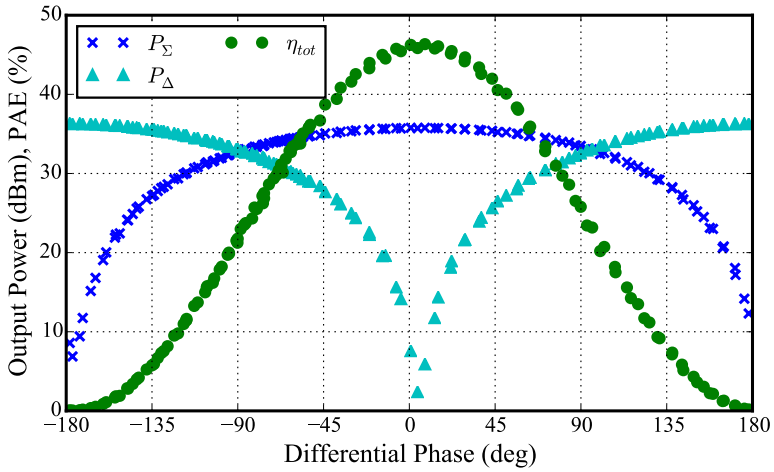


Figure 3.11: Measured system output power and efficiency.

limiting the variation to 7.5 points. As seen in Chireix outphasing, the internal PA efficiencies are separated due to differences in the load-pull characteristic of the two internal MMIC PAs, which come into effect through the internal PA output power imbalance induced by the small amount of load modulation.

The system performance is shown in Fig. 3.11. Now, there are two traces corresponding to RF output powers exiting the sum (Σ) and difference (Δ) ports of the isolated combiner, which are inversely proportional to each other. Since the internal PAs operate at nearly constant efficiency with differential phase, the system efficiency is most influenced by the output power characteristic, which rolls off sharply in LINC outphasing as $\cos^2\theta$. The system achieves a peak output power of 35.8 dBm and a peak total efficiency of 47.6% at a

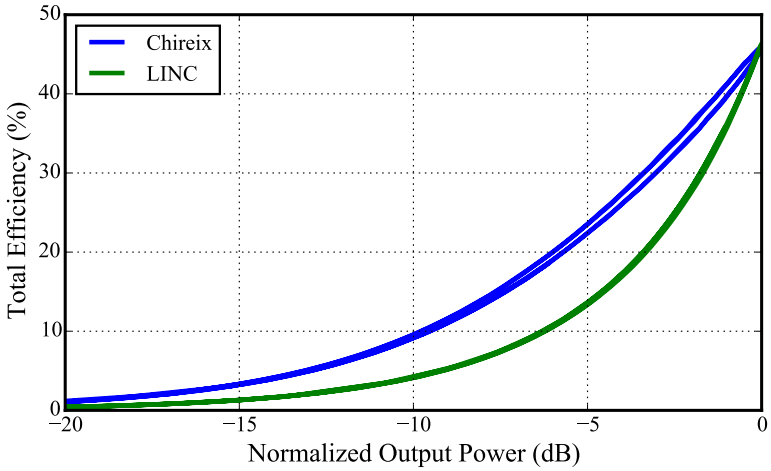


Figure 3.12: Comparison of measured system efficiency as a function of normalized output power, demonstrating the improvement of Chireix outphasing.

Table 3.1: Comparison of Chireix outphasing and LINC system performance

Architecture	Peak P_{out} (dBm)	Peak η_{tot} (%)	ΔP_{out} (dB)	Dynamic Range (dB)
Chireix	35.7	47.0	1.94	32.1
LINC	35.8	47.6	0.95	28.9

Table 3.2: Comparison of measured gain and phase imbalance

Architecture	Max Gain Imbalance (dB)	Max Phase Imbalance (deg)	Max Encoding Distortion (deg)
Chireix	2.01	25.01	5.39
LINC	1.26	20.67	3.74

differential phase of 3.7°.

Fig. 3.12 compares the system efficiency for Chireix outphasing with LINC as a function of normalized output power. At 6 dB back-off, Chireix outphasing achieves a 9.6 point improvement in total efficiency over LINC. A ΔP_{out} of 0.95 dB is achieved with a dynamic range of 28.9 dB, as summarized in Table 3.1.

3.2.3 Linearity Indicators

Table 3.2 summarizes the gain imbalance, phase imbalance, and encoding distortion. Gain imbalance is induced by the combiner, since the internal PAs demonstrate 0.1 dB gain imbalance when independently

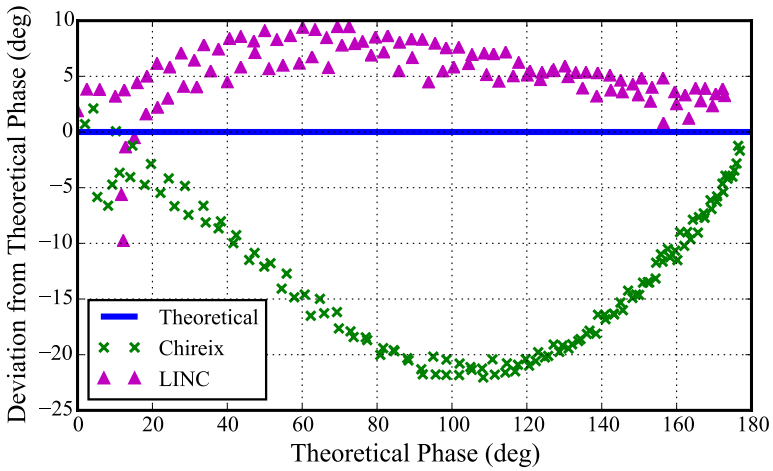


Figure 3.13: Comparison of measured differential phase deviation, showing only up to 8° deviation from ideal operation for the LINC PA.

measured. Along with the unknown internal PA phase imbalance, the induced gain imbalance contributes to the measured phase imbalance [90]. Gain imbalance contributes to encoding distortion through load modulation distortion, and indirectly through phase imbalance. In conjunction with phase imbalance, the deviation of the phase between the internal PAs and the sum and difference ports from 0° and 180° contributes directly to encoding distortion.

A comparison of linearity indicators, as described in detail in subsection 2.4.3, can be made between the LINC and Chireix outphasing prototypes. While the phase imbalance and encoding distortion are close, LINC achieves a 0.75 dB reduction in gain imbalance. More importantly, the nonlinear phase transformation is compared in Figs. 3.13 and 3.14. The near linear response of the LINC PA is established, as it only deviates by 8° from ideal phase and closely follows the power response. The comparison shows that more work will be required to linearize the Chireix outphasing PA as compared to the LINC PA.

3.3 Conclusion

The theoretical foundation for the input signal processing common to all outphasing amplifiers was presented. The internal PA performance and load modulation measurement setup in Chapter 2 was extended in this chapter to LINC, through the design and fabrication of an isolated, off-chip, rat-race combiner. Utilizing

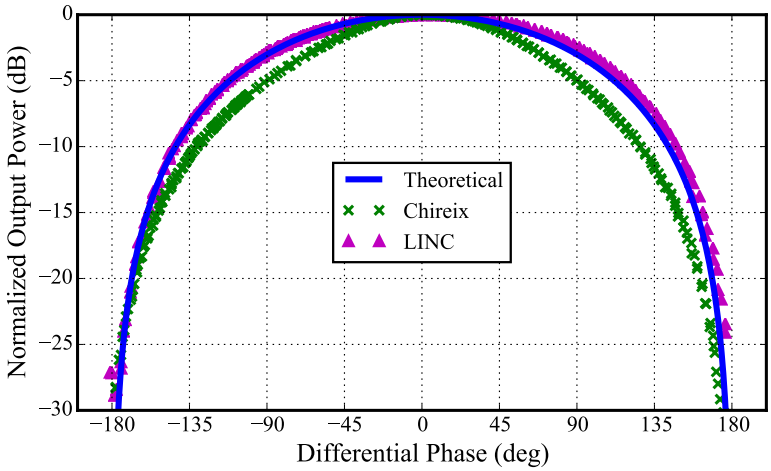


Figure 3.14: Comparison of measured output power with respect to differential phase, showing negligible deviation for the LINC PA.

the same internal PAs enabled a direct comparison between the LINC and Chireix outphasing PAs, which clearly exhibited something that is often confused in literature: the LINC PA amplifies linearly, while the Chireix PA amplifies efficiently. Original contributions in this chapter include the following:

- The extension of the internal PA performance and load modulation measurement setup to isolated outphasing or LINC [83, 93, 94].
- The measurement of load modulation internal to a LINC PA is demonstrated for the first time in literature [83, 93, 94]. In this cases, it is minimal, yet nonzero, due to the finite isolation of the combiner.
- Direct comparison between the LINC and Chireix outphasing PAs is enabled by this measurement setup, which utilizes the same internal PAs. The efficiency improvement of Chireix outphasing, and the linear amplification of LINC are both highlighted [83, 93, 94].

Although these measurements incur extra loss in order to explore the dynamics within the outphasing architecture, the very low measured ΔP_{out} values indicate improvements may be necessary to efficiently amplify high PAR signals. In the next chapter, the addition of discrete supply modulation to the LINC PA architecture is examined.

Chapter 4

Supply Modulated LINC

Contents

Demonstrated in the previous chapter both theoretically and experimentally, the efficiency of the LINC PA decays rapidly with drive level reduction. Supply modulation can be incorporated to improve the efficiency at back-off, thereby improving the average efficiency of amplifying high PAR signals. In this case, supply modulation only needs to perform coarse output power control by discrete steps, since outphasing modulation performs fine control.

In envelope tracking, the supply modulator (SM) must have a *continuously* variable output. Achieving the required modulation bandwidth, which must be at least five times that of the signal for linearization, is very difficult and currently the bottleneck of the ET PA. Additionally, the supply modulator must be able to swing the voltage very fast for high PAR signals, while providing a lot of power, corresponding to a very high slew rate [96]. An eight-phase buck converter operating at a peak power of 176 W, with slew rates up

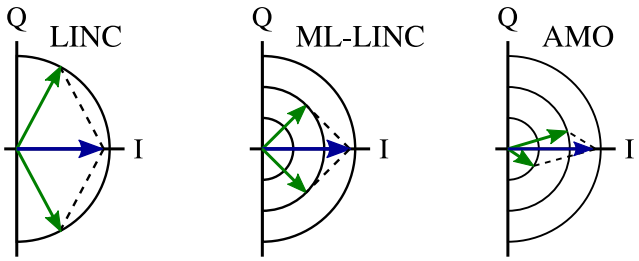


Figure 4.1: LINC, ML-LINC, and AMO vector diagram.

to 3 kV/µs, is shown to track a 5 MHz, 5 dB PAR signal with unknown linearity at 61.3% overall efficiency (including gate drivers) in [97]. A GaN-on-SiC, two-phase synchronous buck converter MMIC operating at a peak power of 10 W is shown to track a 20 MHz, 4.3 dB PAR LTE signal with 1.6% normalized RMS error (NRMSE) at 80.1% overall efficiency in [98, 99]. A discrete supply modulator, on the other hand, is much simpler than its continuous counterpart. A discrete SM may be implemented as a simple switch network [100] or a digital-to-analog converter (DAC) architecture [101]. A 3-bit power-DAC operating at a peak power of 159 W, with slew rates up to 4.23 kV/µs, is shown to track a 20 MHz, 11 dB PAR LTE signal with 5% NRMSE at 78.2% overall efficiency in [101].

Since the isolated combiner at the output of a LINC PA performs a vector combination of the internal PA output voltages, the concept of supply modulated LINC can be understood through vectors. Fig. 4.1 shows the vector addition at the output of the LINC, multi-level LINC (ML-LINC), and asymmetric multilevel outphasing (AMO), where the green vectors represent the internal PA output voltages, and the blue vector is the sum of them, or the load voltage. The discrete supply levels are represented by concentric circles.

The addition of supply modulation allows for a reduction in outphasing angle, thereby reducing the RF power dissipated in the isolated combiner. In ML-LINC, the discrete supply levels are varied symmetrically [102]. These levels can be optimized based on the PDF of the input signal [103, 104]. In AMO, supply levels are allowed to vary independently, providing an increase in efficiency through further reduction of the outphasing angle [104, 105]. AMO has been validated experimentally with GaN, class-E internal PAs at 1.95 GHz in [106] and with CMOS, class-E internal PAs at 2.4 Ghz in [100]. Both works implement a switching network for the discrete supply modulator, and perform linearized modulated measurements.

In this chapter, the internal PA performance and load modulation measurement setup for the LINC

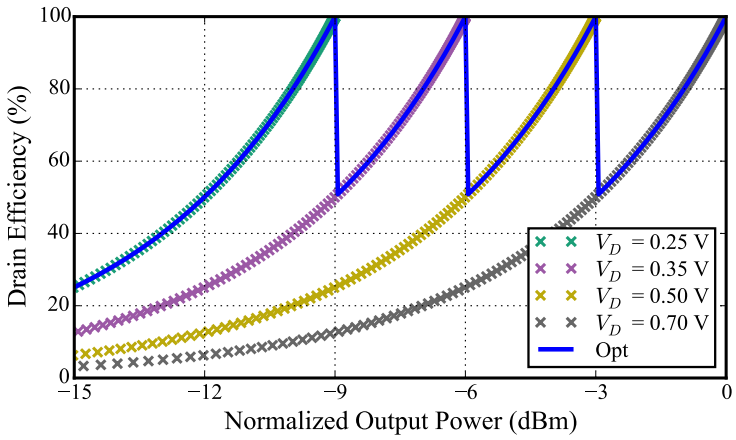


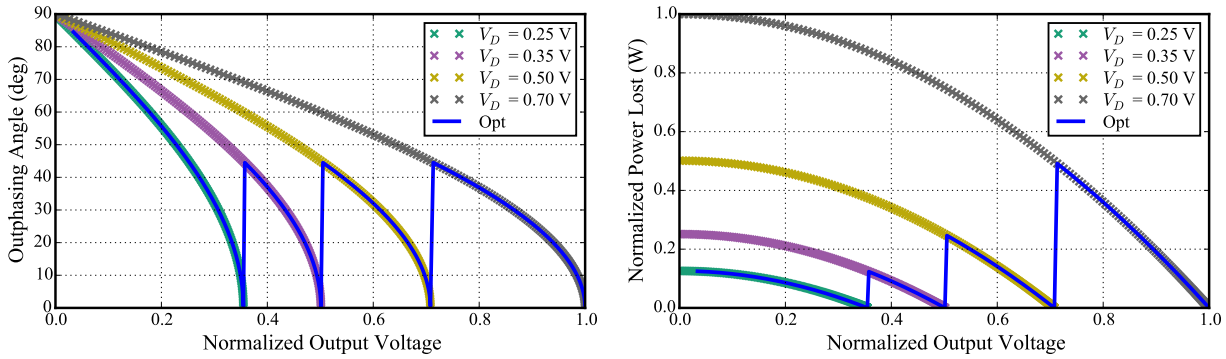
Figure 4.2: Theoretical efficiency of the ideal, four level ML-LINC PA, demonstrating improvement for the optimal trajectory.

PA in Section 3.2 is extended to include discrete supply modulation. The theoretical foundation for the incorporation of symmetric and asymmetric discrete supply modulation with outphasing is presented in Section 4.1 and Section 4.2, respectively. Section 4.3 demonstrates the measured results for these two variations of the LINC PA architecture.

4.1 Multi-Level LINC Theory

In the LINC PA, the amplitude of the output vectors is fixed by the constant supply voltage. On the other hand, ML-LINC allows the supply voltages to vary symmetrically, meaning the green vectors in Fig. 4.1 change in amplitude simultaneously. Now multiple combinations of supply levels and outphasing angles can realize a given output vector. The optimal solution simultaneously minimizes the supply voltages and the outphasing angle. Therein lies the improvement of ML-LINC. The decrease in the required range of outphasing angle directly decreases the power dissipated in the isolated combiner, since its maximum and minimum correspond to those of the outphasing angle.

ML-LINC produces a peak in efficiency for each supply level. Each normalized supply level can be determined from the normalized output power at which the efficiency peaks are desired from (4.15). Fig. 4.2 shows the efficiency for four-level ML-LINC, where the supply levels (0.25, 0.354, 0.5, and 0.707 V) peak



(a) (b)

Figure 4.3: (a) Theoretical outphasing angle for the ideal, four level ML-LINC PA, demonstrating a decrease for the optimal trajectory. (b) Theoretical RF power dissipated in the isolated combiner, with decreases corresponding to those in the outphasing angle.

the efficiency at 9, 6, 3, and 0 dB back-off. Essentially, the LINC PA efficiency curve is reproduced for each additional supply level, so the different colored curves correspond to the four supply voltages listed. Traveling along each curve is still accomplished by varying the outphasing angle. The blue trace demonstrates the optimal trajectory, and its efficiency improvement over that of LINC.

Fig. 4.3 shows both the outphasing angle as well as power dissipated in the isolated combiner as a function of normalized output voltage. For any single supply level, an outphasing angle of 90° must be reached to minimize the output power, dissipating all generated RF power in the isolated combiner. However, for multiple supply levels, the outphasing angle can be minimized over a larger portion of the output voltage, minimizing the RF power lost in the combiner, and maximizing efficiency. Still, all generated RF power is lost to achieve the minimum output power, but at a lower supply level the internal PAs generate much less power.

4.2 Asymmetric Multilevel Outphasing Theory

In AMO, the supply levels are allowed to vary independently. Fig. 4.4 shows an example of AMO vectors, where the green vectors v_1 and v_2 represent the output voltage of the internal PAs, and the blue vector v_{out} is the load voltage. The three supply levels (concentric circles) have amplitudes A_1, A_2, and A_3. Now, even

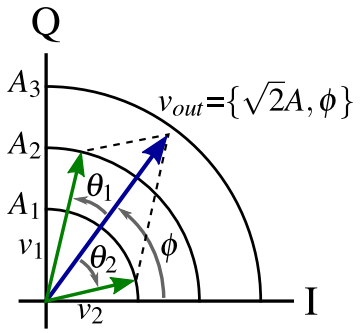


Figure 4.4: Detailed AMO vector diagram.

more combinations of supply levels ($|v_1|$ and $|v_2|$) and outphasing angles (θ_1 and θ_2) can realize a given output vector, since each can be varied independently. As will be shown, some constraints must be placed on these variables in order to maintain the required common phase, $\phi(t)$ [107].

First, consider the conservation of energy for a lossless combiner. The sum of the input powers (internal PA outputs) must equal the sum of the output powers (sum and difference ports):

$$P_1 + P_2 = P_\Sigma + P_\Delta \tag{4.1}$$

If we consider that the power is proportional to the square of the vector amplitude, then this equation can be rewritten as:

$$A_1^2 + A_2^2 = (A_1 + A_2)^2 + (A_1 - A_2)^2 \tag{4.2}$$

which incorrectly results in:

$$A_1^2 + A_2^2 = 2A_1^2 + 2A_2^2 \tag{4.3}$$

In order to satisfy the conservation of energy, the output voltage vector must be defined as:

$$v_{out} = \frac{1}{\sqrt{2}}(v_1 + v_2) \tag{4.4}$$

or

$$(v_1 + v_2) = \sqrt{2}v_{out} \tag{4.5}$$

which is reflected in the vector diagram in Fig. 4.4.

Now the outphasing angles, θ_1 and θ_2, can be found using the law of cosines on their respective triangles in the vector diagram:

$$\theta_1 = \arccos\left[\frac{A_1^2 + 2A^2 - A_2^2}{4A_1A/\sqrt{2}}\right] \tag{4.6}$$

$$\theta_2 = \arccos\left[\frac{A_2^2 + 2A^2 - A_1^2}{4A_2A/\sqrt{2}}\right] \tag{4.7}$$

These equations ensure that the common phase is not altered, while also reducing the independent variables to A_1 and A_2, or $|v_1|$ and $|v_2|$, the two supply levels of the internal PAs. For each output voltage or power, all combinations of supply levels can be considered. The optimal solution minimizes the differential phase, or the difference between the outphasing angles, maximizing efficiency. The output voltage vector can be written from the vector diagram as:

$$v_{out} = \frac{A_1\cos\theta_1 + A_2\cos\theta_2}{\sqrt{2}} \tag{4.8}$$

The total input voltage is:

$$v_{in} = A_1 + A_2 \tag{4.9}$$

Since efficiency is the ratio of the output and input powers, and power is proportional to the square of the voltage, the efficiency can be written as:

$$\eta = \frac{(A_1\cos\theta_1 + A_2\cos\theta_2)^2}{2(A_1 + A_2)^2} \tag{4.10}$$

The theoretical efficiency for AMO is compared to ML-LINC in Fig. 4.5 for the same four supply levels. AMO provides more replicated efficiency curves from the $\binom{N}{2} + N$ combinations of supplies. Notice that the additional peaks do not reach 100%. In an isolated combiner, power will be dissipated in the difference port if the input amplitudes (supply levels) are different, even if the phases are equal. Due to the decrease in efficiency for increasingly separated supply levels, AMO is usually restricted to utilize only symmetric levels and combinations of adjacent levels. In this case, n supply levels will provided $2n - 1$ peaks in efficiency [107].

The efficiency peaks occur at the maximum output power for each given supply level. Therefore the relationship between output power and supply level is found, so the supply levels can be chosen set the

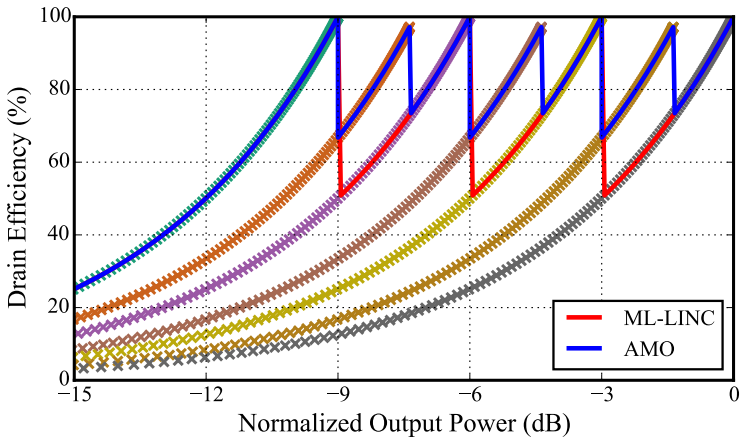


Figure 4.5: Theoretical efficiency of the ideal, four level AMO PA, demonstrating improvement for the optimal trajectory beyond that of ML-LINC.

locations of the efficiency peaks in terms of normalized output power. According to (4.8), the maximum output voltage is produced with the maximum supply level, when θ_1 and θ_2 are zero:

$$\max(v_{out}) = \frac{2A_{max}}{\sqrt{2}} \tag{4.11}$$

Taking the square of the voltage yields the maximum output power:

$$\max(P_{out}) = 2A_{max}^2 \tag{4.12}$$

Normalizing the maximum output power to 1 W, yields the maximum supply level:

$$A_{max} = \frac{1}{\sqrt{2}} \tag{4.13}$$

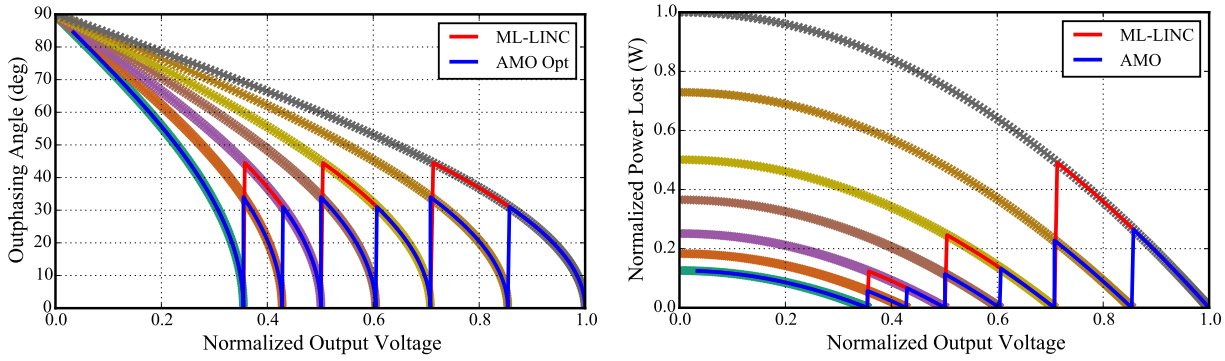
The normalized output power in decibels can be written as a function of the normalized supply level:

$$P_{out,n} = 10\log\left[2\left(\frac{A_n}{A_{max}}\right)^2\right] \tag{4.14}$$

A_n must be less than A_{max}. Solving for the normalized supply, one can choose the supply levels to peak efficiency at the desired normalized output powers:

$$\left(\frac{A_n}{A_{max}}\right) = \sqrt{\frac{10^{P_{out,n}/10}}{2}} \tag{4.15}$$

AMO maintains an even further reduced outphasing angle, as shown in Fig. 4.6a, causing a further decrease in RF power dissipated in the isolated combiner, as shown in Fig. 4.6b, as compared to ML-LINC.



(a) (b)

Figure 4.6: (a) Theoretical outphasing angle for the ideal, four level AMO PA, demonstrating a decrease for the optimal trajectory. (b) Theoretical RF power dissipated in the isolated combiner, with decreases corresponding to those in the outphasing angle. In both cases, greater reduction is achieved by AMO than ML-LINC.

No obvious penalty exists for implementing independent supply variation as in AMO, as compared to symmetric variation in ML-LINC.

4.3 Internal PA Performance and Load Modulation Measurements

The internal PA and load modulation measurements presented in this section are based on the same setup in Section 2.4 with the same adjustments in Section 3.2. To characterize the LINC PA with discrete supply modulation, the drain voltage power supply is stepped, and for each level a full phase sweep is performed. Implementing an actual discrete supply modulator will decrease the system efficiency according to its efficiency, which should be more than 80% or 90% depending on the signal and power level [97–99, 101]. The initial calibration is not affected by operating the internal PAs at varying supply levels.

4.3.1 ML-LINC Measurement Results

The measured ML-LINC total efficiency in Fig. 4.7 is obtained for a drain voltage sweep from 10 to 20 V in 2 V steps, corresponding to each trace of different color. The optimal operating points (solid blue) are chosen for peak total efficiency, and aligns with the method in [102] of choosing the supply level to be as small as possible while reaching the desired output power. The optimal trajectory improves the efficiency by

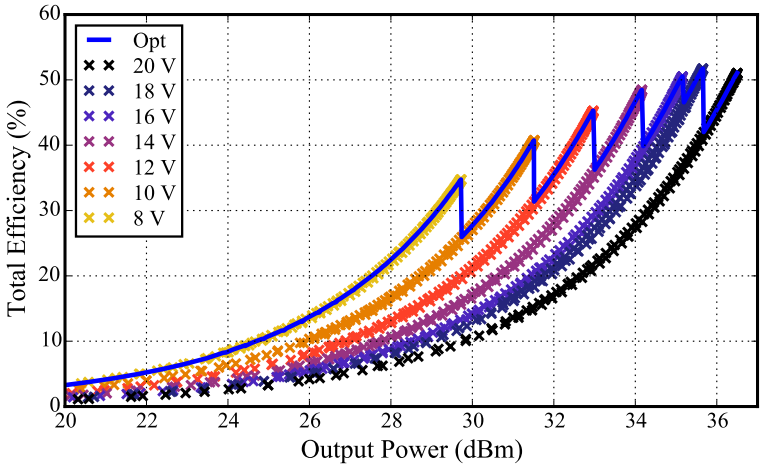


Figure 4.7: Measured system total efficiency of the ML-LINC PA for swept differential phase at drain voltages of 10, 12, 14, 16, 18, and 20 V demonstrating advantageous new peaks.

Table 4.1: Measured system performance of supply modulated LINC PAs

Architecture	Peak P_{out} (dBm)	Peak η_{tot} (%)	ΔP_{out} (dB)	Dynamic Range (dB)
ML-LINC	36.5	51.7	3.1	39.5
AMO	36.5	52.5	4.9	41.1

10 to 26 points beyond the 20 V case.

Table 4.1 summarizes the performance of ML-LINC, showing a ΔP_{out} improvement of 1.2 dB over Chireix outphasing and 2.15 dB over LINC. In the figures following, the optimal operation (blue circles) shows discontinuities corresponding to discrete supply steps. Fig. 4.8 exhibits the reduction in differential phase, where the optimal operation only requires $-24^\circ < \varphi < 55^\circ$ above 28 dBm (8.5 dB back-off), which is a 60° reduction compared to the 20 V supply case.

The reduced differential phase improves the total efficiency because less power is dissipated in the isolated combiner. In Fig. 4.9, the optimal operation dissipates less than 0.92 W of RF power in the combiner, and provides 3.28 W of improvement over 20 V operation at 16.5 dB back-off (20 dBm). Aside from this expected mechanism for efficiency improvement, Fig. 4.10 demonstrates a secondary effect. As in envelope tracking, the DC power consumed by the internal PA reduces with supply voltage. Below 29.6 dBm (7 dB back-off), the DC power consumption is reduced by 6.6 W. Therefore, the benefits of supply modulation contribute to improve the performances of both the internal PAs and combiner.

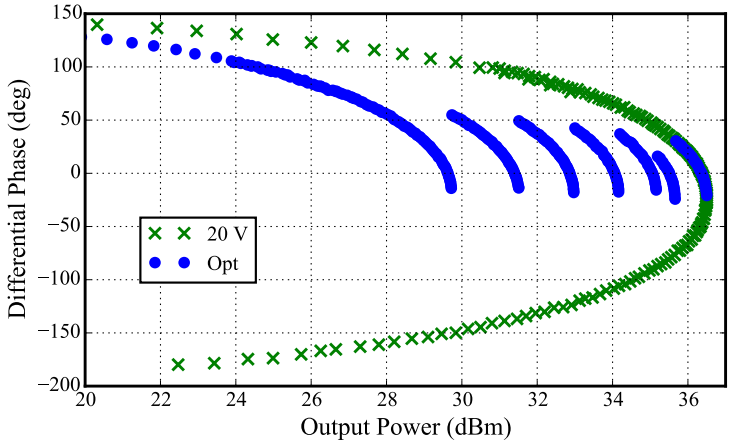


Figure 4.8: Comparison of measured differential phase between constant 20 V and optimal ML-LINC operation, demonstrating a reduction for ML-LINC.

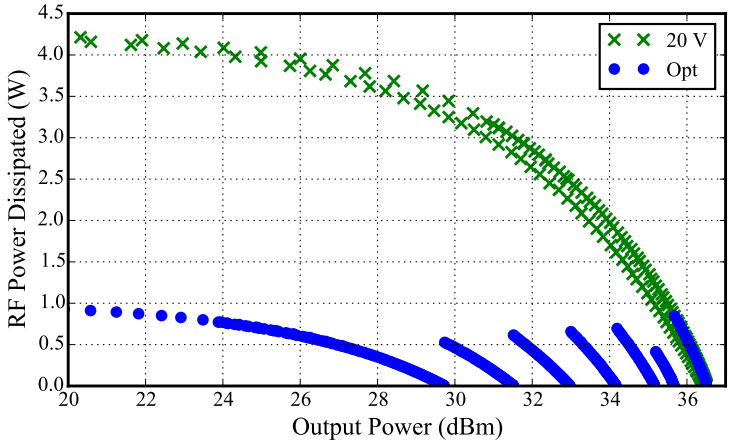


Figure 4.9: Comparison of measured RF power dissipated in the isolated combiner between constant 20 V and optimal ML-LINC operation, which remains below 0.92 W up to 6.5 dB back-off for ML-LINC.

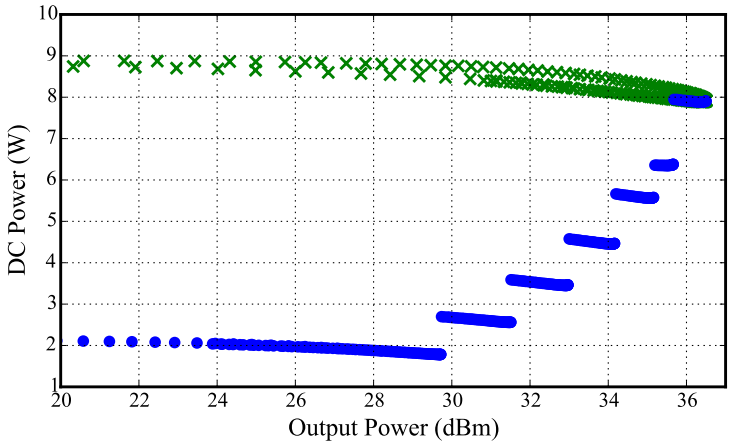


Figure 4.10: Comparison of measured DC power consumption between constant 20 V and optimal ML-LINC operation, demonstrating power savings of up to 6.6 W by ML-LINC.

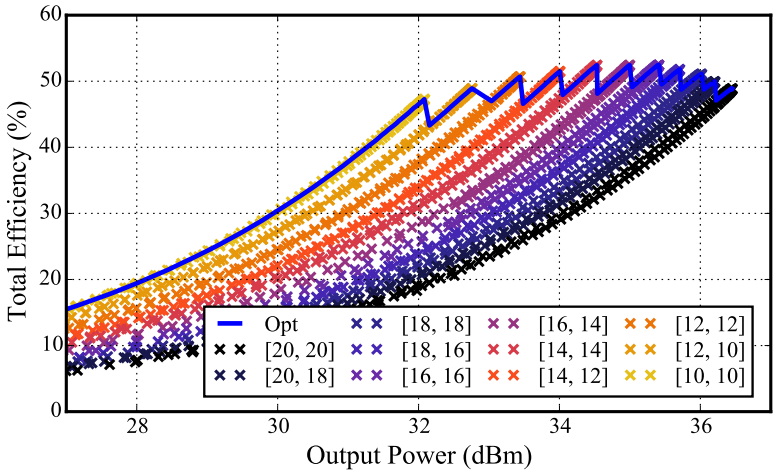


Figure 4.11: Measured system total efficiency of the AMO PA for swept differential phase at drain voltages of 10, 12, 14, 16, 18, and 20 V and combinations of adjacent levels, demonstrating nearly twice as many peaks as ML-LINC.

4.3.2 AMO Measurement Results

For the AMO measurements, the supplies are varied independently in all combinations of drain voltages from 10 to 20 V in 2 V steps. The measured total efficiency in Fig. 4.11 only shows symmetric levels, and combinations of adjacent levels. In doing so, the six supply voltages produce eleven peaks in efficiency, which is five more than ML-LINC, creating a much smoother optimal trajectory. This improvement would be even more pronounced for fewer supply levels. Table 4.1 summarizes the performance showing a further ΔP_{out} improvement of 1.8 dB compared to ML-LINC.

As in ML-LINC, the differential phase range is reduced for AMO in Fig. 4.12 to $-75^\circ < \varphi < -5^\circ$ down to 32 dBm (4.5 dB back-off), which is 55° of improvement over 20 V supply case. The same two mechanisms are again reducing lost power. Fig. 4.13 illustrates the reduced RF power wasted in the isolated combiner, remaining below 0.48 W down to 30 dBm (6.5 dB back-off), where an improvement of 2.5 W is achieved. Fig. 4.14 validates the supply modulation effect through the decreased DC power consumption of the internal PA, which is improved by 4.9 W below 31.2 dBm (4.4 dB back-off). As shown in the total efficiency of AMO, the increased number of supply level combinations provides a more continuous reduction in wasted RF and DC power.

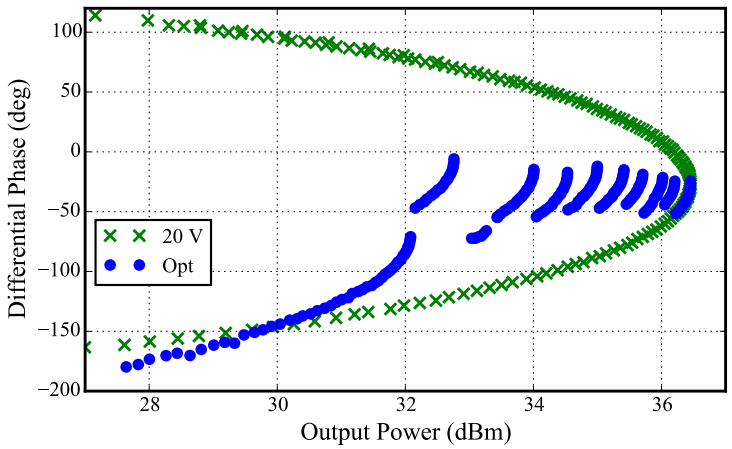


Figure 4.12: Comparison of measured differential phase between constant 20 V and optimal AMO operation, demonstrating a reduction for AMO.

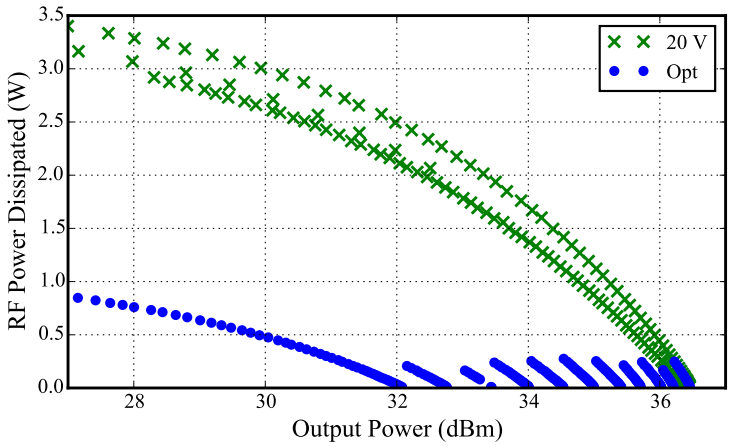


Figure 4.13: Comparison of measured DC power consumption between constant 20 V and optimal AMO operation, demonstrating power savings of up to 4.9 W by AMO.

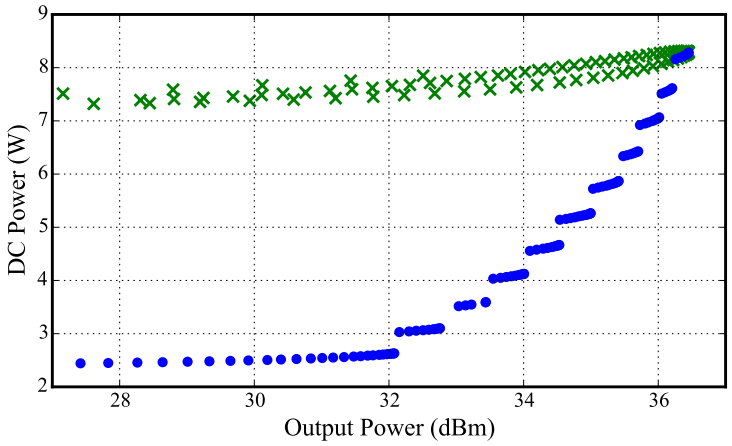


Figure 4.14: Comparison of measured RF power dissipated in the isolated combiner between constant 20 V and optimal AMO operation, which remains below 0.48 W up to 6.5 dB back-off for AMO.

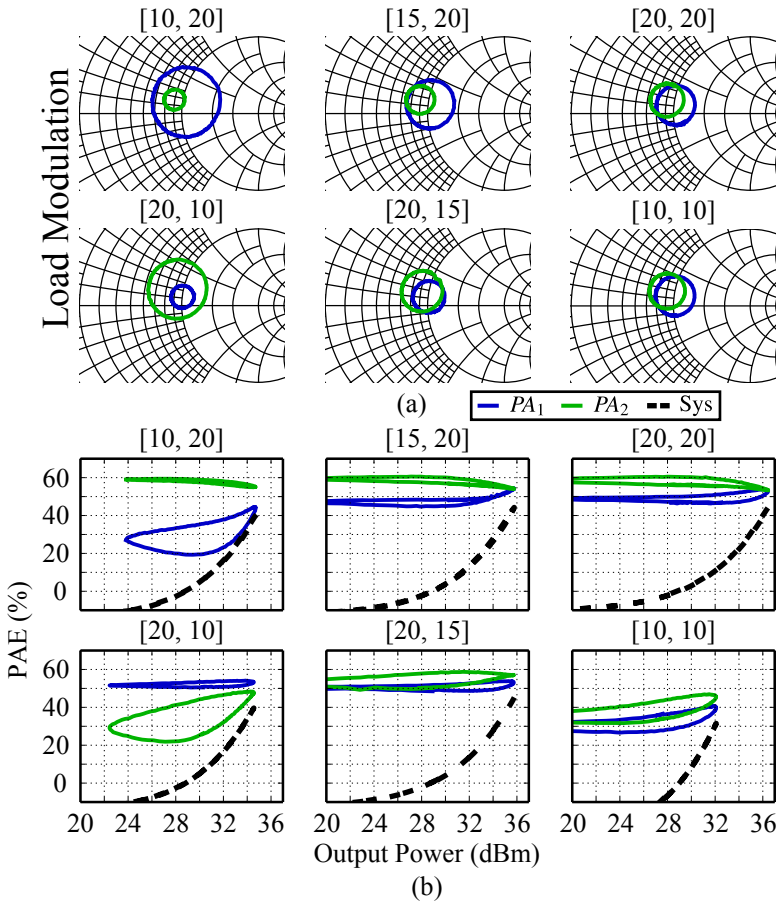
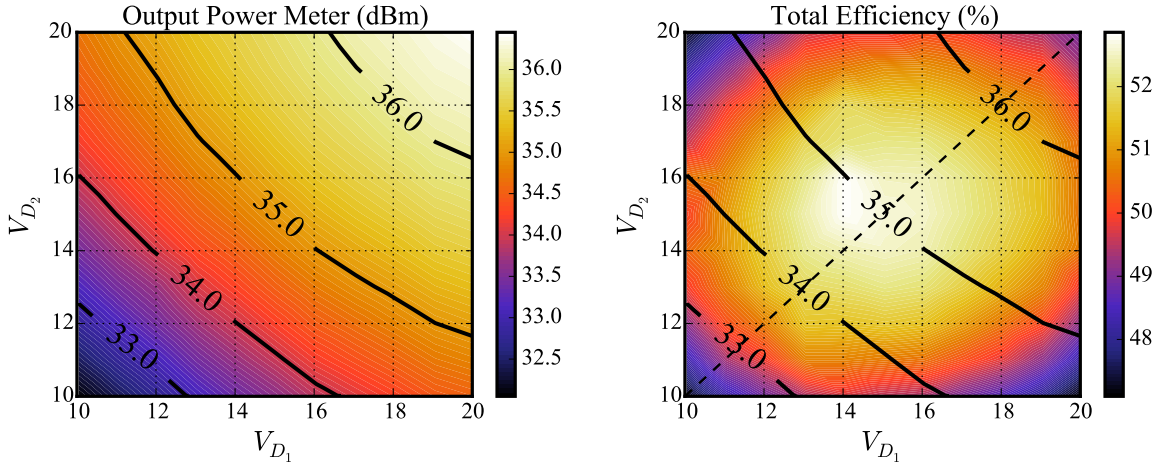


Figure 4.15: Measured (a) load modulation, and (b) internal PA and system PAE for the AMO PA with varying separation between supply levels $[V_{D_1}, V_{D_2}]$. Large supply separation shows significant load modulation, causing both internal PA and system efficiency degradation.

As previously stated, AMO PAs typically utilize only symmetric supply levels and combinations of adjacent levels, because the combining efficiency of an isolated combiner decreases as the difference between supply levels increases, leading to a negligible improvement in efficiency [104]. Further substantiation for this restriction is evident in Fig. 4.15, which shows the load modulation, internal PA efficiency, and system efficiency for the following supply voltage combinations: $[V_{D_1}, V_{D_2}]$ = [10 V, 20 V], [15 V, 20 V], [20 V, 20 V], [10 V, 10 V], [20 V, 15 V], and [20 V, 10 V]. As the internal PA output powers become imbalanced by large a difference in the asymmetric supply levels, the isolation in the combiner is insufficient to prevent substantial load modulation (Fig. 4.15a). Of course, a designer working with an AMO PA and isolated combiner would probably not suspect that load modulation is occurring within the PA. Fig. 4.15b shows that this amount of load modulation is enough to decrease the efficiency of one internal PA as well as the system.



(a) (b)

Figure 4.16: (a) Output power and (b) total efficiency for all combinations of drain voltages from 10 V to 20 V in 1 V steps with the dashed black line demonstrating supply level symmetry. For each output power, symmetric supplies maximizes efficiency.

Compared to the efficiencies shown for restricted levels in Fig. 4.11, the system efficiency for large supply imbalances is significantly decreased.

Further confirmation for the supply level restriction is established in Fig. 4.16, which exhibits output power and efficiency for all combinations of the drain voltages from 10 V to 20 V in 1 V steps. At each supply combination, the outphasing angle is chosen from a sweep for maximum efficiency. For each output power contour (solid black lines), the optimal total efficiency lies on the trajectory of symmetric supply levels (dashed black line). While the optimal continuous trajectory maintains balanced supply levels, AMO offers efficiency improvement over ML-LINC when implementing discrete supply levels through additional adjacent asymmetric level combinations.

4.3.3 Linearity Indicators

A comparison of linearity indicators, as described in subsection 2.4.3, is made between the ML-LINC and AMO prototypes. Table 4.2 compares the gain and phase imbalances as well as encoding distortion, which result for the same reasons as discussed in subsection 3.2.3. Both supply modulated LINC PAs show an encoding distortion similar to LINC and a slightly better (3°) maximum phase imbalance. ML-LINC

Table 4.2: Measured gain and phase imbalance in supply modulated LINC PAs

Architecture	Max Gain Imbalance (dB)	Max Phase Imbalance (°)	Max Encoding Distortion (°)
ML-LINC	1.21	17.75	-24.25
AMO	1.48	16.31	-26.4

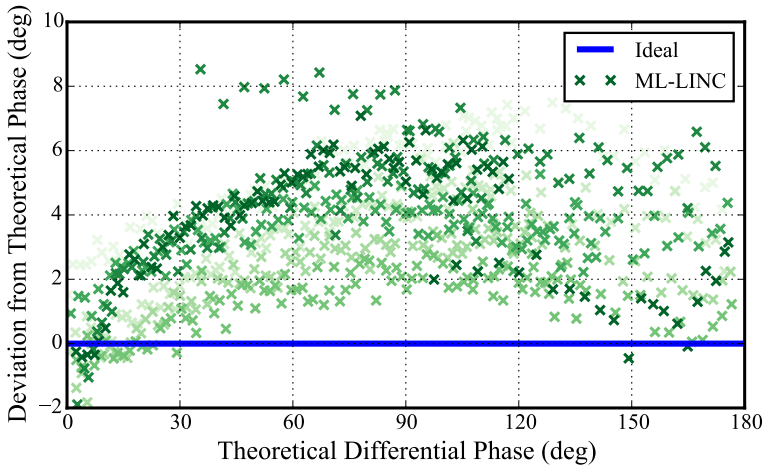


Figure 4.17: Measured differential phase deviation in ML-LINC, showing up to 8° deviation from ideal operation.

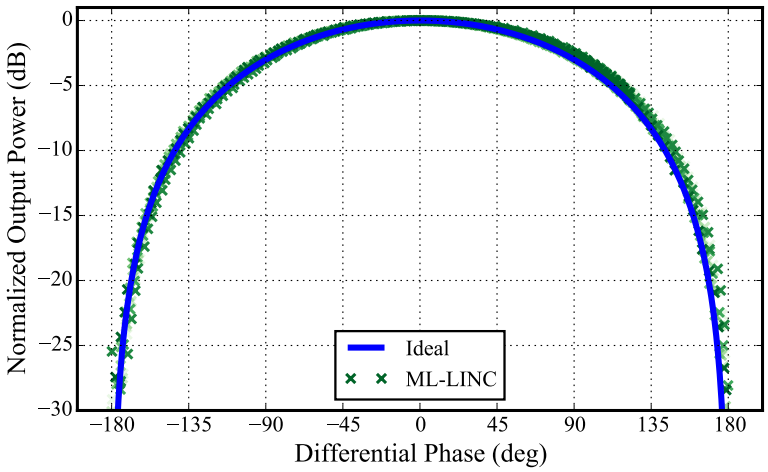


Figure 4.18: Measured output power with respect to differential phase in ML-LINC, showing negligible deviation.

has the same gain imbalance as LINC, while the slight asymmetry in AMO causes an approximate 0.2 dB degradation.

Even with symmetric, discrete supply modulation, the ML-LINC PA still demonstrates the same linear

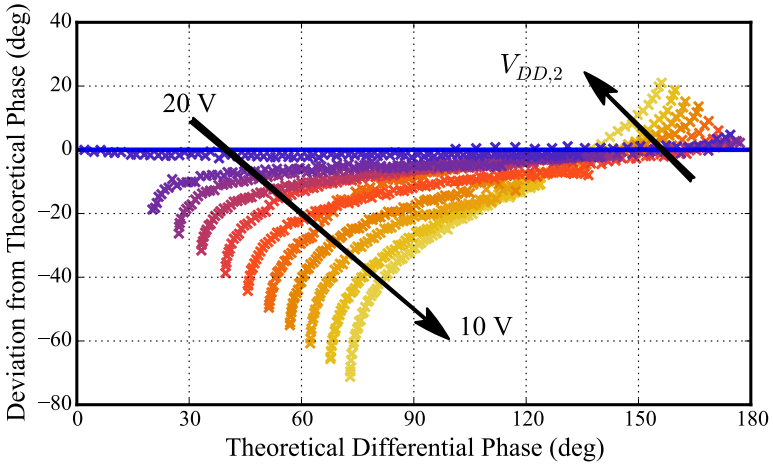


Figure 4.19: Measured differential phase deviation for the AMO PA. V_{D_1} is 20 V, and V_{D_2} is varied from 10 V to 20 V in 1 V steps. The phase deviation increases substantially with the difference between supply levels.

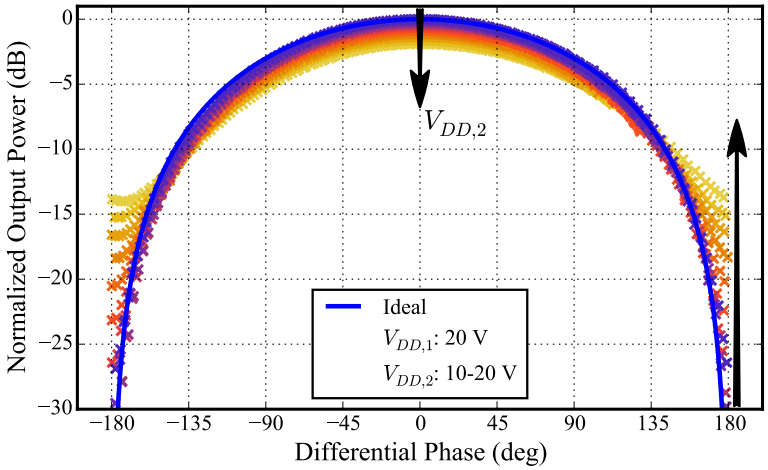


Figure 4.20: Measured output power with respect to differential phase for the AMO PA. V_{D_1} is 20 V, and V_{D_2} is varied from 10 V to 20 V in 1 V steps. As the supply level difference increases, significant output power distortion occurs.

behavior as in LINC in terms of the nonlinear phase transformation. In Fig. 4.17, ML-LINC attains the same maximum deviation of 8° found in the LINC PA, along with the negligible deviation from ideal operation in the output power in Fig. 4.18.

Interestingly, the AMO PA experiences increasingly nonlinear phase transformation as the difference in its supply levels increases. To exhibit this behavior, one supply is set to 20 V while the other (V_{D_2}) is varied from 10 to 20 V in 2 V steps. As V_{D_2} decreases, the deviation from linear phase relationship increases to

75° in Fig. 4.19. In Fig. 4.20, not only does the peak power decrease, but the minimum power increases by upwards of 20 dB. Both of these effects would significantly degrade the linearizability of the system if those combinations of supply levels were used. The linearity degradation provides another reason to utilize only symmetric and adjacent combinations of supply levels.

4.4 Conclusion

The concept of the supply modulated LINC PA architecture was described theoretically, detailing the optimal split between outphasing angle and supply level. The internal PA performance and load modulation measurement setup from Chapter 3 was extended through static variation in the drain voltage of each internal PA. Symmetric (ML-LINC) and asymmetric (AMO) supply modulation led to ΔP_{out} improvements beyond the LINC PA of 2.15 dB and 3.95 dB respectively, as well as improvements beyond the Chireix outphasing PA of 1.16 dB and 2.96 dB respectively. Compared to the LINC PA, the ML-LINC PA was not found to degrade load modulation or linearity performance, while increasing efficiency. However, when the supply levels in AMO were separated by 5 V or more, significant load modulation and linearity issues arose. AMO operated optimally in terms of efficiency, load modulation, and linearity when the levels were restricted to be symmetric or adjacent combinations. Original contributions in this chapter include the following:

- The extension of the internal PA performance and load modulation measurement setup to supply modulated LINC [94], demonstrating the efficiency improvement caused by minimized both RF and DC power dissipation.
- The measurement of load modulation internal to the supply modulated LINC PA [94], which became significant when the asymmetric supplies were separated by several volts, and led to decreased internal PA efficiency.

Chapter 5

Multi-Level Chireix Outphasing

Contents

The previous chapter highlighted the efficiency improvement obtained by incorporating discrete supply modulation with the LINC PA, making one wonder what could be achieved if it were incorporated with Chireix outphasing, which already has a higher efficiency performance, especially at power back-off. In this thesis, and for the first time in literature [94, 108], this concept is demonstrated and named multi-level Chireix outphasing (ML-CO). Fig. 5.1 shows the system architecture, featuring a non-isolated combiner at the output and a discrete supply modulator.

The purpose of the discrete supply modulator is the same as when incorporated with LINC, to provide coarse modulation of the internal PA output power. Effectively, this varies the amplitudes of the voltage sources in Fig. 2.2b from the Chireix outphasing theory in Section 2.1. Two different amplitudes are shown at the output of the internal PAs in the block diagram, while the differential phase modulation within the

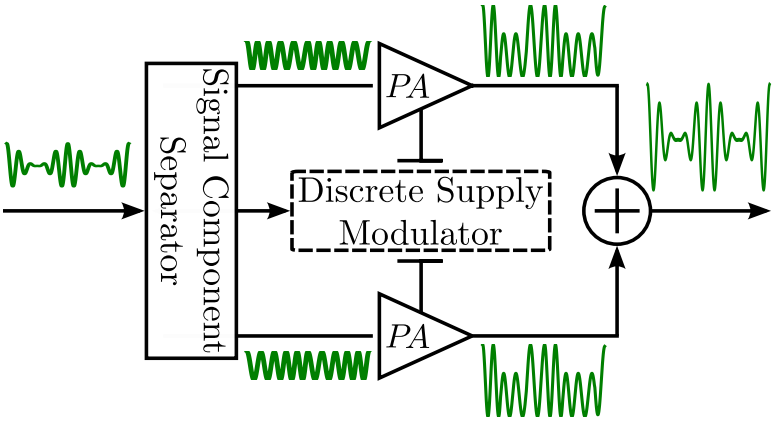


Figure 5.1: Block diagram of multi-level Chireix outphasing.

signal provides fine output amplitude control.

The inner workings of the ML-CO PA are investigated and discussed in this chapter. The theoretical performance is described in Section 5.1, before returning to the internal PA performance and load modulation measurement setup which is extended to include this new architecture in Section 5.2. Finally, a ML-CO PA implemented on a GaN MMIC at X-band is presented in Section 5.3.

5.1 Multi-Level Chireix Outphasing Theory

The operation of the efficiency improvement in ML-CO is very similar to ML-LINC, in that the discrete supply modulation theoretically replicates the efficiency curve of Chireix outphasing with a given reactive compensation for each supply level, as shown in Fig. 5.2. The four normalized supply levels (0.355, 0.5, 0.708, and 1.0 V) are chosen to reach a maximum output power at 9, 6, 3, and 0 dB back-off. The normalized supply voltages can be found by normalizing the Chireix outphasing output power in (2.14) to 1 W at its peak (θ=90°, $A_0 = A_{max} = 1\,V$), yielding a load resistance of 4 Ω. At peak power for any supply level, A_n, (2.14) now simplifies to:

$$P_{out,n} = \left(\frac{A_n}{A_{max}}\right)^2 \tag{5.1}$$

Converting to decibels, and solving for the normalized supply level:

$$\left(\frac{A_n}{A_{max}}\right) = 10^{P_{out,n}/20} \tag{5.2}$$

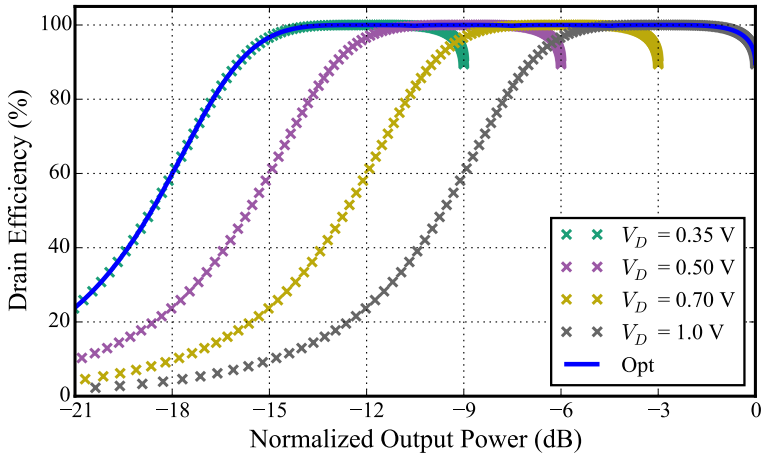


Figure 5.2: Theoretical efficiency of the ideal, four level ML-CO PA, demonstrating improvement for the optimal trajectory. The normalized supply levels of 0.355, 0.5, 0.708, and 1.0 V set the maximum output powers at 9, 6, 3, and 0 dB back-off.

In this example, the compensation susceptance is chosen to peak the efficiency at 3 dB back-off. From (2.27), the corresponding outphasing angle is found to be 45°, and the product $R_L B_C$ is found to be 1.0 from (2.28). Of course, the choice to peak efficiency at 3 dB is arbitrary, and four levels would not be necessary if the peak was moved to a lower normalized output power.

As with ML-LINC, multiple combinations of outphasing angle and supply level yield a given output power. The optimal solution minimizes the supply level. In the case of ML-CO, the outphasing angle may not be minimized, due to overlapping between the efficiency curves of adjacent supply levels. In this example, at peak power for a given supply (other than the highest), the efficiency of the next higher supply is better. This means that the range of outphasing angle is not condensed at one extreme, 0° or 90°, but rather somewhere in the middle of the range, as shown in Fig. 5.3. The compression of outphasing angle is completely dependent upon the number and value of supply levels, as well as the compensation susceptance.

In any outphasing PA, to achieve both maximum and minimum output power, the outphasing angle must reach the extremes, but the compression over a range of output power reduces the bandwidth required of the signal component separator. In ML-LINC and AMO, the reduction of outphasing angle directly decreased the RF power dissipated in the isolated combiner, but in ML-CO, the combiner is not isolated and therefore lossless.

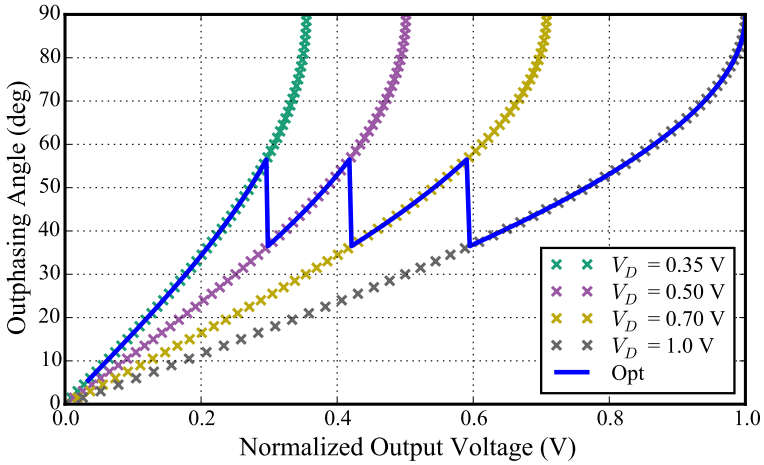


Figure 5.3: Theoretical outphasing angle for the ideal, four level ML-CO PA. Normalized supply voltages are 0.355, 0.5, 0.708, and 1.0 V.

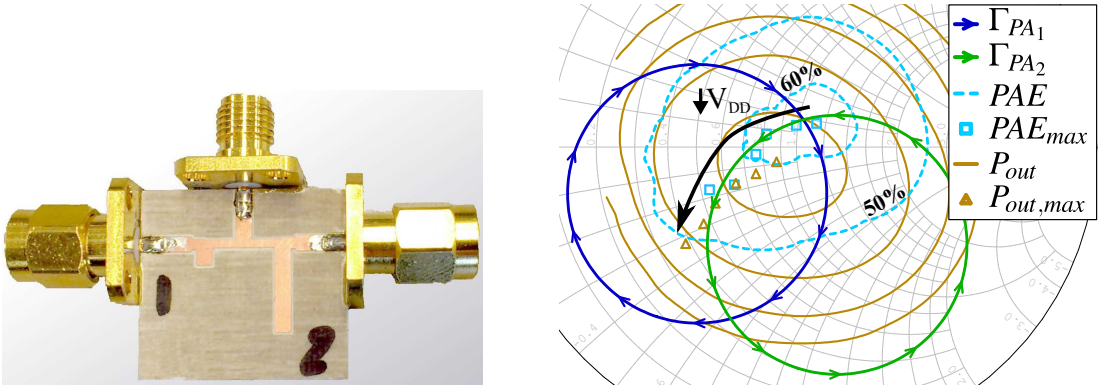
5.2 Internal PA Performance and Load Modulation Measurements

The internal PA and load modulation measurements presented in this section are based on the setup in Section 2.4. To characterize the ML-CO PA with discrete supply modulation, the drain voltage power supply is swept statically, and for each level a full phase sweep is performed. The initial calibration is not affected by operating the internal PAs at varying supply levels.

5.2.1 ML-CO Combiner Design

A new Chireix combiner must be designed for ML-CO operation. As described in detail for Chireix outphasing in Section 2.3, the combiner includes the bi-directional couplers and all transitions from the MMICs. The combiner must be designed at the same reference plane at which the MMIC PA is characterized. As described in subsection 2.2.3, the internal MMIC PA is characterized by load-pull measurements at the MMIC bond wire plane for drain voltages from 10 to 20 V in 2 V steps.

The load-pull contours are compiled in Fig. 5.4b to aid the design of the new combiner. The PAE contours for all supply voltages are combined into regions of greater than 50% and 60%, so that an impedance inside this region can achieve at least 50% or 60% PAE at one of the measured drain voltages. Of course, adding supply modulation increases the size of these two regions compared to a single voltage. Using (2.66) and



(a) (b)

Figure 5.4: (a) Photograph of Chireix combiner designed for ML-LINC measurements at 10.1 GHz and fabricated on 30 mil Ro4350B substrate. (b) Measured load-pull contours at drain voltages of 10, 12, 14, 16, 18, and 20 V. Output power contours are traced from 29 to 34 dBm (with 1 dB step) for a 20 V supply to aid output power balancing. PAE contours for all voltages are combined into regions designating PAE > 50% and 60%, showing expansion of high efficiency impedances. The predicted load modulation follows the movement of the PAE and output power maxima with drain voltage. Smith chart is normalized to 50 Ω.

(2.67), the predicted load modulation for the combiner is overlaid on the compiled, measured load-pull contours. Notice that the peak PAE and output power impedances follow a somewhat linear trajectory toward the edge of the Smith chart with decreasing drain voltage. This combiner is designed to follow that trajectory, by intersecting the circles at the peak PAE load for a 20 V drain supply, and following the peaks while maintaining output power balance. The output power contours are shown only for 20 V, but balancing the output power is difficult across various supply levels as the line of symmetry shifts.

The combiner shown in Fig. 5.4a is fabricated on 30 mil Rogers 4350B substrate. Looking at the measured load modulation circles, it is clear that the overlapping section does not exactly follow the trajectory of the peak PAE and output power, showing a slight counterclockwise rotation. This leads to distortion in the load modulation measurement.

As the drain voltage is varied, the load-pull contours of the internal PAs change. If the load modulation is power balanced for all supply levels, then the circles remain unchanged. In that case, the interaction between the changing load-pull contours and the constant load modulation circles would cause a replication of the hysteresis-like efficiency of Chireix outphasing, except each replication would have a different shape due to the changing interaction between the internal PAs and combiner. In reality, the load modulation circles are

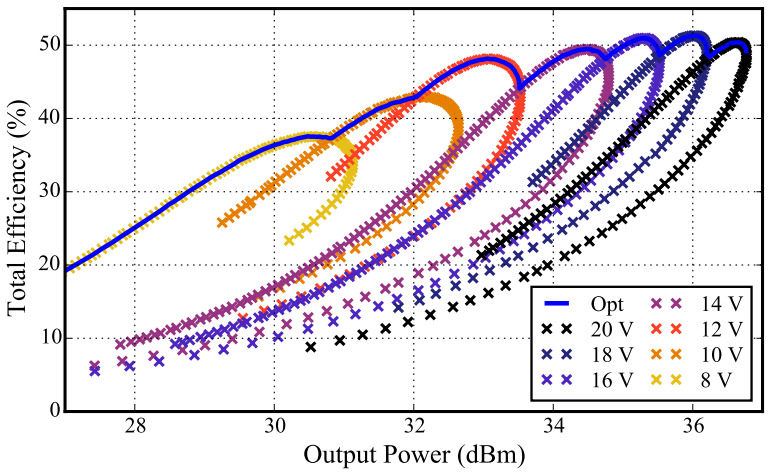


Figure 5.5: Measured system total efficiency of ML-CO PA for swept differential phase for drain voltages from 8 to 20 V in 2 V steps. Optimal operation, selected for peak total efficiency at each output power, takes advantage of load modulation hysteresis to maintain high efficiency.

not power balanced for all supply levels. Each drain voltage varies the load-pull contours and subsequently distorts the load modulation circles, so the operation is not as simple.

5.2.2 Measurement Results

The ML-CO system total efficiency is obtained for differential phase sweeps at drain voltages from 8 to 20 V in 2 V steps, and shown in Fig. 5.5. Each trace of different color corresponds to a unique drain voltage. The drain voltages are swept symmetrically, since independent variation in the supplies would force imbalances in the load modulation. The optimal operating points are chosen for peak total efficiency at a each output power.

The width, peak, slope, and shape of the total efficiency varies with supply voltage. At lower drain voltages, the curves widen, which improves the performance and reduces the number of discrete levels required to maintain high efficiency. The measured load modulation in Fig. 5.6 explains the advantageous widening in the efficiency. The optimal phase trajectory starts at the peak output power load and moves toward the peak efficiency load. At high supply voltages, both peak loads occur near the center of the Smith chart, and the optimal trajectory moves toward the edge. However, when the supply is 12 V, a reversal in the optimal trajectory occurs. The peak output power is located near the bottom load modulation intersection,

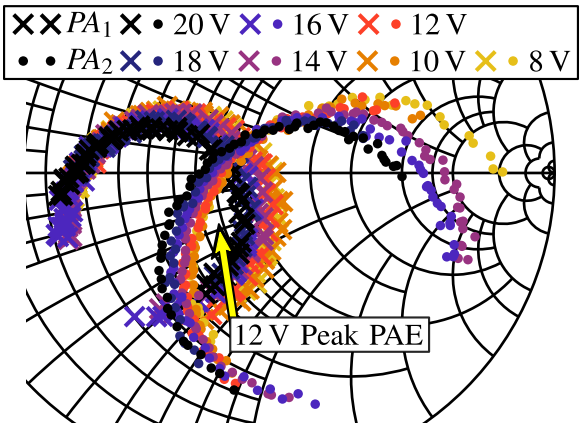


Figure 5.6: Measured internal load modulation in the ML-CO PA. Imbalance in impedance loci radii exposes the difficulty in maintaining internal PA P_{out} balance, but is mitigated through reduced differential phase requirements and balanced supply levels.

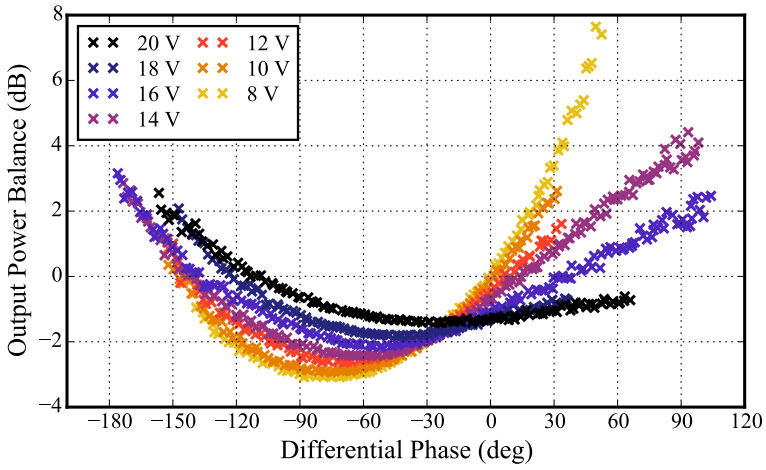


Figure 5.7: Measured power imbalance at the output of the internal PAs, demonstrating a the effects of imbalanced loading conditions which worsen with reduced supply voltage.

while the peak efficiency is in between the intersections. Now the upward phase trajectory remains in the high efficiency region for a larger range of outphasing angles and output power. The separation of the peak efficiency and output power loads at lower supply levels aids in the widening of the efficiency curve.

The load modulation also demonstrates the difficulty in maintaining internal PA output power balance over several supply levels, which rises up to nearly 8 dB with an 8 V supply voltage in Fig. 5.7. During this measurement sweep, the input power balance is maintained to within ± 0.8 dB. The effect is also evident in the imbalanced radii of the load modulation circles. This issue may lead to instability, but the ML-CO mitigates the risk by reducing the range of required differential phase, and thus the region of actual load

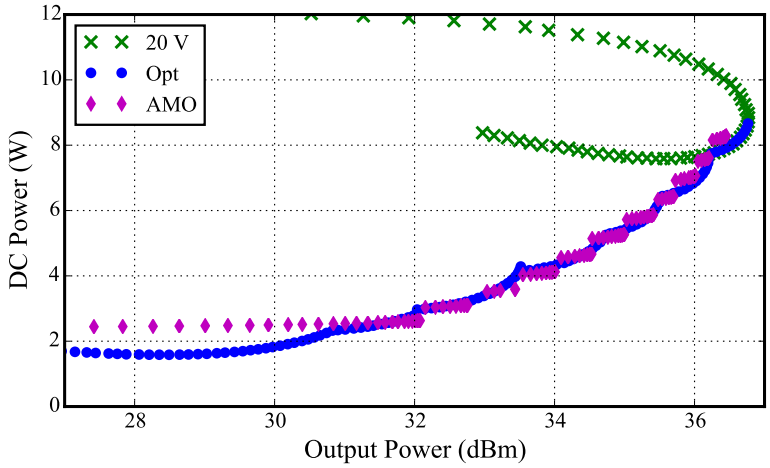


Figure 5.8: Comparison of measured DC power consumption between constant 20 V, optimal AMO, and optimal ML-CO operation, demonstrating commensurate power savings between ML-CO and AMO.

modulation. Restriction to symmetrically varying supplies helps as well. Attempting to build this PA with separate internal PA MMICs and off-chip combining is the worst case scenario for imbalances and load modulation distortion. Implementing the entire PA on a single MMIC, as done in Section 5.3, reduces the risk by ensuring better internal PA balance.

Unlike the supply modulated LINC PAs, the ML-CO PA is lossless in the sense that no power is dissipated in the combiner to provide isolation. Therefore, the only mechanism improving performance, aside from reactively compensated load modulation, is the reduction of DC power consumption with supply level. Fig. 5.8 demonstrates the DC power consumption of optimal ML-CO operation is comparable with that of the AMO PA, showing a reduction of 8 W compared to 20 V operation at 30 dBm (6.8 dB back-off). In Fig. 5.9 the required differential phase is decreased for optimal ML-CO operation to -80° < φ < -3° down to 29 dBm output power (7.8 dB back-off), a 75° improvement over 20 V operation.

A comparison of the optimal efficiency curve between ML-LINC, AMO, and ML-CO is shown in Fig. 5.10. ML-CO performs similarly to the others at peak power, and surpasses them below 31.5 dBm, more than 5 dB back-off. Table 5.1 summarizes the system performances, showing a further increase in ΔP_{out} of 0.35 dB beyond the AMO PA, but a 30 dB decrease in dynamic range. Part of this reduction results from the sweeps not completing the full load modulation circles near the edge of the Smith chart, while another major factor is the imbalance which distorts the circles away from the edge of the Smith chart. However, simulation

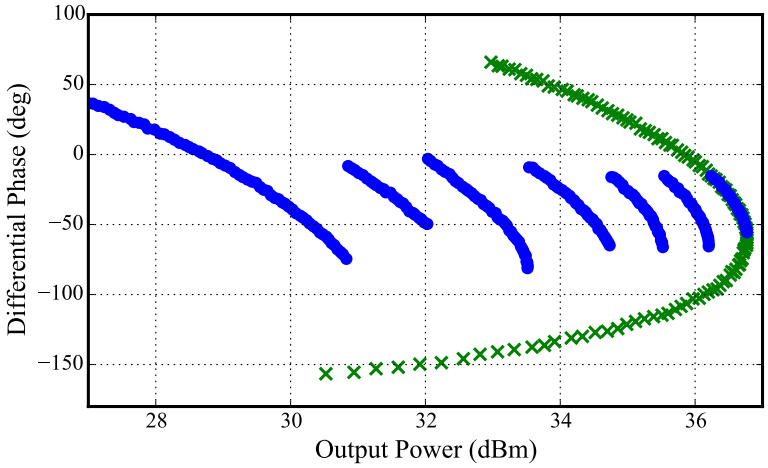


Figure 5.9: Comparison of measured differential phase between constant 20 V and optimal ML-CO operation, demonstrating a significant reduction. The optimal trajectory utilizes supply voltages from 8 V to 20 V in 2 V steps.

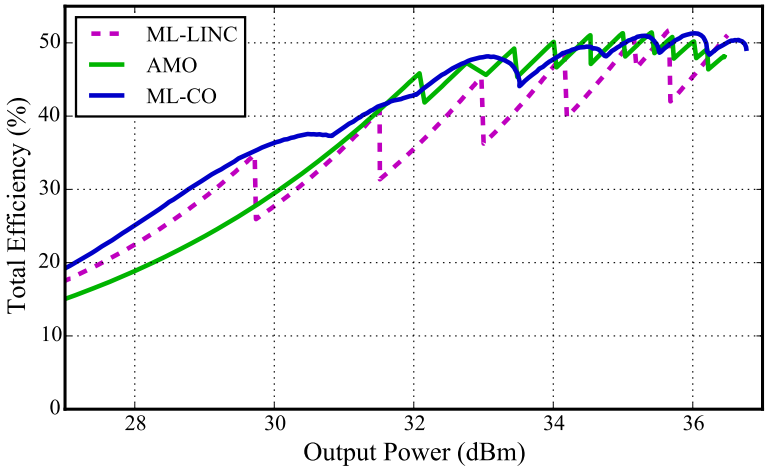


Figure 5.10: Comparison of efficiency for optimal ML-LINC, AMO, and ML-CO operation.

Table 5.1: Measured system performance of supply modulated outphasing PAs

Architecture	Peak P_{out} (dBm)	Peak η_{tot} (%)	ΔP_{out} (dB)	Dynamic Range (dB)
ML-LINC	36.5	51.7	3.1	39.5
AMO	36.5	52.5	4.9	41.1
ML-CO	36.8	51.3	5.25	10.5

confirms a dynamic range comparable to the supply modulated LINC PAs under full load modulation sweeps.

Table 5.2: Measured gain and phase imbalance in supply modulated outphasing PAs

Architecture	Max Gain Imbalance (dB)	Max Phase Imbalance (°)	Max Encoding Distortion (°)
ML-LINC	1.21	17.75	-24.25
AMO	1.48	16.31	-26.4
ML-CO	2.79	52.52	-103.2

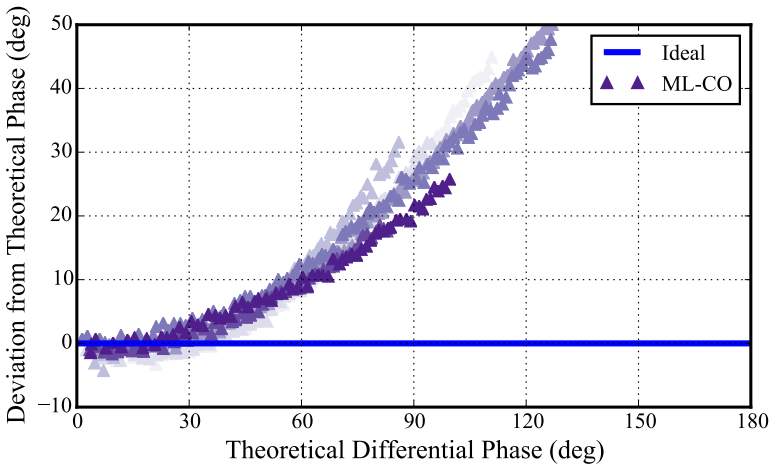


Figure 5.11: Measured differential phase deviation in ML-CO, showing up to 50° deviation from ideal operation. The shades of purple designate the supply voltage, the lightest and darkest corresponding to 10 V and 20 V, respectively.

5.2.3 Linearity Indicators

A comparison of linearity indicators, as described in subsection 2.4.3, is made between supply modulated LINC PAs and the ML-CO PA in Table 5.2. The ML-LINC and AMO PAs exhibit better gain imbalance by more than 1 dB and better phase imbalance by 35°. The ML-CO PA reaches the maximum measured encoding distortion at -103.2°, but this is simply an offset.

Variation of the supplies in ML-CO exacerbates the nonlinearity of Chireix outphasing, which is discussed in detail in subsection 2.4.3. In both nonlinear phase transformation measurements, the linearity indicator of the ML-CO PA is shown for each supply level in different shades of purple, with the lightest designating 10 V and the darkest designating 20 V. In Fig. 5.11, the ML-CO PA shows up to 50° of deviation from theoretical phase, and in Fig. 5.12, up to 7.5 dB of deviation in power is exhibited.

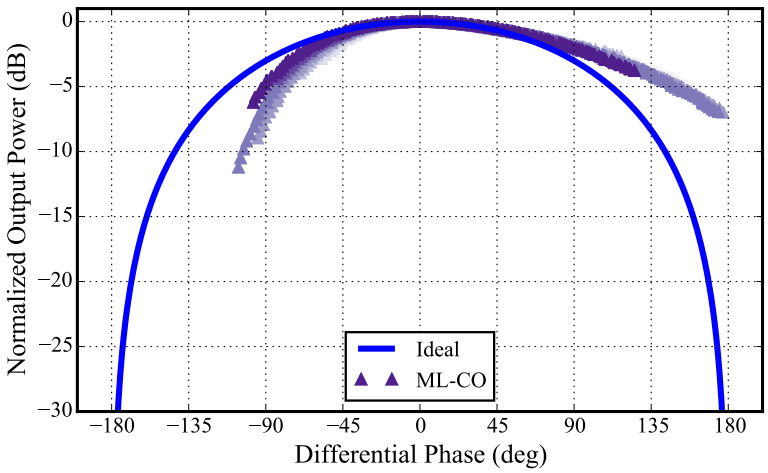


Figure 5.12: Measured output power with respect to differential phase in ML-CO, showing up to 7.5 dB deviation from ideal operation.

Compared to the linearity indicators of supply modulated LINC in subsection 4.3.3, linearizing the ML-CO PA is much more difficult. While these measurements show significant linearity concerns, adequate linearization has been performed for Chireix outphasing in [48,91] and with supply modulated LINC in [100]. Nevertheless, these measurements provide insight into the linearizability of each architecture.

5.2.4 Prediction of Load Modulation Distortion

The distortion of the measured load modulation in Fig. 5.6 compared to the the predicted load modulation in Fig. 5.4b calls to question the validity and usefulness the small-signal combiner analysis and resulting design equations, (2.66) and (2.67). The major discrepancy came from ignoring the power imbalance, implemented in the equations by the variable x, when predicting the load modulation. As illustrated in Fig. 5.7, the induced power imbalances are varying and nonzero. Furthermore, in ML-CO, the output power balance varies with supply voltage. Therefore, entering a single value for x will not accurately predict load modulation.

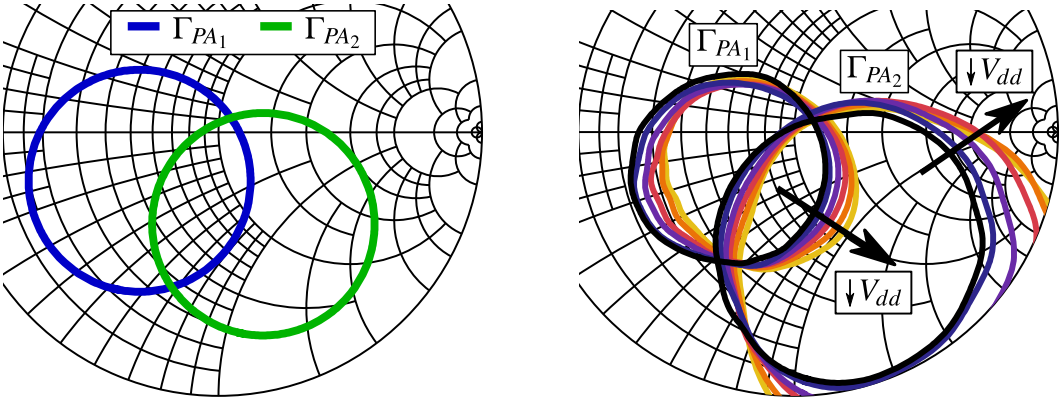
In order to aid in the combiner design for these cases, a measurement based simulation method is developed. It uses feedback to accurately predict load modulation with power imbalance. Because each internal PA is characterized, this method will predict the imbalances caused by the differences in the two chips.

The procedure is as follows:

- Characterize each internal PA with load-pull measurement at all desired supply levels.
- Interpolate load-pull measurements.
- Simulate or measure S-parameters of combiner at the same frequency and reference plane as internal PA characterizations.
- Calculate initial values of Γ_{PA_1} and Γ_{PA_2} from (2.66) and (2.67), as seen in Fig. 5.13a.
- From load-pull interpolation, find output power for each internal PA at initial values of Γ_{PA_1} and Γ_{PA_2}.
- Calculate power imbalance, the difference in output power between the internal PAs.
- Re-calculate values of Γ_{PA_1} and Γ_{PA_2} from (2.66) and (2.67), inserting the array of calculated power imbalances as the variable x, as seen in Fig. 5.13b.

The simulation is set up in Keysight's Advanced Design System (ADS) software. The measured load-pull characterizations are stored in CITI formatted files. The Data Access Component is used in ADS to interpolate the load-pull data. Although the data adheres to a polar grid better, a rectangular (Cartesian coordinates) interpolation is utilized due to phase discontinuities in polar interpolation. It is important to recognize that the interpolation of data near the edge of the measured range of impedances will not be reliable or accurate, due to the abrupt end of data. Therefore, the load modulation predicted at the edge of the Smith chart should be considered cautiously. A dummy DC simulation is used to force ADS to perform the calculation of the initial (balanced) load modulation circles, extract corresponding output powers from the interpolated load-pull characterization, and re-calculate the unbalanced load modulation circles. Note that an additional iteration in this feedback calculation does not improve the accuracy of the prediction, which indicates that the steady state solution does not completely balance output power.

The procedure is performed for the measured combiner used in ML-CO measurements. The newly predicted load modulation in Fig. 5.13b shows the same expansion of the Γ_{PA_2} and shrinking of the Γ_{PA_1} circles, as well as the trend of the distortion being exacerbated at low supply voltages as found in measurement.



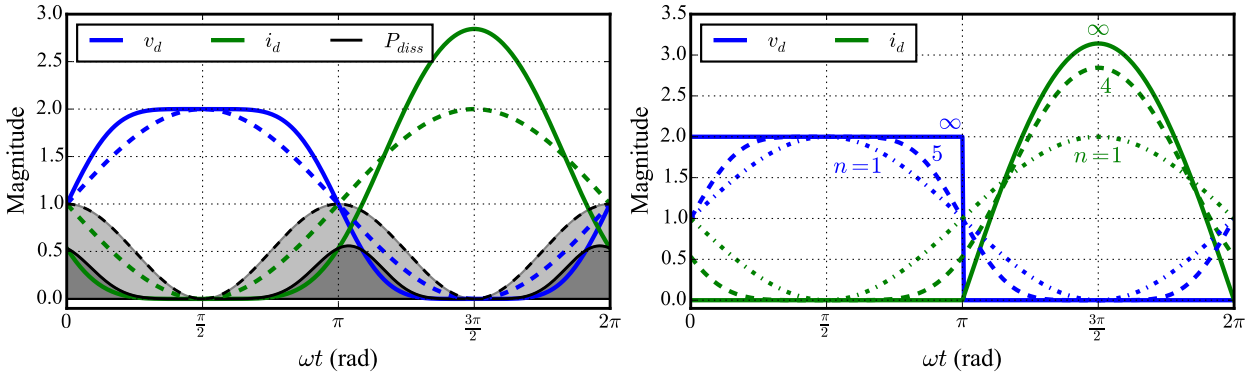
(a) (b)

Figure 5.13: (a) Simulation predicting the load modulation of a measured combiner based on (2.66) and (2.67) with x=1 and internal PAs are biased at 20 V. (b) Simulated predicted load modulation using feedback to account for internal PA output power imbalance at supply levels between 10 V and 20 V in 2 V steps.

The predicted load modulation using feedback compares extremely well qualitatively to the measurement in Fig. 5.6. Note that the load-pull characterization had a limited range of reflection coefficient magnitude, so the load modulation at the edge of the Smith chart will not be accurate due to interpolation error.

5.3 Multi-Level Chireix Outphasing GaN MMIC PA

The Chireix outphasing measurements in subsection 2.4.2 at 10.1 GHz as well as 5 GHz [51], demonstrate that the second peak in efficiency at low output power has not been realized at high frequencies. The efficiency load-pull contours rapidly degrade as compared to the output power contours, preventing high efficiency operation at low output power. This may be due to the class of operation of the internal PAs as well as parasitics at these frequencies. In this section, the same effect is present for a fully integrated ML-CO GaN MMIC PA with high-efficiency class-F internal PAs. In this case, the integration reduces parasitics, while class-F PAs should operate highly efficiently under load modulation [38]. The addition of discrete supply modulation is found to improve the efficiency for a high PAR signal.



(a) (b)

Figure 5.14: (a) Comparison of intrinsic drain waveforms and dissipated power between sinusoidal class-A operation (dashed, light gray) and class-F with five harmonic terminations (solid, dark gray). (b) Evolution of intrinsic drain voltage and current waveforms for increasing number of class-F terminated harmonics.

5.3.1 ML-CO MMIC Design

5.3.1a Output Harmonic Terminations

To achieve high efficiency, the internal PAs are designed to operate in class-F [109]. In a harmonically terminated power amplifier, such as class-F, the transistor is biased near pinch-off and driven hard to generate harmonic power. Then, the output matching network synthesizes an infinite (open circuit) or zero (short circuit) impedance at harmonic frequencies to shape the voltage and current waveforms at the intrinsic drain of the transistor such that less power is dissipated, as demonstrated in Fig. 5.14a. In that case, theoretically, no harmonic power is generated by the transistor. In the class-F PA, the OMN presents a short circuit to even harmonics and an open circuit to odd harmonics, squaring the voltage waveform and peaking the current waveform, as shown for an increasing number of harmonic terminations in Fig. 5.14b. Terminating an infinite number of harmonics yields 100% efficiency for class-F operation [15].

In practice, a transistor will not generate harmonic power up to an infinite number of harmonics, so only a few harmonics can be usefully terminated. Even if only the first three harmonics are terminated, a peak efficiency of 75% is achievable, while five terminations will yield 83% efficiency [15]. A general Fourier analysis of harmonically terminated PA operation is available in [110], while an in-depth description and analysis of class-F operation is presented in [111]. Of course, [12] and [72] also provide ample information

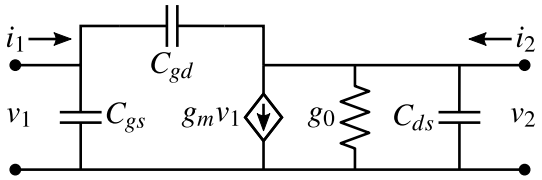


Figure 5.15: Simplified small signal model for capacitance extraction using Y-parameter analysis.

regarding high-efficiency PA classes, while [112] compares the performance of class-E, class-C, and class-F PAs with a finite number of harmonics.

Because the harmonic terminations must synthesize an impedance at the intrinsic drain, and the available transistor model does not have any internal accessibility, the output parasitics must be estimated and de-embedded. For a transistor in this GaN MMIC process, the parasitics are well approximated by the output capacitance, as confirmed in previous design experience [113, 114]. The output capacitance is extracted from the nonlinear model using the method in [115] based on the simplified field-effect transistor (FET) shown in Fig. 5.15. The small-signal scattering parameters are simulated at 10 MHz as a function of bias point and then converted to admittance parameters. The FET π-model capacitances are calculated using the following equations:

$$C_{gd} = -\frac{\mathrm{Im}\{Y_{12}\}}{2\pi f} \tag{5.3}$$

$$C_{ds} = \frac{\mathrm{Im}\{Y_{22}\}}{2\pi f} - C_{gd} \tag{5.4}$$

$$C_{gs} = \frac{|Y_{11} + Y_{12}|^2}{2\pi f \times \mathrm{Im}\{Y_{11} + Y_{12}\}} \tag{5.5}$$

where the gate is port 1, the drain is port 2, and the source is grounded. The output capacitance is then found by considering the combination of physical capacitances:

$$C_{out} = C_{ds} + C_{gd} || C_{gs} \tag{5.6}$$

At pinch-off (I_{dq}=3 mA), the output capacitance reaches a steady value of 0.332 pF, as shown in Fig. 5.16. This phenomenon is helpful in high-efficiency PA design, because those PA classes are most often biased at pinch-off. Furthermore, the value of the output capacitance greatly affects the sensitivity of the phase of harmonic terminations, making its estimation critical. Fortunately, GaN has a quite linear output capacitance,

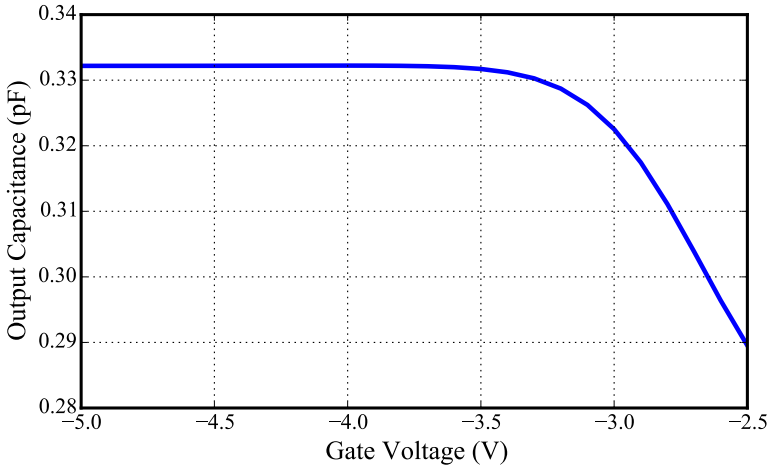


Figure 5.16: Extracted output capacitance of a 10×100µm pHEMT in Qorvo's 0.15 µm GaN process as a function of bias voltage.

and the value is further reduced in the MMIC process. The output capacitance is absorbed into the output matching network to shift the design reference plane to the intrinsic drain.

Typically, harmonic terminations are implemented in descending order, with the highest located closes to the transistor [116], in order to minimize the losses at higher frequency so as to attain maximum reflection. However, when the output capacitance is small enough such that it does not shift the phase of a harmonic termination appreciably, then it may be desirable to place a lower order harmonic termination closest to the transistor. For example, in this design, the bias tee is used to provide a second harmonic short circuit, as shown in Fig. 5.17. The fundamental frequency performance (input impedance and isolation) is sacrificed slightly to achieve a minimum impedance at the second harmonic of 1.88 Ω, as shown in Fig. 5.18, presenting a reflection coefficient with a magnitude of 0.94 and a phase of 178.1°. De-embedding the output capacitance only shifts the phase by 0.1°, therefore an acceptable short circuit is presented to the intrinsic drain at the second harmonic.

Now, how does the designer know if the output capacitance is "small enough" to not shift the phase of a termination "too far"? What is small enough and too far? Well, this is always dependent on the desired performance and application. The general harmonically terminated PA analysis in [110] characterizes the efficiency improvement for any second or third harmonic impedance. From this information, ranges in magnitude and phase of a harmonic termination are determined based on the desired performance. For

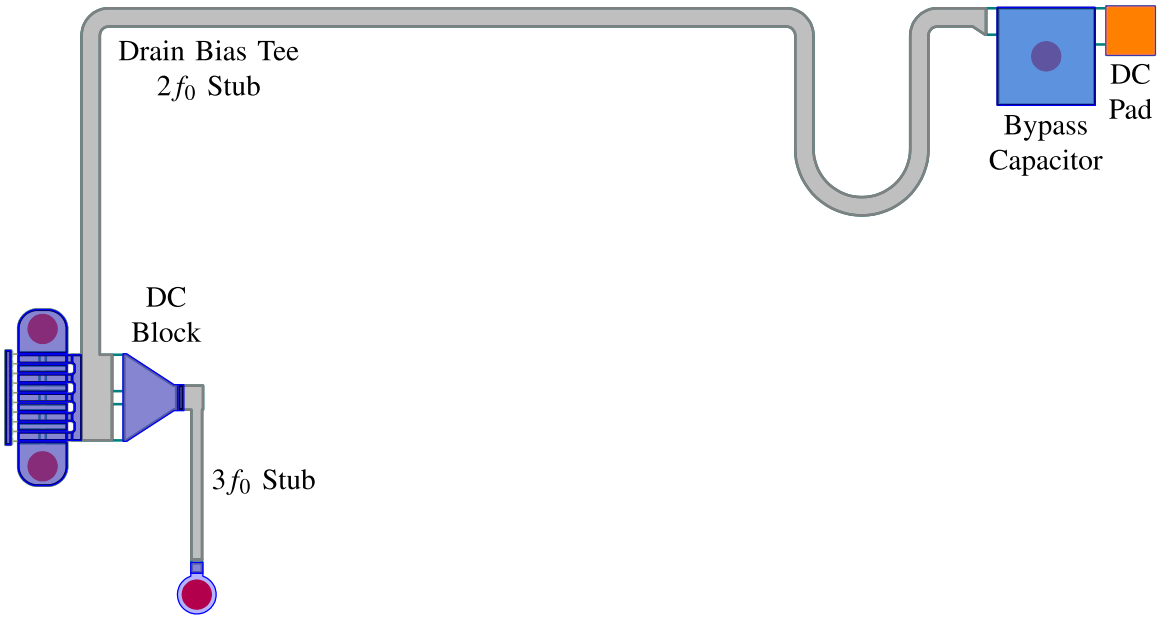


Figure 5.17: Layout of second and third harmonic terminations at the output of the transistor.

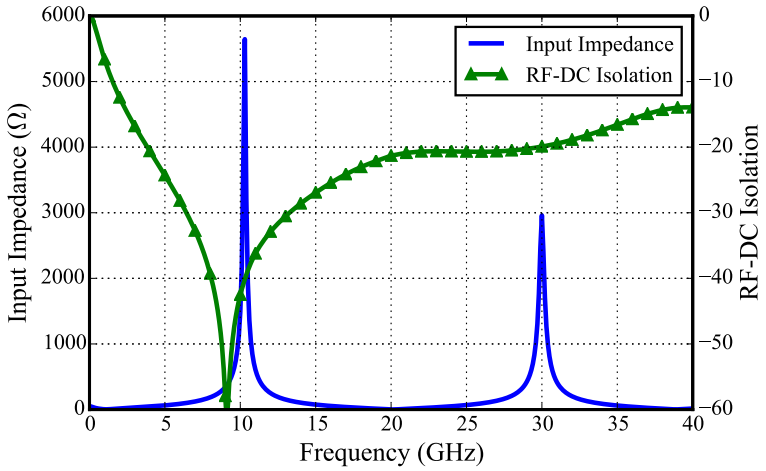


Figure 5.18: Simulation of gate bias tee, demonstrating high input impedance and isolation at f_0, low impedance at $2f_0$, and high impedance at $3f_0$.

example, a purely reactive second harmonic termination ($|\Gamma_L(2f_0)|$=1) improves efficiency beyond 70% within ±22.5° of a short or open circuit. Therefore, the harmonic termination does not need to be an exact open or short to provide a significant improvement.

Since the bias tee presents a high, shunt impedance at the third harmonic, the termination must be implemented with another element. This element must provide a resonance at the desired frequency so as to appear as a short circuit at its connection to the through path. At frequencies where lumped elements are

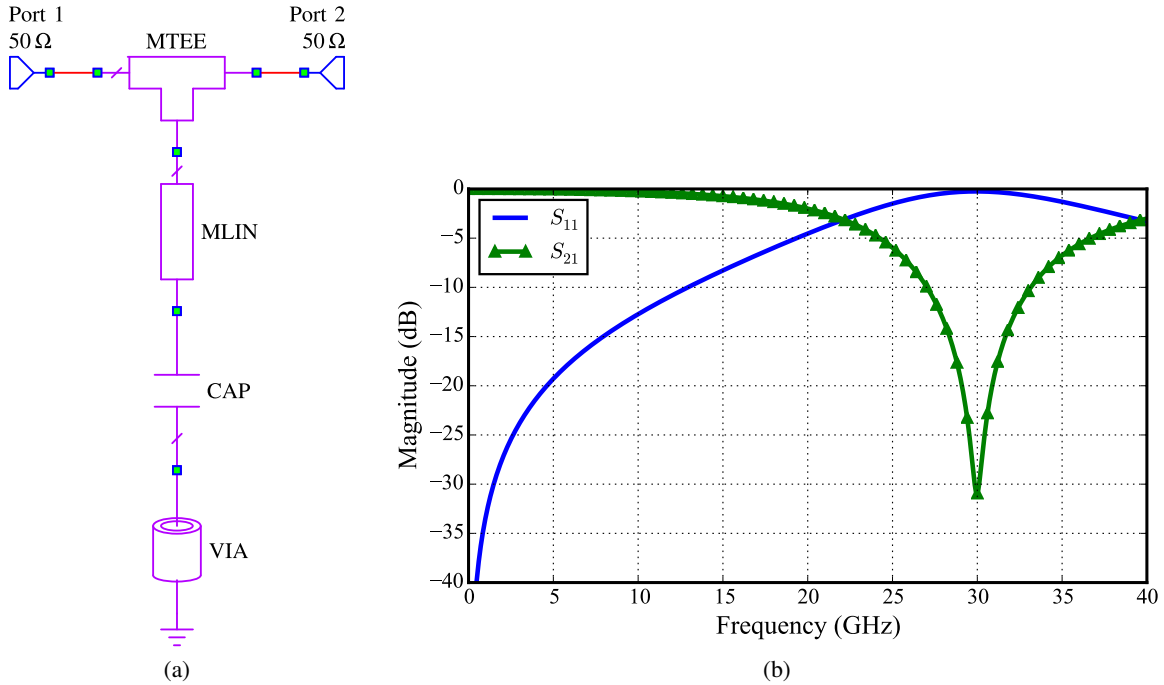


Figure 5.19: (a) Schematic of simulated third harmonic termination circuit. (b) Simulated S-parameters of third harmonic termination.

not appropriate, shunt stubs are used. In this design, the inductive portion of the resonator is approximated by a microstrip transmission line, as shown in Fig. 5.17. In general, any harmonic termination circuit can be simulated as in Fig. 5.19. To reflect power at a harmonic frequency, S_{21} should be minimized and S_{11} maximized. The insertion loss at the fundamental frequency is critical as well, and will depend on the quality factor of the resonator. In this case, the harmonic termination achieves a 31 dB resonance with 0.25 dB of insertion loss at the fundamental frequency.

Once the resonator has been designed, it must be properly phased with respect to the intrinsic drain. To do so, the harmonic terminations must be simulated at the intrinsic drain reference plane, as shown in Fig. 5.20. The electrical length of the transmission line (microstrip lines and taper) between the intrinsic drain and the third harmonic resonator must be determined to get zero phase at the intrinsic drain. The sensitivity of the harmonic termination phase, and subsequently the electrical length of the series transmission lines, increases with both output capacitance and frequency.

Fig. 5.21a demonstrates the desired second and third harmonic terminations presented at the intrinsic

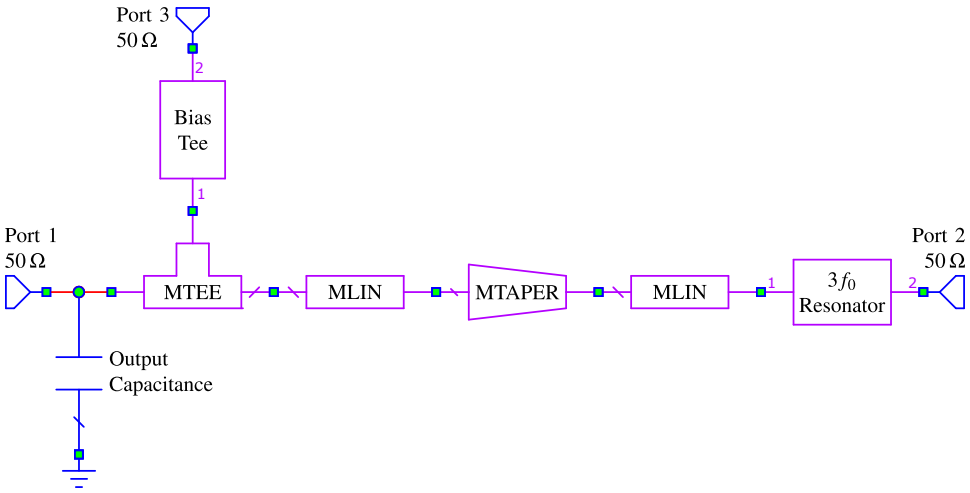
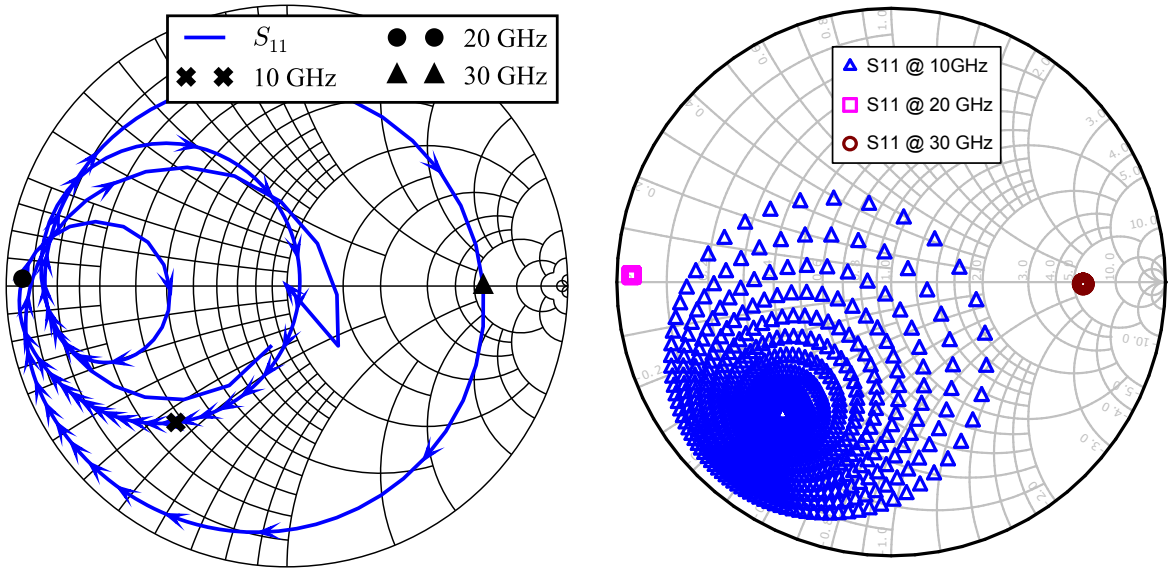


Figure 5.20: Schematic of simulated second and third harmonic terminations at the intrinsic drain.



(a) (b)

Figure 5.21: (a) Simulated impedance presented to the transistor at the intrinsic drain. (b) Simulated tuning range at harmonic frequencies, demonstrating tunability at the fundamental frequency, but not at harmonics, which are terminated.

drain by the designed OMN. The impedance synthesized at the second harmonic is $1.47 + j0.7\,\Omega$, and at the third harmonic is $282 + j1.54\,\Omega$. At this point in the design process, it is important to check and make sure that the loss in the harmonic terminations at the fundamental frequency has not restricted the ability to match for peak efficiency. A tuner element is placed at the output of the harmonic termination network and varied around the passive Smith chart at fundamental and harmonic frequencies, while the impedance is monitored

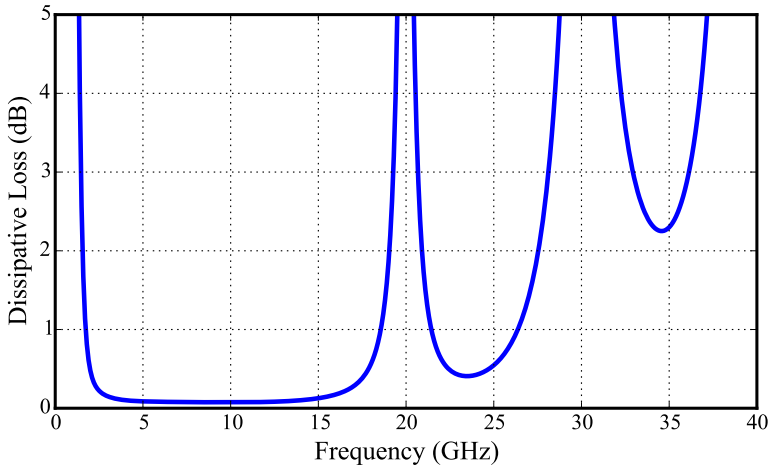


Figure 5.22: Dissipative loss in the harmonic termination network with 50 Ω load. Fundamental frequency matching is not performed yet.

at the intrinsic drain. Fig. 5.21b demonstrates the resulting tunability at the fundamental frequency. At harmonic frequencies, the implemented terminations fix the impedance presented at the intrinsic drain. The fundamental tuning range is enabled by the minimized dissipative loss of 0.067 dB in the harmonic terminations, demonstrated in Fig. 5.22. At the harmonics, the dissipative loss is very high, due to the implemented terminations.

5.3.1b Input Matching Network

Once the harmonic terminations are designed, an iterative source- and load-pull is performed to find the optimal fundamental impedances, resulting in an optimal reflection coefficient of $\Gamma_S(f_0) = 0.94\angle 159°$ for the gate in terms of power and gain. The designed IMN in Fig. 5.23 utilizes the bias line as a matching element, which is implemented as a shunt, grounded capacitor, providing 37 dB of RF-DC isolation. An additional shunt, capacitive stub along with series transmission lines provides enough elements to match at two frequencies. When these frequencies are placed in close proximity, more bandwidth is achieved, as shown in Fig. 5.24, where the match is better than 25 dB over 1.2 GHz of bandwidth centered at 10 GHz.

A resistor (de-Q) is placed in the bias line to protect against a resonance occurring between the bypass capacitor and any off-chip components, by reducing the quality factor. The DC blocking capacitor is integrated into the series transmission line. A 1 Ω shunt resistor is required with the bypass capacitor to

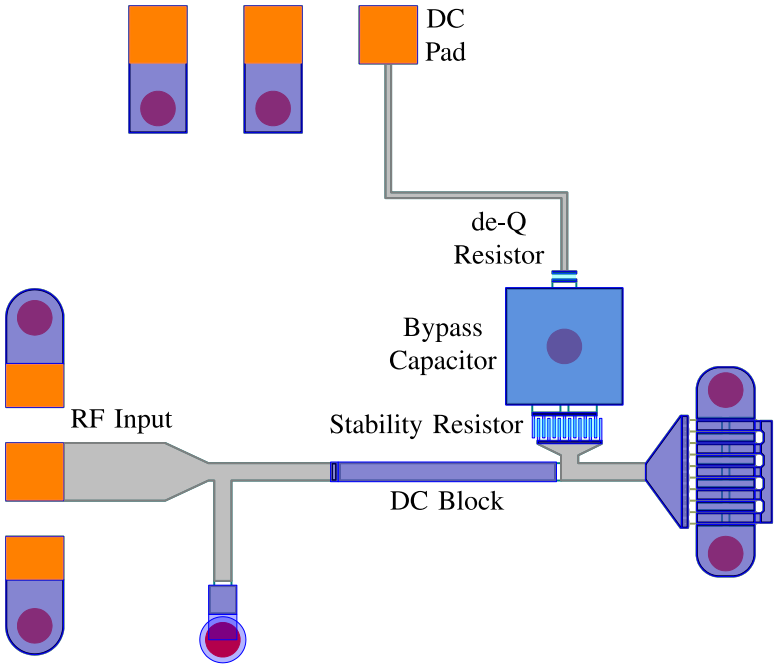


Figure 5.23: Layout of input matching network.

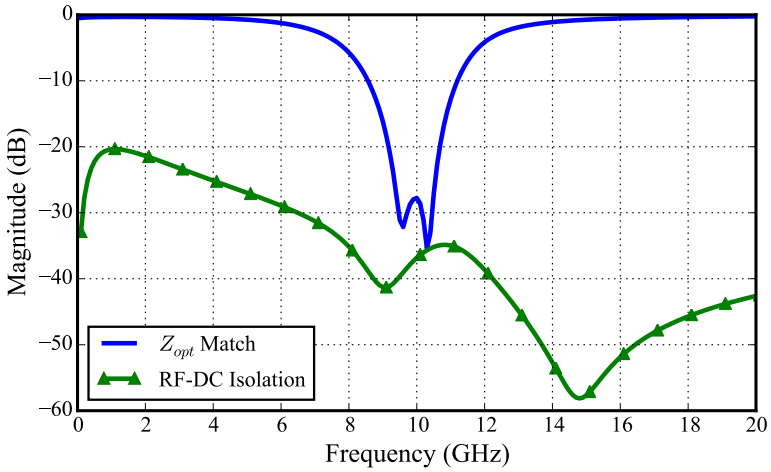


Figure 5.24: Simulation of input matching network match and RF-DC isolation.

provide stability. A regular tantalum nitride (TaN) resistor must be extremely wide relative to its length in order to obtain such a small resistance, posing design rule issues. In order to obtain a small resistance, an interdigital resistor is formed with a parallel combination of TaN resistors.

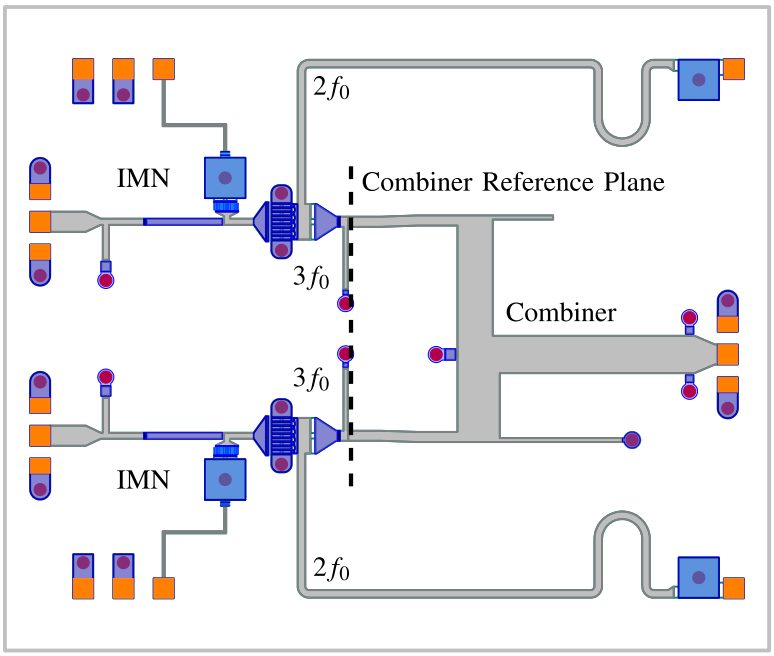


Figure 5.25: Layout of full ML-CO MMIC PA, defining the combiner and its design reference plane.

5.3.1c Combiner Design

To minimize loss, the combiner performs all fundamental matching directly, without matching to an intermediate impedance. Therefore, as discussed in the previous Chireix combiner designs, the internal PAs are characterized by load-pull simulation immediately after the harmonic terminations, labeled the combiner reference plane in Fig. 5.25. A general Chireix-type combiner with a tee-junction and compensation susceptances is tuned until the load modulation circles, labeled Γ_{PA_1} and Γ_{PA_2}, overlap the load-pull characterization for the desired performance, as shown in Fig. 5.26. It is critical to note that the final form of the combiner is completely dependent upon the reference plane at which it is designed, which must be where the internal PAs are characterized by load-pull.

In this design, the load modulation circles intersect at an outphasing angle near the peak efficiency impedance, then move toward the edge of the Smith chart while maintaining internal PA output power balance along the inner trajectory. With the combiner, the total dissipative loss in the output matching network at the fundamental frequency increases to 0.32 dB. For this calculation, the internal PA ports are connected as a single port and (2.35) is applied.

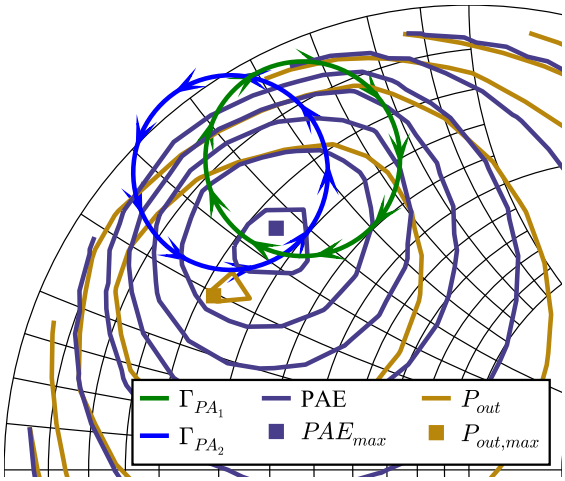


Figure 5.26: Load modulation of each PA, Γ_{PA_1} and Γ_{PA_2}, overlaid on the PAE and output power load-pull contours at the combiner reference plane. Smith chart is normalized to 50 Ω.

An implementation issue arises from Chireix outphasing theory, which assumes a differential load [19] that is not easily implemented at gigahertz frequencies in microstrip. In [64], quarter-wave transformers are used to convert each voltage source (internal PA) to a current source, so that the two outputs can be summed using a common grounded load [12]. However, two quarter-wave transmission lines are difficult to fit into the restricted area of a MMIC. Rather than using two quarter-wave transformers at the outputs of the internal PAs, one can be used after the combining node. To save even more space, a transmission line equivalent circuit can be used. Unfortunately, these equivalences are only readily available for the 90°, 180°, and 270° electrical lengths common to passive combining structures [117, 118]. In [64], the transmission lines are 90° because the combiner is referenced to the intrinsic drain, but in this design the reference plane has shifted and the electrical lengths are no longer 90°. Therefore, an equivalent circuit, shown in Fig. 5.27b, is derived for a variable length transmission line, shown in Fig. 5.27a. The derivation is also performed for other low- and high-pass equivalent networks in Appendix B. In this MMIC process, it is favorable to use a microstrip line rather than an inductor in the π-network to reduce loss.

First, the ABCD matrix of the TL-π network is found by cascading the ABCD matrices of its three elements (C_p-TL-C_p) as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C_p & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_s & jZ_s \sin\theta_s \\ jY_s \sin\theta_s & \cos\theta_s \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_p & 1 \end{bmatrix} \tag{5.7}$$

Figure 5.27: (a) Ideal transmission line. (b) Ideal TL-π equivalent network.

Resulting in:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta_s - \omega Z_s C_p \sin\theta_s & jZ_s \sin\theta_s \\ j\left[2\omega C_p \cos\theta_s + \sin\theta_s \left(\frac{1}{Z_s} - \omega^2 C_p^2 Z_s\right)\right] & \cos\theta_s - \omega Z_s C_p \sin\theta_s \end{bmatrix} \tag{5.8}$$

Equating this to the ABCD matrix of an ideal transmission line [119]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_0 \sin\theta \\ jY_0 \sin\theta & \cos\theta \end{bmatrix} \tag{5.9}$$

Two of the three unknown variables (C_p, Z_s, θ_s) can be solved for.

Solving for C_p and Z_s:

$$C_p = \frac{1}{Z_0} \frac{\cos\theta_s - \cos\theta}{\omega \sin\theta} \tag{5.10}$$

$$Z_s = Z_0 \frac{\sin\theta}{\sin\theta_s} \tag{5.11}$$

Solving for C_p and θ_s:

$$C_p = \frac{1}{Z_0} \frac{\sqrt{Z_s^2 - Z_0^2 \sin^2\theta} - Z_s \cos\theta}{\omega Z_s \sin\theta} \tag{5.12}$$

$$\theta_s = \arctan\left(\frac{Z_0 \sin\theta}{\sqrt{Z_s^2 - Z_0^2 \sin^2\theta}}\right) \tag{5.13}$$

Solving for Z_s and θ_s:

$$Z_s = \frac{Z_0 \sin\theta}{\sqrt{1 - \left(\omega C_p Z_0 \sin\theta + \cos\theta\right)^2}} \tag{5.14}$$

$$\theta_s = \arctan\left(\frac{\sqrt{1 - \left(\omega C_p Z_0 \sin\theta + \cos\theta\right)^2}}{\omega C_p Z_0 \sin\theta + \cos\theta}\right) \tag{5.15}$$

In this case, θ_s is chosen at the onset to be approximately 30°, since the physical length of the series TL is of utmost concern, leading to a shunt capacitance of approximately 0.5 pF. In choosing θ_s there is a

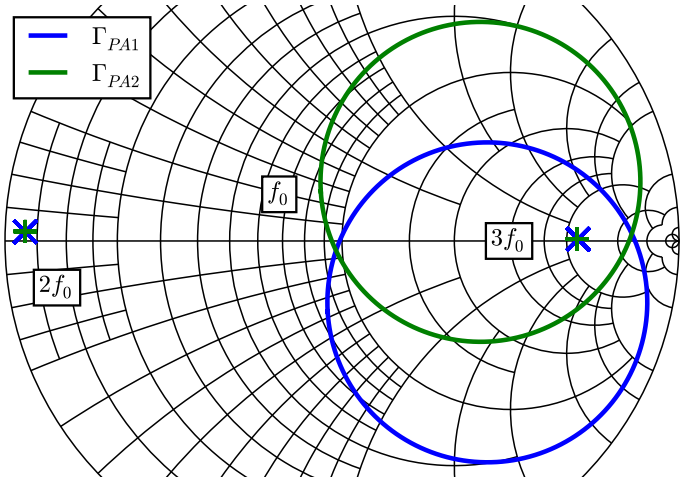


Figure 5.28: Simulated load modulation at the intrinsic drain of each PA during outphasing. The harmonic terminations do not change with fundamental load modulation due to the high quality factor of the resonators.

trade-off between loss and length; a shorter line leads to more dissipative loss in the equivalent network. Using the TL-π equivalent circuit, the long TL is shrunk to fit on the MMIC. The shunt capacitors are visible in Fig. 5.25 at the combiner junction, and the one near the RF pad is split into two parallel capacitors for symmetry.

Fig. 5.28 shows the simulated load modulation at the intrinsic drain of each internal PA during outphasing operation, a differential phase sweep. The fidelity of the harmonic terminations is demonstrated in their immobility. Their effectiveness, though, is always relative to the fundamental impedance. As the fundamental impedance increases with outphasing angle, the effect of the third harmonic termination is decreased. The second harmonic termination is always much lower than the fundamental load, and thus provides a good short circuit. Additionally, the fundamental loading is quite symmetric about the real axis, indicating internal PA power balance.

Using the fundamental load modulation at the intrinsic drain, the combining efficiency or power factor can be calculated and is shown in Fig. 5.29. The system efficiency is the product of the combining and internal PA efficiencies. A second peak is created by the Chireix compensation at an outphasing angle of 80°. The difference between combining efficiencies for each internal PA is small, confirming that the designed load modulation in Fig. 5.26 maintains balanced internal PA output power.

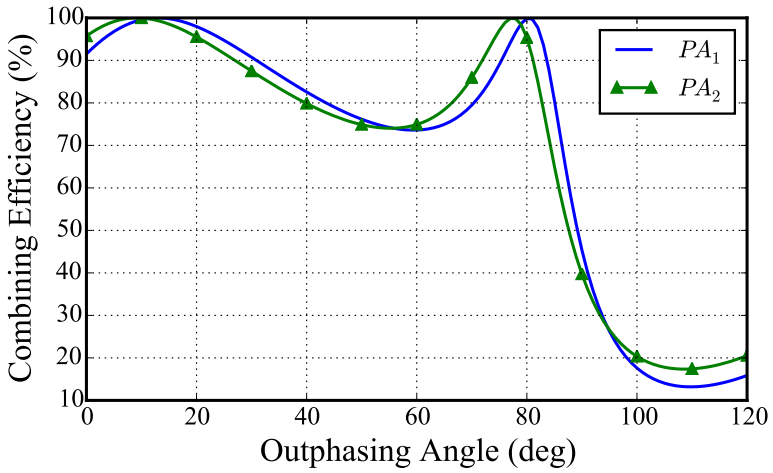
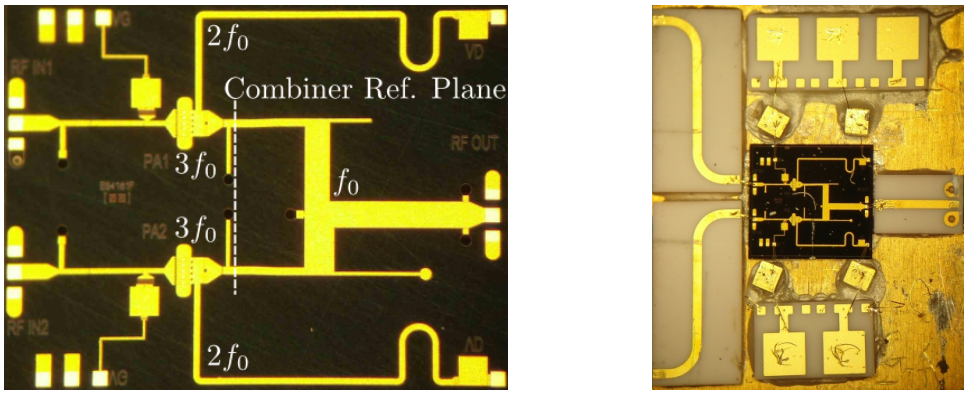


Figure 5.29: Simulated combining efficiency of the microstrip combiner (referenced to the intrinsic drain) is maintained above 70 % over 85° of outphasing range.



(a) (b)

Figure 5.30: Photographs of (a) ML-CO GaN MMIC PA, with a size of 3.8×3.2 mm^2, and (b) MMIC mounted in fixture as detailed in subsection 2.2.3.

5.3.2 Measurement Setup

The 3.8×3.2 mm^2 MMIC is fabricated in Qorvo's 0.15 µm GaN process, and shown in Fig. 5.30a. It is fixtured in a similar fashion to the other MMICs in this work, as detailed in subsection 2.2.3 and shown in Fig. 5.30b. The only difference is that there are two curved alumina lines at the input, rather than a single straight line. This will make a slight difference in the de-embedding of the fixture.

In the measurement setup shown in Fig. 5.31, a phase shifter sweeps the differential phase. The source amplitude on that branch is adjusted to compensate for the variable attenuation of the phase shifter. The

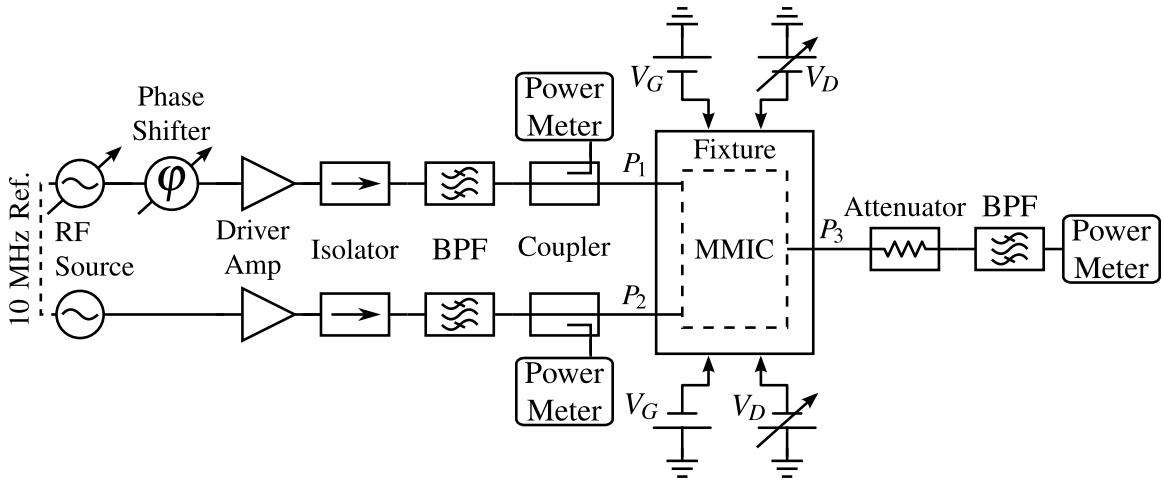


Figure 5.31: ML-CO measurement setup. Separate sources drive each PA branch, while a phase shifter sweeps the differential phase. The source driving the phase shifter adjusts its amplitude to maintain constant available input power to within 0.1 dB.

RF inputs and output are filtered and measured with a power meter. For each desired supply level, V_D, a CW differential phase sweep is performed. The variable supply is implemented with a standard power supply (Keysight E3649A) initially, before testing with a GaN discrete supply modulator MMIC, described in the next section. In both cases, only a CW characterization is conducted: a phase sweep is performed for each statically supplied drain voltage. Since modulated measurements are not performed, the average total efficiency ($\eta_{tot,avg}$) for a modulated signal is calculated in post-processing to provide valuable performance insight. The probability density function (PDF) of a QPSK signal with a 6 dB PAR is shown in Fig. 5.36 and used as a weighting function to yield the average efficiency using the optimal trajectory.

A power calibration must be carefully performed to maintain constant available input power in the phase shifting branch, and balanced power between branches. With the output power meter (PM_3) connected to port P_1 and the phase shifter voltage set initially to 0 V, the source finds the required amplitude to obtain the desired input power measured by PM_3 using a basic difference loop. Starting from an initial value, the source increments its amplitude based on the difference between the desired and measured powers until it obtains the solution within a predefined error. Once the source has the correct amplitude, the phase shifter control voltage is swept, and for each value an offset is calculated and recorded between the newly measured and desired input power. During measurement, this offset table is utilized to maintain constant available

input power. This calibration is performed across frequency and input power levels. Note that available input power is measured because only the forward wave is sampled by the directional coupler, and the output power meter at port P_1 is in a matched, 50 Ω system. The same procedure is performed at input port P_2 to find the required second source amplitude to match the available input power at port P_1. Constant available input power as well as input power balance are maintained within ± 0.1 dB across phase after calibration.

Now that the input power can be precisely controlled, calibration must be performed for the accurate measurement of power. When PM_3 is placed at the input reference plane, P_1 or P_2, its measurement dictates the available input power. The difference between PM_3 and the corresponding coupled port power meter, PM_1 or PM_2, is the frequency dependent difference in loss between the paths from the output of the band-pass filter to the two power meters. This is the offset that must be added to the raw measurement of the coupled port power meter to obtain the power at the input reference plane:

$$\Delta I_{1,2} = \mathrm{PM}_3 - \mathrm{PM}_{1,2} \tag{5.16}$$

At each frequency, any single calibration measurement performed for input power control can be used to find these offsets.

Finally, the output power meter must be calibrated. With the frequency dependent offsets, the input power meters, PM_1 and PM_2, can determine the available input power at P_1 and P_2. Now, the output power meter is connected to the output attenuator and filter, and port P_3 is connected to either port P_1 or P_2. At each frequency, a measurement is performed at any power level high enough to be readable on the connected power meters. The output offset describes the loss through the attenuator and filter, and can be calculated from power meter measurements as:

$$\Delta O = \mathrm{PM}_{1,2} + \Delta I_{1,2} - \mathrm{PM}_3 \tag{5.17}$$

If a "Thru" standard is available on the fixture, its loss can be calculated and de-embedded with another measurement by replacing the fixtured MMIC between port P_3 and port P_1 or P_2 with the standard. At each frequency, another output offset can be calculated exactly as before:

$$\Delta O_T = \mathrm{PM}_{1,2} + \Delta I_{1,2} - \mathrm{PM}_3 \tag{5.18}$$

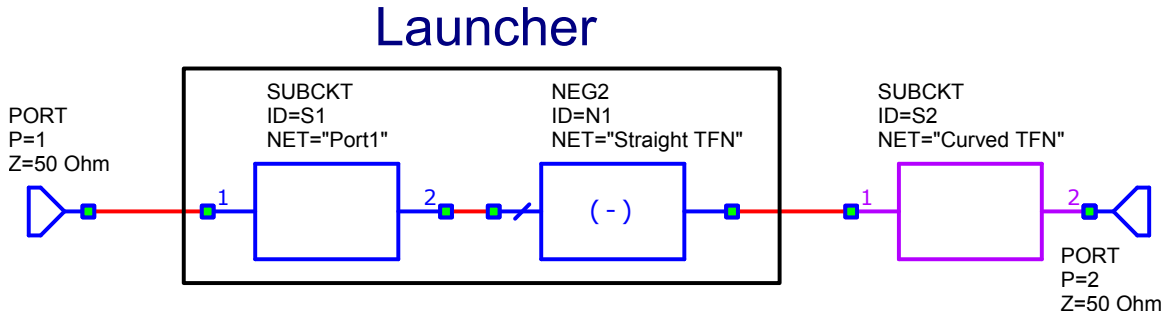


Figure 5.32: AWR schematic of de-embedding straight alumina line simulation from the measured fixture input transition, before embedding the curved alumina line simulation.

and compared to find the through loss:

$$\Delta T = \Delta O_T - \Delta O \tag{5.19}$$

Note that this calibration technique does not take into account reflections at each transition, which will introduce error into the power meter measurements. It is not known how much error is introduced, but the transitions were designed (expensively) to maintain good matching. For example, the launchers have a return loss better than 25 dB at 10 GHz.

Because the input alumina transmission lines on this fixture are curved, no through standard is available to immediately de-embed the fixture loss. Instead, the input and output powers are adjusted in post processing according to the calculated dissipative loss in the fixture transition (launcher and alumina line). The two-port S-parameters of input and output transitions with a straight alumina lines are already known from measurement of the TRL standards, as described in subsection 2.2.3. In NI AWR Microwave Office, the straight and curved alumina lines are electromagnetically simulated with Axiem. The straight line simulation is de-embedded from the measured two-port transition, leaving only the launcher. Afterward, the curved line simulation is embedded onto the launcher to form an estimation of the actual fixture with curved alumina lines, as shown in Fig. 5.32. The magnitude of S_{21} is only decreased by 0.084 dB with the curved line compared to the straight one, and the magnitude of the return loss at each port of the fixture does not change significantly (less than 0.1 dB).

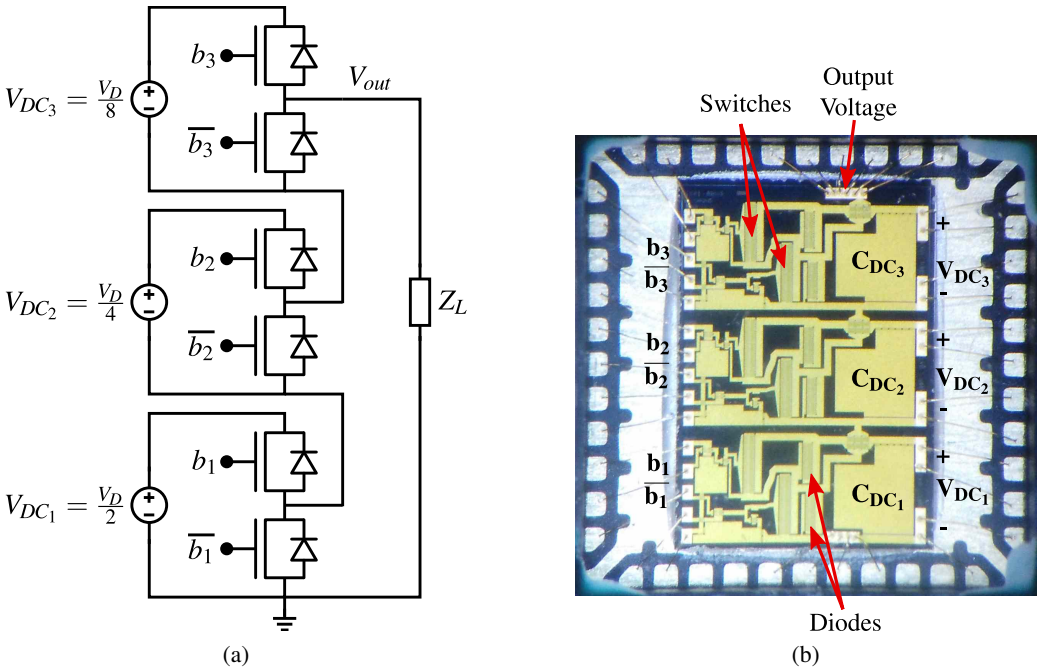


Figure 5.33: (a) Circuit diagram of the power-DAC architecture. (b) Photograph of the fabricated GaN implementation, with a size of 3.8×5.4 mm^2.

5.3.2A GaN Power-DAC MMIC

An implementation of a discrete supply modulator, referred to as a power-DAC in [101], is implemented in Qorvo's 0.15 µm GaN-on-SiC process. The power-DAC is based on a direct digital-to-analog conversion architecture, where the digital bits, b_i and $\overline{b_i}$, control the three half-bridges of the circuit, as shown in Fig. 5.33a. The three half-bridges are supplied with $N = 3$ isolated voltages, whose values are chosen to be binary scaled: $V_D/2$, $V_D/4$, and $V_D/8$. Since the voltage is modulated from 5.5 V to 19.6 V in measurement, a voltage offset of 5.5 V is added in series. The power-DAC output voltage applied to the load is obtained by:

$$V_{out} = \sum_{i=1}^{3} b_i \frac{V_D}{2^i} + V_{offset} \tag{5.20}$$

thus behaving like a DAC circuit, where the output can deliver power to the load. In actuality, the load Z_L in the circuit diagram is the power amplifier.

A photograph of 3.8×5.4 mm^2 chip is shown in Fig. 5.33b. The leftmost pairs of transistors are the high-side and low-side switches of each half-bridge, employing large periphery pHEMT devices (64×150 µm) to

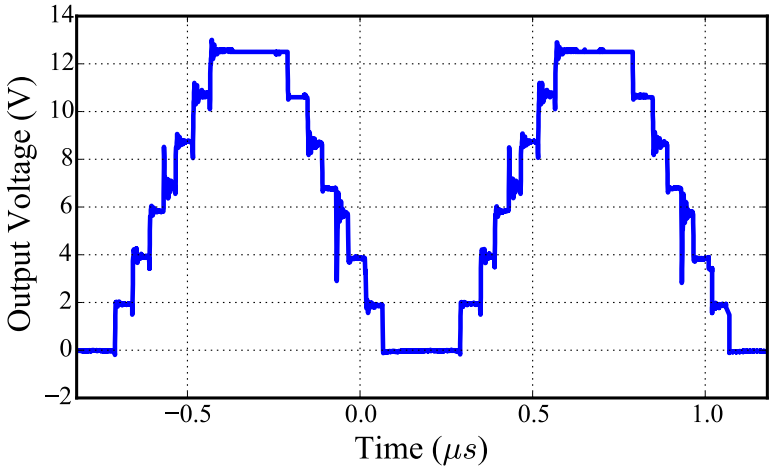


Figure 5.34: GaN power-DAC MMIC output voltage approximate of 1 MHz sinusoid across a fixed resistive load.

reduce the conduction resistance, R_{on}. To the right and in parallel to these power switches, high-side and low-side diodes (40×125 µm) are used to maintain a current path when both switches are turned off (blanking time). The conduction resistance of the power switches has been accurately measured in DC regime to be 0.33 Ω. In every control bit configuration, three switches are connected in series, so the total conduction resistance of the Power-DAC is just below 1 Ω. The isolated supply voltages of each half-bridge are bypassed with an on-chip MIM (Metal-Insulator-Metal) capacitor of 330 pF. In order to control each half-bridge of the power-DAC, The digital control signals, b_i and $\overline{b_i}$, are isolated, level-shifted and amplified by external isolators. Fig. 5.34 demonstrates the power-DAC MMIC output voltage approximating a 1 MHz sinusoid across a fixed, 33 Ω resistive load at a measured efficiency of 96.4%. The GaN-on-Si hybrid implementation in [101] demonstrated linearized tracking of vary fast signals, e.g. 10 MHz LTE. Please refer to this source for more details on this topology.

The details of the power-DAC portion of the measurement setup are shown in Fig. 5.35. The supply board on the right provides the three DC isolated voltages from a single power source, while power-DAC board on the left interfaces these voltages and the digital control signals with the QFN packaged power-DAC MMIC. During ML-CO measurements, only two half-bridges of the power-DAC are utilized to synthesize seven different supply levels. The two supply voltages, labeled V_2 and V_3 in Fig. 5.35, are set to roughly half of the desired output voltage for each level, splitting the current nearly evenly to protect the bond-wires,

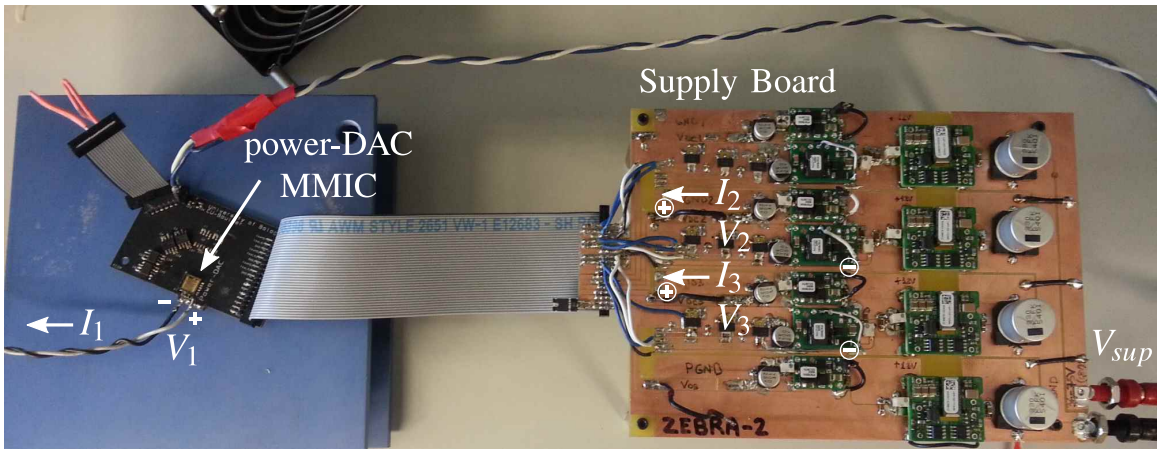


Figure 5.35: Detail of power-DAC portion of overall measurement setup. Three isolated DC voltages are produced by the supply board on the right, while the power-DAC board on the left interfaces digital control signals and DC voltages with the MMIC, which is mounted in a QFN package.

which were continually failing at currents near the peak expected current for the ML-CO PA. The total DC input power for the power-DAC is measured at the two outputs of the supply board with an oscilloscope via current and voltage probes. The DC output power of the power-DAC is measured in a likewise manner along the wires interfaced to the MMIC PA. When a measurement accounts for the power-DAC consumption, the power-DAC input power is used as the DC power in the efficiency calculation. If the power-DAC is ignored, its output power is used as the DC power.

5.3.3 ML-CO Measurement Results

Initially, the measurements are performed with a *power supply* varying the drain voltage statically, while frequency and input power are swept. Fig. 5.36 shows a compilation of phase sweeps for swept supply levels from 6 V to 20 V in 2 V increments at 9.7 GHz. A peak output power of 37 dBm (5 W) is achieved, while a peak total efficiency of 60.2% is reached at 35.7 dBm. The optimal trajectory, which is chosen to maximize total efficiency, remains within 10 points of its peak for 5.45 dB of output power range (ΔP_{out}). An average total efficiency of 48.1% is calculated in post processing for the 6 dB PAR QPSK signal at 9.7 GHz, which is 15.6 points higher than the average efficiency for only the 20 V supply.

The average total efficiency for the defined QPSK signal is calculated across frequency, where the optimal trajectory is determined as described above for the same range of supply voltages. Fig. 5.37 compares the

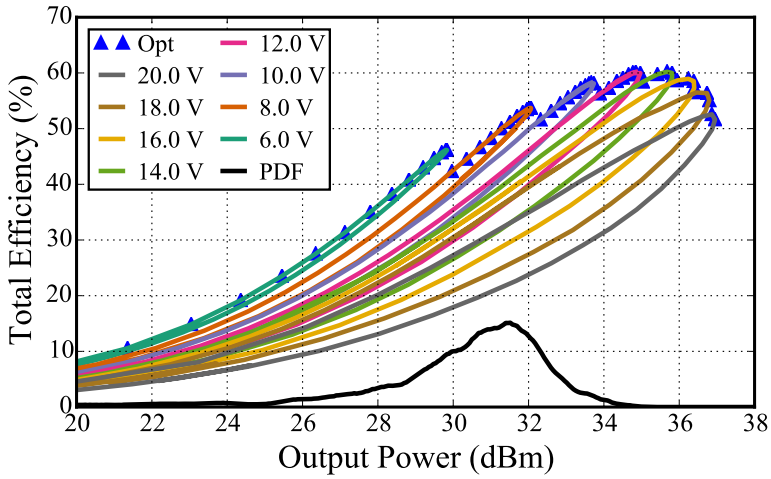


Figure 5.36: Compilation of measured total efficiency for swept differential phase and supply levels from 6 V to 20 V in 2 V increments at 9.7 GHz. The optimal trajectory is selected to maximize η_{tot}. In black is the PDF of a 6 dB PAPR QPSK signal used to calculate average total efficiency.

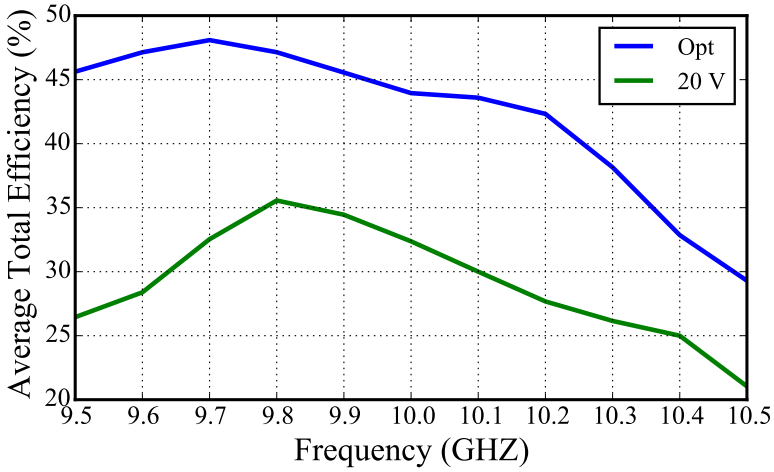


Figure 5.37: Comparison of average total efficiency across frequency between the optimal trajectory and 20 V supply, showing improvements between 8 and 19 points. Optimal operation achieves 400 MHz of bandwdith with $\eta_{tot,avg} > 45\%$.

average total efficiency for the optimal trajectory at each frequency with only the 20 V supply. In the optimal case, the average total efficiency is greater than 45% for at least 400 MHz of bandwidth, from 9.5 GHz to 9.9 GHz. The bandwidth of the driver amplifier and filters limited the frequency range of this measurement on the low end. The improvement in efficiency of discrete supply modulation over constant supply ranges from 8 to 19 points across the measured frequency range.

Finally, the average total efficiency at 9.7 GHz is calculated for restricted number of supply levels and

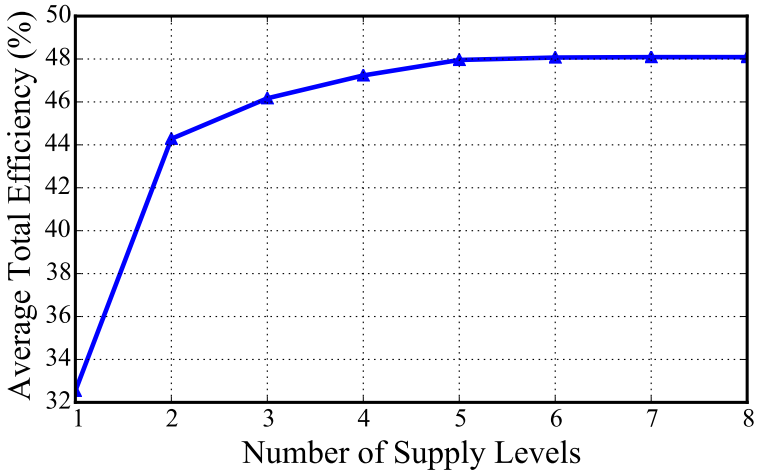


Figure 5.38: Average total efficiency for a 6 dB PAR QPSK signal with restricted supply levels, showing diminishing returns for increasing number of levels.

Table 5.3: Average total efficiency with restricted supply levels

# Levels	Supply Levels (V)	$\eta_{tot,avg}$ (%)
1	20	32.54
2	10, 20	44.3
3	8, 12, 20	45.88
4	8, 10, 12, 20	47.23
5	6, 8, 10, 12, 20	47.96
6	6, 8, 10, 12, 14, 20	48.07
7	6, 8, 10, 12, 14, 16, 20	48.09
8	6, 8, 10, 12, 14, 16, 18, 20	48.09

shown in Fig. 5.38. The 20 V level must be included in all cases to maintain the same peak power. For each number of supply levels, the optimal subset of the measured supplies is found for the 6 dB PAR QPSK signal, by checking the average total efficiency for every combination of supplies in the subset. The optimal subsets are listed in Table 5.3. The addition of a single supply level shows a significant improvement in average total efficiency, 12 points, while the improvements diminish with additional levels, only improving by 4 more points with the addition of 7 more levels.

Now, the static measurements are repeated with the *GaN power-DAC* supplying the drain voltage and power. At each supply level, the power-DAC is manually adjusted and a phase sweep is performed. Due to

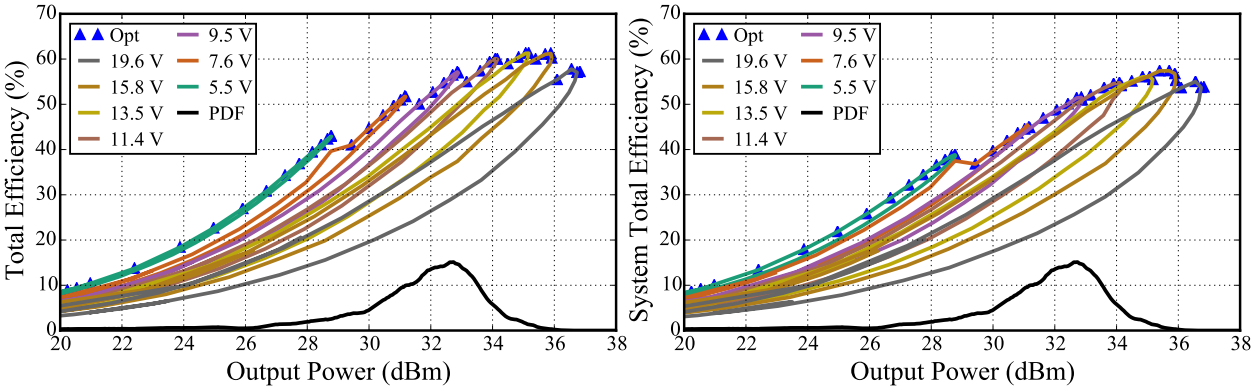


Figure 5.39: Total efficiency (a) without and (b) with considering power-DAC dissipation.

a small resistance in the power-DAC transistors, the supply voltage varies during the phase sweep, since the DC current is varying. The variation ranges from 0.48 V for the 5.5 V level to 1.3 V for the 19.6 V level. Of course, the variation will increase with the supplied current. This measurement is similar to the previous one, except that the power-DAC input power is measured as well, so its efficiency can be taken into account.

Fig. 5.39 demonstrates the total efficiency for swept supply voltage generated by the power-DAC, without considering its power consumption in (a) and accounting for it in (b). The supply voltage vary across the phase sweep, and are labeled with the average value . At 19.6 V, a peak output power of 36.8 dBm or 4.8 W is achieved in both cases. The efficiency curves in Fig. 5.39a should, and do, match very well with those produced using the power supply in Fig. 5.36, since the power-DAC efficiency is ignored.

When taking the consumption of the power-DAC into account, the peak total efficiency drops from 61.3% to 57.4%. The decrease in performance is evident visually in comparing (a) and (b), but more obvious in the comparison of the optimal trajectories in Fig. 5.40. The performance decreases at higher supply voltages, because the efficiency of the power-DAC holds more weight at the system level, since it is supplying significantly higher currents. At 5.5 V, the power-DAC is supplying a maximum of 218 mA, while at 19.6 V, it is supplying 419 mA, corresponding to DC powers of 1.2 W and 8.2 W respectively. However, even when considering the consumption of the power-DAC, the average total efficiency for the 6 dB PAR signal only drops 4 points, from 48.2% to 44.1%. Therefore, the system is further validated by the use and consideration of a real discrete supply modulator.

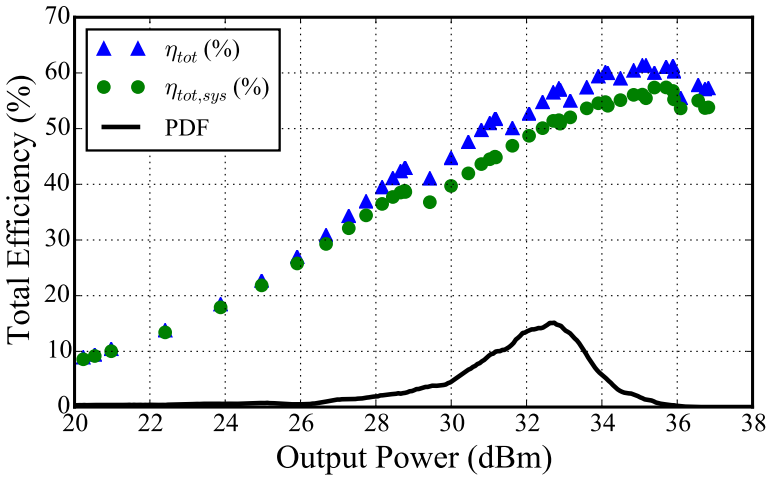


Figure 5.40: Comparison of optimal trajectories with and without accounting for power-DAC consumption.

The efficiency of the power-DAC is shown in Fig. 5.41 for each phase swept supply level, as well as the operating points of the optimal trajectory. The power-DAC operates more efficiently for higher output voltage, and less current (power). Therefore, the efficiency decreases with the supplied voltage level. The curve for each level exhibits hysteresis caused by the load modulation in the ML-CO PA. Along the most efficient load trajectory, the internal PAs draw less current, thereby improving the power-DAC efficiency. As the output power decreases, the power-DAC current decreases, causing the voltage drop across its internal resistance to decrease, increasing the output voltage. Thus, at low output power, the power-DAC supplies the highest voltage for a given supply level and the lowest current, which allows it to operate most efficiently. Along the optimal trajectory the power-DAC operates between 81.5% and 91.5% efficiency.

Again, the average total efficiency is calculated for restricted number of supply levels, as shown in Fig. 5.42 with and without consideration for the power-DAC consumption. In both cases, the diminishing returns are clearly visible, with the system efficiency (considering power-DAC dissipation) approaching 44.1%, 4 points lower than the previous measurements ignoring the efficiency of the discrete supply modulator.

Although these measurements do not prove the dynamic capabilities of amplifying a modulated signal with a ML-CO PA, they provide a more realistic, static characterization of expected performance. In order to amplify with acceptable linearity, nonlinearities caused by both the outphasing dynamics at RF as well as the transient response of the discrete supply modulator will need to be taken into account. Unfortunately,

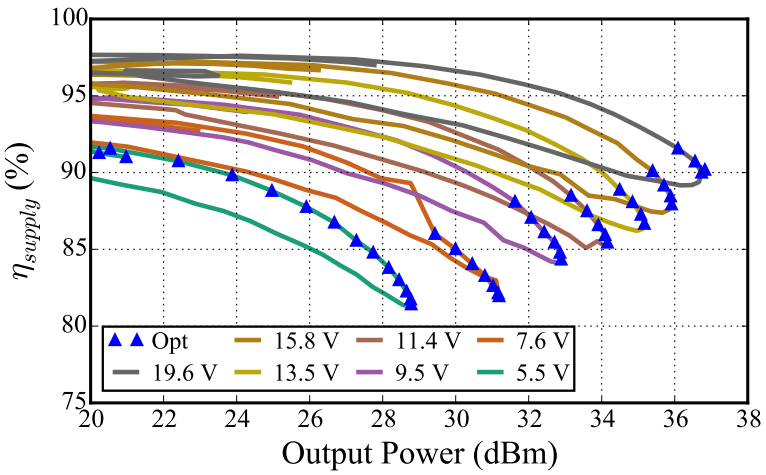


Figure 5.41: Efficiency of the power-DAC, showing the operating points of the optimal trajectory.

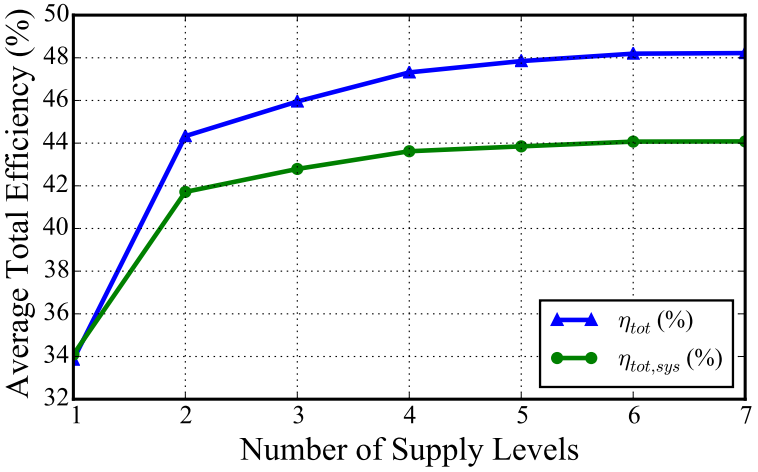


Figure 5.42: Comparison of the average total efficiency for a 6 dB PAR QPSK signal with restricted supply levels, with and without considering the power-DAC efficiency.

due to time and resource constraints, these steps were not attempted.

5.4 Conclusion

The combination of discrete supply modulation with the Chireix outphasing PA was performed for the first time in literature. The internal PA performance and load modulation measurement setup from chapter 2 was extended to include static variation in the drain voltage, while a new Chireix combiner was designed for optimal load modulation with supply variation. The architecture further improved efficiency with a ΔP_{out} of 5.25 dB, which is 0.35 dB beyond AMO. The internal load modulation measurements demonstrated the

difficulty in maintaining internal PA power balance while sweeping the supply. An integrated GaN MMIC implementation was shown to mitigate imbalances seen in the hybrid prototype. The supply modulated Chireix outphasing MMIC PA was tested with a GaN discrete supply modulator, demonstrating improved efficiency for high PAR signals. Finally, a study of supply level restrictions showed that only a few voltage levels are required to produce a significant improvement in average efficiency for a 6 dB PAR signal. Original contributions in this chapter include the following:

- The extension of the internal PA performance and load modulation measurement setup to supply modulated Chireix outphasing [94], demonstrating efficiency improvement, along with significant imbalances of internal PA output power with swept supply, leading to load modulation distortion.
- The prediction of load modulation distortion caused by internal PA output power imbalance was demonstrated to match measurement [83].
- Design of a GaN MMIC PA incorporating all of the RF components of the architecture (class-F internal PAs and Chireix combiner) that achieved 48% average total efficiency for a 6 dB PAR QPSK signal at 9.7 GHz with 5 W of output power [108]. This work won the student paper competition at the Compound Semiconductor and IC Symposium.
- Testing of supply modulated Chireix outphasing GaN MMIC PA with a real supply modulator, implemented in GaN [120].
- Study of optimal supply levels under quantity restriction [108, 120], demonstrating a 12 point improvement only a single additional level.

Special thanks to Tommaso Capello and Prof. Corrado Florian, from the University of Bologna, as well as Dr. Scott Schafer. Tommaso helped perform outphasing measurements with the power-DAC during his stay at CU. Dr. Schafer performed the 0.15 μm GaN layout of the power-DAC to the specifications of Tommaso and Prof. Florian.

Chapter 6

Power Recycling LINC

Contents

Rectification can be incorporated in the LINC PA to improve its poor efficiency roll-off, discussed in Chapter 3. Introduced in [121, 122] and detailed in the block diagram in Fig. 6.1 rectifies the RF power wasted in the isolated combiner. Although the Wilkinson combiner is often used in implementations of the LINC PA, the power dissipated in the isolation resistor is not readily accessible. If a 180° hybrid or rat-race combiner is used instead, the isolated port power is dissipated in an external load, which could be replaced by a rectifying element. The rectified power can be recycled into the power supply of the internal PA through additional power management circuitry. Aside from the work presented in this thesis, the only power recycling LINC PA is demonstrated at VHF in [123], demonstrating a 24.1 point average efficiency improvement for a 50 kHz, 6.5 dB PAR signal at a 48 MHz carrier frequency and 20.8 W of output power.

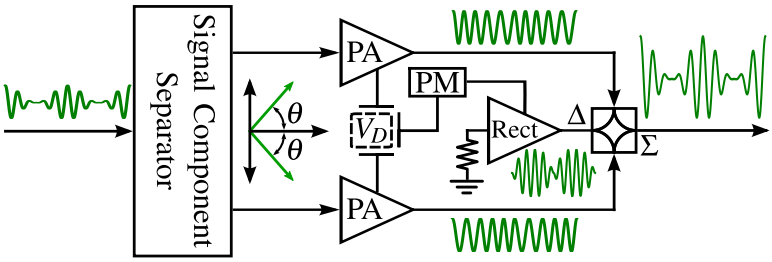


Figure 6.1: Block diagram of a LINC PA with power recycling.

This chapter details a power recycling LINC GaN MMIC PA utilizing a high-efficiency, transistor-based rectifier. Section 6.1 presents the idealized theory behind efficiency improvement in the LINC PA with power recycling. In Section 6.2, the applications and challenges for rectification at microwave frequencies are discussed. Section 6.3 delves into the duality between power amplifiers and rectifiers, while Section 6.4 validates the concept experimentally with two X-band MMIC PAs. Finally, an entire power recycling LINC GaN MMIC PA is presented in Section 6.5.

6.1 Power Recycling LINC Theory

From the block diagram in Fig. 6.1, the efficiency of the power recycling LINC PA can be calculated for a generalized rectifying element. The analysis is performed with the following highly idealized assumptions:

(1) the internal PAs are identical, matched, and isolated;

(2) the rectifier is matched and operates at constant efficiency;

(3) the combiner is lossless;

These assumptions do not take into account branch gain and phase imbalances, or detuning of the combiner by the rectifier, which is treated as a perfect load. From the LINC theory presented in Section 3.1, the power at the sum and difference ports of the isolated combiner are:

$$P_{\Sigma} = 2P_{out,PA}\cos^2\theta \tag{6.1}$$

$$P_{\Delta} = 2P_{out,PA}\sin^2\theta \tag{6.2}$$

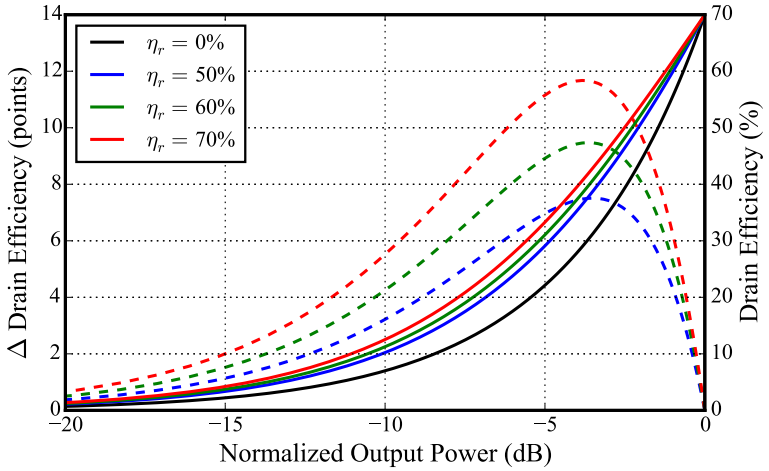


Figure 6.2: Theoretical improvement in system drain efficiency with rectification of power on the isolated port. The internal PAs are assumed to be 70% efficiency ($\eta_{d,PA} = 70\%$), while the rectifier efficiency is set to 50%, 60%, and 70%.

where θ is the outphasing angle. The total DC power consumption can be related to the output power, $P_{out,PA}$, and drain efficiency, $\eta_{d,PA}$, of the internal PAs as:

$$P_{DC,tot} = 2\frac{P_{out,PA}}{\eta_{d,PA}} \tag{6.3}$$

The system drain efficiency without rectification is simply:

$$\eta_d = \frac{P_\Sigma}{P_{DC,tot}} = \eta_{d,PA}\cos^2\theta \tag{6.4}$$

Considering the rectified power, the system drain efficiency becomes:

$$\eta_{d,r} = \frac{P_\Sigma}{P_{DC,tot} - \eta_r P_\Delta} = \frac{\eta_{d,PA}\cos^2\theta}{1 - (\eta_{d,PA})(\eta_r)\sin^2\theta} \tag{6.5}$$

where η_r is the rectification efficiency. The efficiency improvement with rectification can be written as:

$$\Delta\eta_d = \eta_{d,r} - \eta_d = \frac{(\eta_{d,PA}^2)(\eta_r)\cos^2\theta\sin^2\theta}{1 - (\eta_{d,PA})(\eta_r)\sin^2\theta} \tag{6.6}$$

Fig. 6.2 illustrates the theoretical system drain efficiency improvement with rectification. The internal PA drain efficiency is assumed to be 70% and the rectification efficiency is set to 50%, 60%, and 70%, leading to peak system drain efficiency improvements of 7.5, 9.5, and 11.7 points, respectively. These efficiencies are chosen based on expectations for the prototype. Interestingly, the three peaks in improvement occur

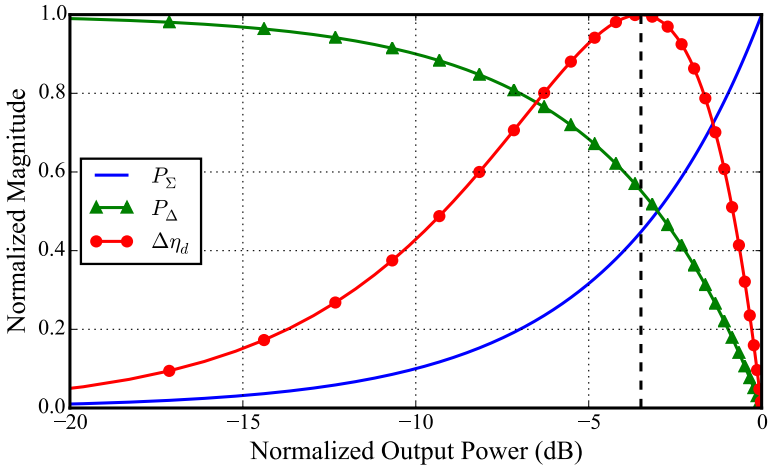


Figure 6.3: Theoretical improvement in system drain efficiency with rectification of power on the isolated port. $\eta_{d,PA}$ = 70%, and η_r is set to 50%, 60%, and 70%.

at -3.49 dB, -3.66 dB, and -3.84 dB normalized output power, respectively, even though the rectification efficiency is held constant with output power.

The improvement from rectification depends on both the sum and difference output powers, which are plotted against the normalized output power (sum port power) in Fig. 6.3. The sum port power is taken as the output power, directly decreasing the efficiency as it decreases. The difference port power is rectified according to the rectification efficiency, thus improving the efficiency as the output power decreases. Near peak power, there is no difference port power to be rectified, and thus no improvement to be made. At the other end, the rectified power is not enough to improve the efficiency with so little output power. Since the efficiency improvement is minimized at low and high output power levels, the peak in efficiency improvement must occur somewhere in between. Fig. 6.3 shows the peak just after the difference port power becomes larger than the output power.

Drain efficiency can be a misleading metric for outphasing PAs, since it does not consider the input power, which is both constant and significant. Therefore, the theory based on the drain efficiency definition is expanded to include input power using the total efficiency definition. The total available input power into the internal PAs is defined as:

$$P_{av} = \frac{2P_{out,PA}}{G_t} \tag{6.7}$$

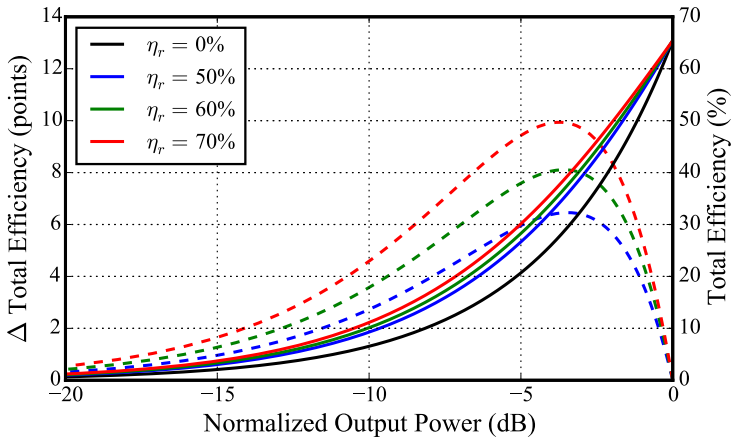


Figure 6.4: Theoretical improvement in system total efficiency with rectification of power on the isolated port. $\eta_{d,PA}$ = 70%, and η_r is set to 50%, 60%, and 70%.

where G_t is the transducer gain of the internal PAs. The system total efficiency is written as:

$$\eta_{tot} = \frac{P_{\Sigma}}{P_{DC,tot} + P_{av}} = \frac{(G_t)(\eta_{d,PA})\cos^2\theta}{G_t + \eta_{d,PA}} \tag{6.8}$$

Considering the rectified power, the system total efficiency becomes:

$$\begin{aligned} \eta_{tot,r} &= \frac{P_{\Sigma}}{P_{DC,tot} + P_{av} - \eta_r P_{\Delta}} \\ &= \frac{(G_t)(\eta_{d,PA})\cos^2\theta}{G_t + \eta_{d,PA} - (G_t)(\eta_{d,PA})(\eta_r)\sin^2\theta} \end{aligned} \tag{6.9}$$

Therefore, the efficiency improvement with rectification is:

$$\begin{aligned} \Delta\eta_{tot} &= \eta_{tot,r} - \eta_{tot} \\ &= \frac{(G_t^2)(\eta_{d,PA}^2)(\eta_r)\cos^2\theta\sin^2\theta}{[G_t + \eta_{d,PA}]\,[G_t + \eta_{d,PA} - (G_t)(\eta_{d,PA})(\eta_r)\sin^2\theta]} \end{aligned} \tag{6.10}$$

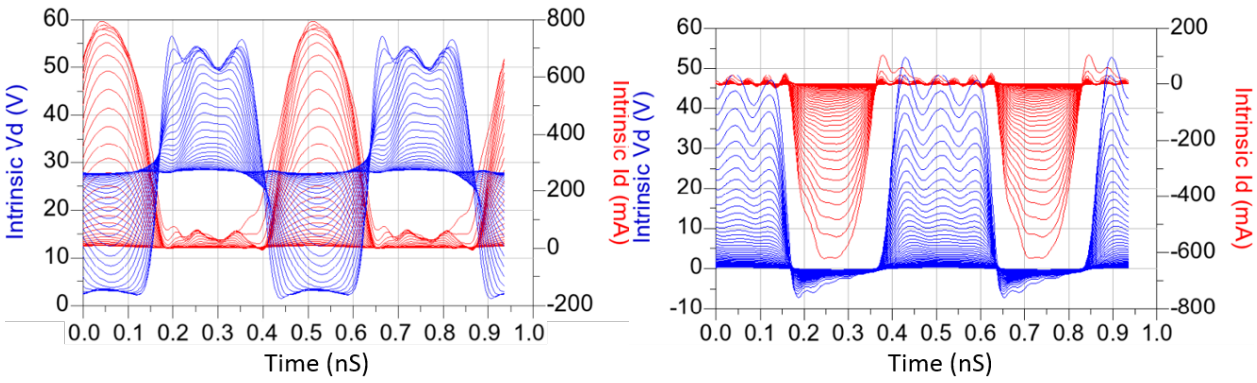
Fig. 6.4 illustrates the theoretical system total efficiency improvement with rectification. Again, the internal PA efficiency is assumed to be 70% and the rectification efficiency is set to 50%, 60%, and 70%, leading to peak system total efficiency improvements of 6.5, 8.1, and 9.9 points, respectively. The three peaks in efficiency improvement occur at the same output power as for the drain efficiency, and for the same reasons as discussed previously.

6.2 Microwave Rectifiers

This section discusses the rectifier portion of the PA in Fig. 6.1. Many applications for microwave rectifiers have developed alongside the modern communication infrastructure. Diode detectors rectify an AM radio signal to receive its envelope. Wireless power transfer is used to power electronics from implanted medical devices [124] to cars [125], all of which must have a rectifier [126]. In wireless energy harvesting, broadband rectifiers are used to recover the ambient electromagnetic waves from sources such as a microwave or a Wi-Fi router [127]. To reduce the size, improve the transient response, and increase the power density of DC power converters, microwave DC-DC converters have been developed [128] by utilizing an amplifier (DC input, RF output) to drive a rectifier (RF input, DC output). Microwave rectifiers can even be used to improve the efficiency of amplifiers under load mismatch by rectifying the reflected power [129].

As it pertains to power recycling LINC PAs, all reported results are based on diode rectifiers, typically using Schottky diodes [121, 130–132]. The focus has been mainly on the variation in input impedance of the rectifier with input power. The primary method to reduce the impedance variation is through the addition of a resistance (or impedance) compression network (RCN or ICN) [130]. Conjugate reactances are used to compress the input impedance of two loads (rectifiers) with the same variation in input impedance. A 100:1 variation in resistance can be compressed to 5.05:1, or a 10:1 variation to 1.74:1. Compressing the input impedance improves the efficiency across input power as well as maintaining impedance matching. Originally implemented with lumped elements, this method has been expanded to utilize transmission lines [133, 134], called a transmission line resistance compression network (TLRCN), to operate up to 4.6 GHz [131]. RCNs have become useful enough to warrant looking into bandwidth restrictions [135] and even dual-band design [136]. Other effective methods at improving rectification efficiency with input power variation include use of a stepped-impedance resonator [132] or a self-biasing scheme [137], which follows an optimal bias trajectory similar to that of an envelope tracking PA.

Unfortunately, the aforementioned research is not suitable to implement in an X-band MMIC. Diode-based rectifiers are not optimal for efficient, watt-level rectification at X-band frequencies, and adding a second rectifier and a TLRCN is not feasible for monolithic integration due to size constraints. Therefore,



(a) (b)

Figure 6.5: Simulated time-domain intrinsic drain voltage (blue) and current (red) waveforms for varying RF power at drain for (a) PA and (b) rectifier operation. For PA operation, V_{DS} = 28 V.

a transistor-based rectifier approach is adopted, enabled by the time-reversal duality between the power amplifier and rectifier circuits as described in [138], and detailed in the next section.

6.3 Time Reversal Duality of Power Amplifiers

Presented in [138] and expanded in [139], the high-efficiency rectifier and high-efficiency power amplifier are shown to be related by time-reversal duality [140] of the transistor's main current source, which means the intrinsic drain voltage and current during rectifier operation are related to those of the amplifier by $v_{PA}(t) = v_R(t)$ and $i_{PA}(t) = -i_R(t)$. In [138], a class-F harmonically terminated transistor amplifier circuit is shown to operate efficiently as both an amplifier and rectifier at 2 GHz. Simulations are performed with a 8×75 µm GaN HEMT model, which includes nonlinear capacitances C_{gs} , C_{gd} and C_{ds}, gate-source and gate-drain diodes, and breakdown and trapping effects. This model reproduces the nonlinear transistor behavior for both positive (first quadrant) and negative (third quadrant) drain voltages. The design of both high-efficiency power amplifiers and rectifiers consist of shaping the intrinsic drain voltage and current waveforms by presenting appropriate load impedances at the fundamental and harmonic frequencies. For the class-F PA circuit with terminations up to the fifth harmonic, Fig. 6.5a shows the expected squared voltage and peaked current. Due to the time-reversal duality of the main current source, the circuit exhibits high-efficiency intrinsic drain waveforms during rectifying operation, as shown in Fig. 6.5b. This technique

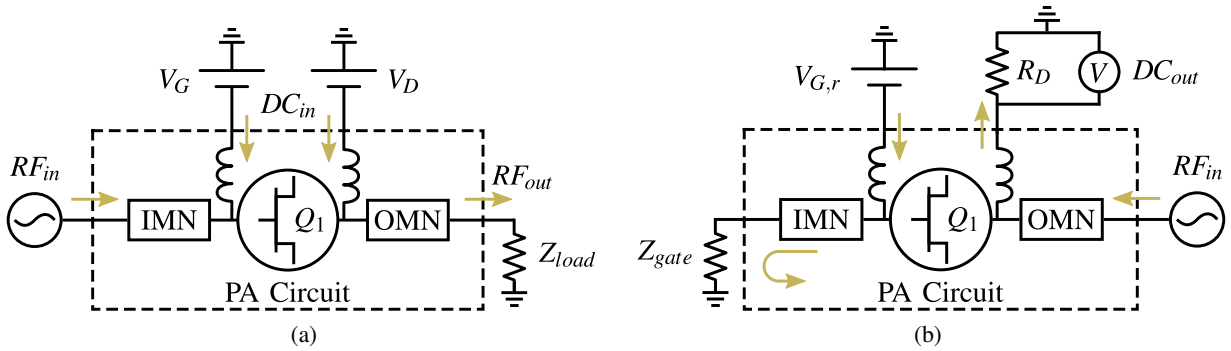


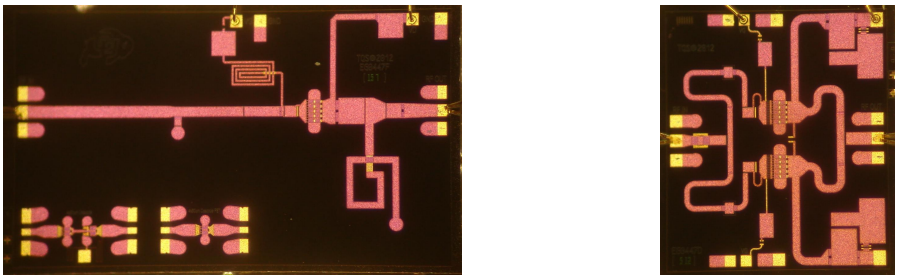
Figure 6.6: PA circuit operating as (a) power amplifier and (b) rectifier.

will be leveraged to implement a highly efficient rectifier at X-band.

Operating a power amplifier as a rectifier is detailed in Fig. 6.6, where the input is now the RF drain, the output is the DC drain, and the gate remains DC biased. The RF source moves from the gate to the drain and increases in power to roughly the saturated output power under PA operation. The drain supply is replaced with a resistive load to measure the rectified DC output power. Synchronous operation of the rectifier requires a second RF source to drive the gate of the transistor to turn it on. Self-synchronous operation relies upon power coupled from the drain to the gate through the shared capacitance, C_{gs}. With a highly reflective termination, Z_{gate}, the coupled power can be reflected into the gate to turn on the transistor without a second RF source.

6.4 X-Band GaN MMIC PA and Rectifier Measurements

Two high-efficiency GaN MMIC PAs [35] are characterized under PA and rectifier operation, to confirm the principle of duality at X-band. Both MMICs are designed Qorvo's 0.15 µm GaN-on-SiC process, and shown in Fig. 6.7. Circuit-A is a single-stage amplifier using a 10×100 µm transistor biased at pinch-off ($I_{DQ} \approx$ 5mA), with an output matching network optimized for efficiency. The layout includes testing structures and has an unnecessarily long input network to fit the reticle layout of the wafer. Circuit-B is a single-stage amplifier that combines two 10×100 µm transistors, biased in deep class-AB, with a reactive combiner.



(a) (b)

Figure 6.7: X-Band MMIC power amplifiers tested as rectifiers. (a) Circuit-A: single-stage PA, at a size of 3.8×2.3 mm^2. (b) Circuit-B: single-stage power combined PA, with a footprint of 2.0×2.3 mm^2.

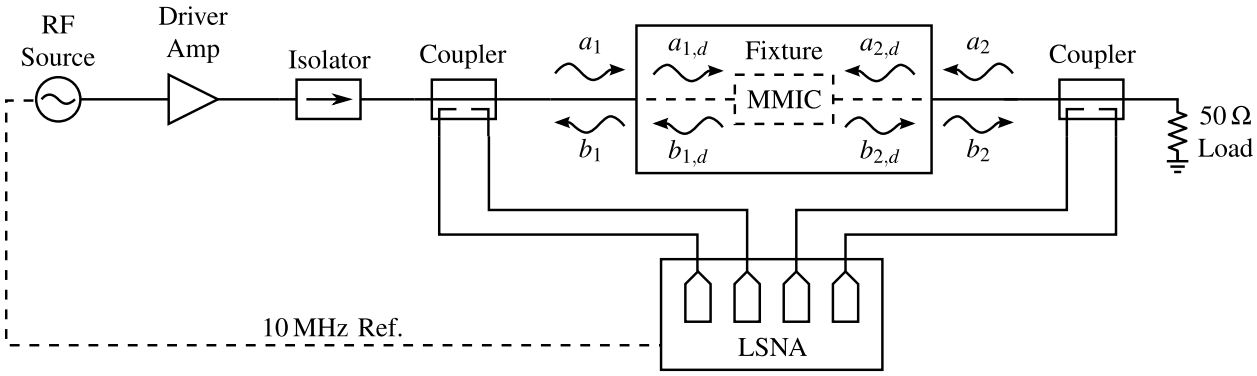


Figure 6.8: Power amplifier measurement setup, utilizing an LSNA. Measurement reference planes are de-embedded to the MMIC bond wire within the test-fixture.

6.4.1 Power Amplifier Measurements

The measurement setup, shown in Fig. 6.8, is equivalent to the setup described in subsection 2.2.3, except for the exclusion of the passive load-pull tuner. Nonetheless, the calibration and de-embedding previously described apply to this measurement as well.

First, the two MMICs are measured as power amplifiers, providing the basis for comparison with the same circuits in rectifying operation. Circuit-A is measured at 10.1 GHz with a gate bias voltage of -4.0 V and drain supply of 20 V. Shown in Fig. 6.9, the MMIC achieves a peak PAE of 68.0% and a peak drain efficiency of 79.1% with 34.8 dBm of output power at an input drive of 25.9 dBm, yielding a saturated gain of 8.9 dB. The DC drain current drawn at peak efficiency is approximately 192 mA. Circuit-B is measured under the same conditions. Fig. 6.10 demonstrates a peak PAE of 63.1% with 35.4 dBm of output power at an input drive of 29.1 dBm, yielding a saturated gain of 6.3 dB. The DC drain current drawn at peak efficiency

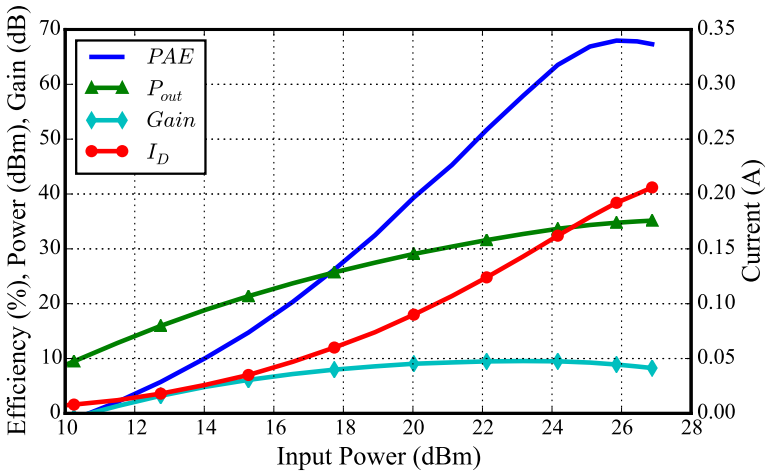


Figure 6.9: Circuit-A power swept amplifier measurement at 10.1 GHz with $V_G = -4.0$ V and $V_D = 20$ V, demonstrating a peak PAE of 68.0% at an output power of 34.8 dBm and 192 mA of DC drain current drawn.

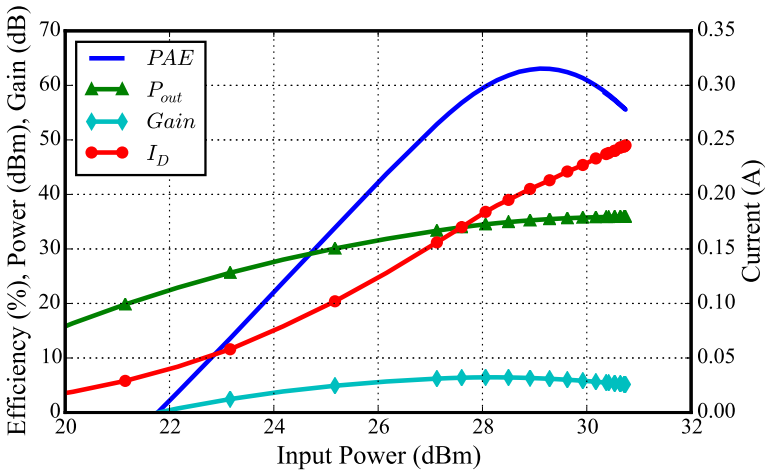


Figure 6.10: Circuit-B power swept amplifier measurement at 10.1 GHz with $V_G = -4.0$ V and $V_D = 20$ V, demonstrating a peak PAE of 63.1% at an output power of 35.4 dBm and 225 mA of DC drain current drawn.

is approximately 225 mA. These power amplifier measurements are straightforward, and will provide the baseline for comparison between power amplifier and rectifier operation.

6.4.2 Rectifier Measurements

The core of the rectifier measurement setup is the same as described for the power amplifier, utilizing the four-channel LSNA and the same calibration and de-embedding methods. The differences arise from the changing operation of the DUT. The setup in Fig. 6.11 orients the MMIC in the same way as the PA

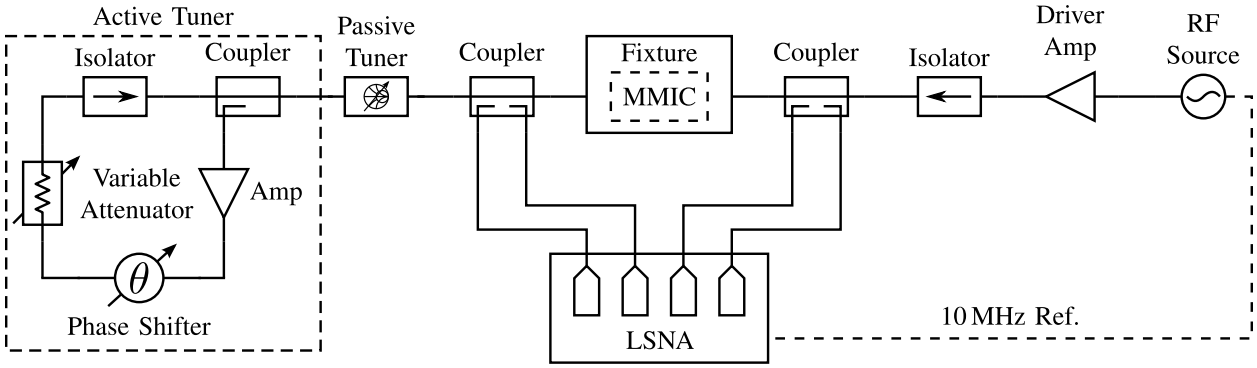
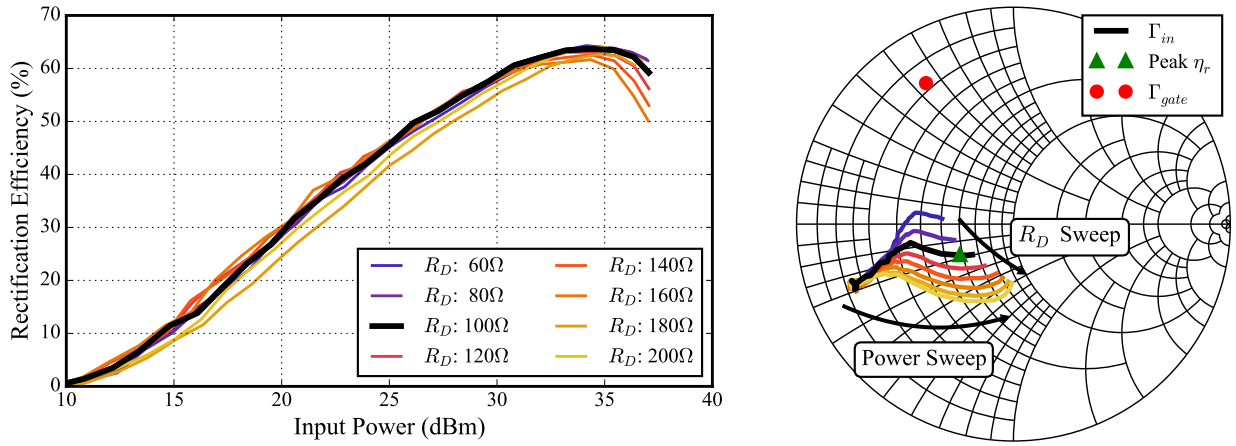


Figure 6.11: Rectifier measurement setup, utilizing LSNA and active tuning on the RF gate. The active tuning loop is used to overcome the losses in the passive tuner and extend the reflection coefficient magnitude achievable. When using active tuning, the passive tuner is set to appear as a 50 Ω transmission line.

measurement setup. While the gate remains biased, the drain bias is replaced with a DC load, R_D. The DC power dissipated in this load is the output power. In this setup, the load is a variable resistor, and the voltage across it is measured with a digital multi-meter to obtain the DC output power. The RF source now drives input power into the drain (PA output). The gate (PA input) is terminated for synchronous operation.

The gate termination is initially implemented with a passive tuner, but the loss between the tuner and the MMIC at the fundamental frequency (10.1 GHz) reduces the achievable magnitude of the reflection coefficient. As will be discussed in detail subsequently, the peak rectification efficiency is achieved with a gate termination at the edge of the Smith chart, at impedances the tuner cannot achieve. Therefore, an active loop is implemented to overcome the losses of the tuner. Although the passive tuner could be used to assist the active loop, it is set to behave as a 50 Ω transmission line during active load-pull. The active loop couples the gate power, sets the magnitude with an amplifier and variable attenuator, and adjusts the phase with a phase shifter, before injecting the power back into the gate to synthesize any impedance on the Smith chart, provided there is enough power. If a nonlinear model that can accurately predict the behavior of the transistor in the third quadrant existed, then the gate termination could be implemented on the MMIC and achieve the high magnitude reflection coefficient required for high rectification efficiency.

In order to obtain optimal rectifier performance, the effect of the variable parameters must be examined for each circuit. The three controls for the self-synchronous rectifier are the DC drain load (R_D), the gate bias voltage (V_G), and the gate termination (Z_{gate}). These parameters have been listed in order of increasing



(a) (b)

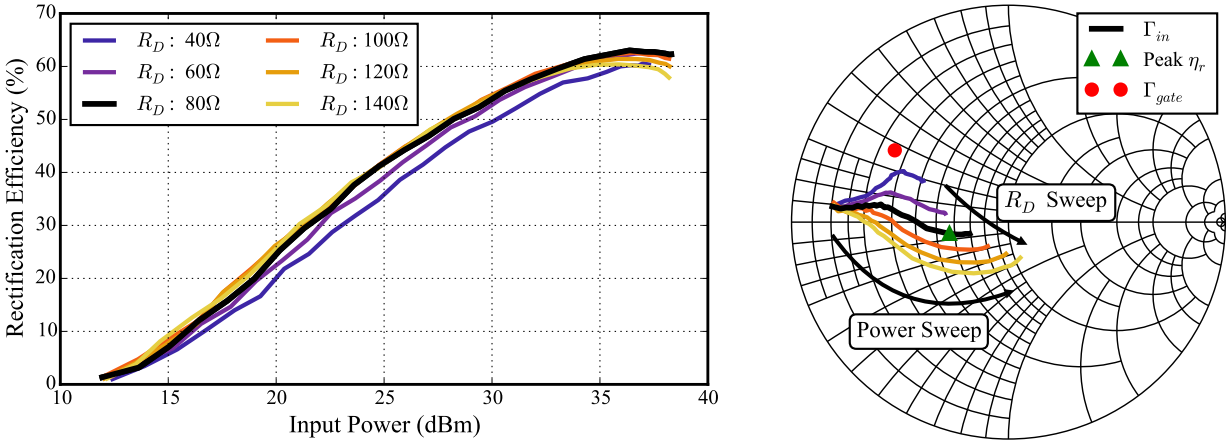
Figure 6.12: Circuit-A (a) rectification efficiency and (b) input impedance as a function of input power and DC drain load. An insignificant 2.7 point fluctuation occurs in the efficiency with load variation, while the input impedance shows more significant variation.

importance and sensitivity with respect to rectification efficiency, which is defined as:

$$\eta_r = \frac{P_{DC}}{P_{in}} = \frac{2|V_D|^2}{R_D \,\mathrm{Re}\left\{v_{f0} i_{f0}^*\right\}} \tag{6.11}$$

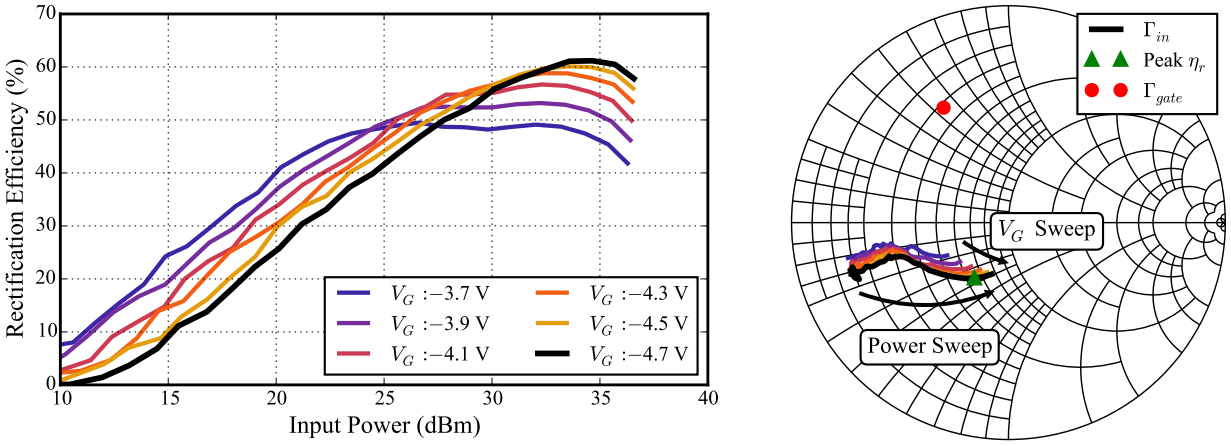
The DC drain resistance will determine the magnitude of the current and voltage for a given output power, and therefore it should be chosen to limit those magnitudes to values that the transistor can handle. The value can be estimated from the power amplifier design and operation. At a 20 V drain supply, both circuits approach approximately 200 mA of DC drain current, which leads to an approximate impedance of 100 Ω. For circuit-A, Fig. 6.12 demonstrates the effect of sweeping the DC drain load on the rectification efficiency and the input impedance at a constant gate bias of -4.7 V and optimal gate termination. The load is swept from 60 Ω to 200 Ω in 20 Ω steps. The peak rectification efficiency, in Fig. 6.12a, is not significantly affected by variations around the optimal 100 Ω load, dropping only 2.7 pts over the measured 140 Ω variation. However, the load impacts the input impedance of the rectifier in Fig. 6.12b.

In Fig. 6.13, similar results are shown for Circuit-B, with a load sweep from 40 Ω to 140 Ω in 20 Ω steps at a gate bias of -4.7 V and suboptimal gate termination. The rectification efficiency varies by only 2.6 points throughout the load sweep in Fig. 6.13a, while the input impedance varies significantly in Fig. 6.13b.



(a) (b)

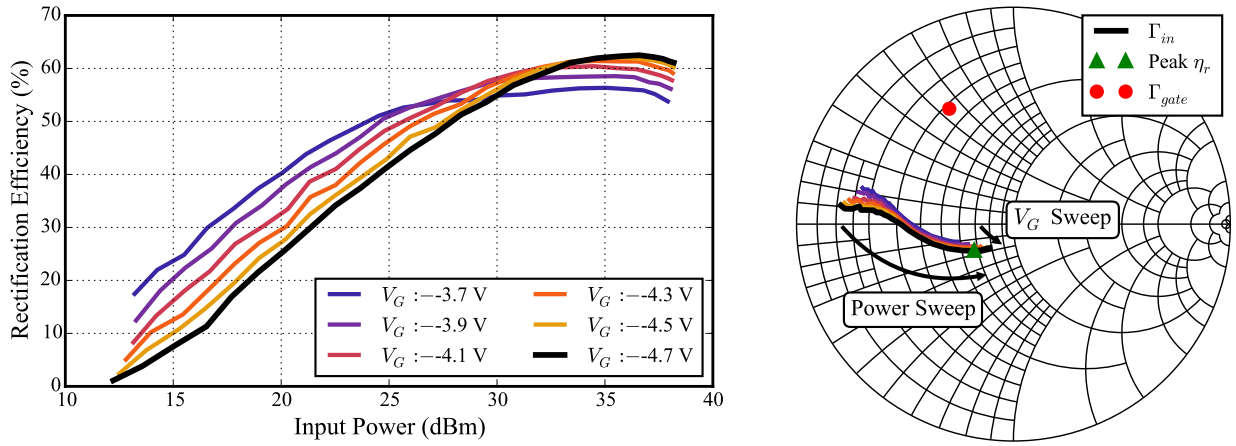
Figure 6.13: Circuit-B (a) rectification efficiency and (b) input impedance as a function of input power and DC drain load. The efficiency ranges by only 2.6 points with variations in the load, while the input impedance shows more significant variation.



(a) (b)

Figure 6.14: Circuit-A (a) rectification efficiency and (b) input impedance of the rectifier under gate bias voltage and input power sweeps. The gate bias voltage is swept from -3.7 V to -4.7 V in 0.2 V increments. Deep pinch-off improves the efficiency by 12 points, but has little effect on the input impedance.

The gate bias affects the rectification more significantly than the DC drain resistance. Fig. 6.14 shows the effect of the gate bias on the rectification efficiency and input impedance of the circuit-A rectifier. The gate bias voltage is swept from -3.7 V to -4.7 V in 0.2 V increments with a drain load of 100 Ω and the optimal passive tuner gate termination. In Fig 6.14a, higher gate biases are shown to turn the transistor on more, causing it to saturate quicker, broadening the range of peak efficiency with respect to input power, but



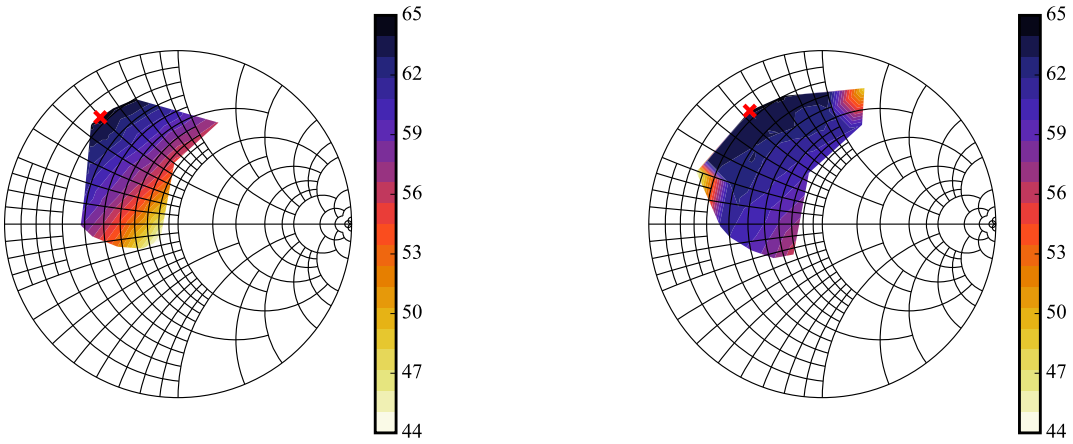
(a) (b)

Figure 6.15: Circuit-B (a) rectification efficiency and (b) input impedance of the rectifier under gate bias voltage and input power sweeps. The gate bias voltage is swept from -3.7 V to -4.7 V in 0.2 V increments. Deep pinch-off improves the efficiency by 6.2 points, but has little effect on the input impedance.

reducing the peak value. As the transistor bias moves toward pinch-off, the peak rectification efficiency is increased by 12 points and narrowed with respect to input power. Contrary to the DC drain load, the gate bias voltage does not significantly affect the input impedance of the rectifier, seen in Fig 6.14b.

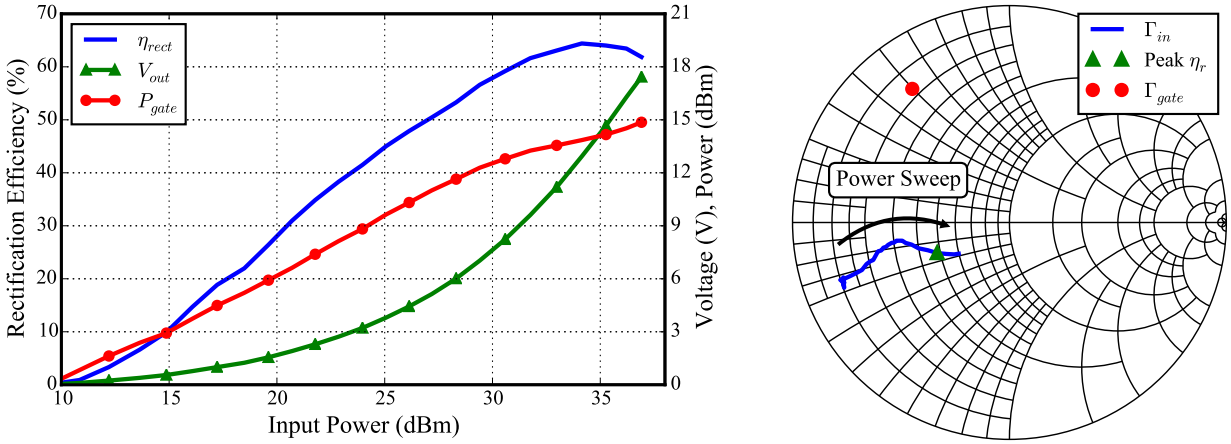
Fig. 6.15 shows the same trend for circuit-B, which is swept over the same bias conditions, gate termination, and drain load, which is 20 Ω away from optimal. Fig 6.15a demonstrates an improvement of 6.2 points in rectification efficiency by reducing the bias of the device, and Fig 6.15b corroborates the insensitivity of the input impedance to gate bias variation.

The gate reflection coefficient, Γ_{gate}, presented by the RF gate termination, Z_{gate}, is the most important parameter for rectification efficiency. The magnitude of the reflection coefficient must be high to reflect enough power, coupled from the drain through C_{gd}, to drive the transistor into saturation, peaking rectification efficiency. The phase of this reflection coefficient is quite sensitive, as shown for circuit-A in Fig. 6.16a, which combines the data taken with the passive tuner with the data using the active loop. Reducing the magnitude of the reflection coefficient from 0.76 at the maximum to 0.3 will decrease the rectification efficiency by 10 points. The active load-pull increased the reflection coefficient magnitude by 0.15, increasing the rectification efficiency by 3 points. Though only a small region of the Smith chart was swept in each case, Fig. 6.16b more clearly shows the phase sensitivity for circuit-B, where significant efficiency degradation occurs at the



(a) (b)

Figure 6.16: Gate termination load-pull contours combining passive tuner and active loop data for (a) circuit-A, and (b) circuit-B.

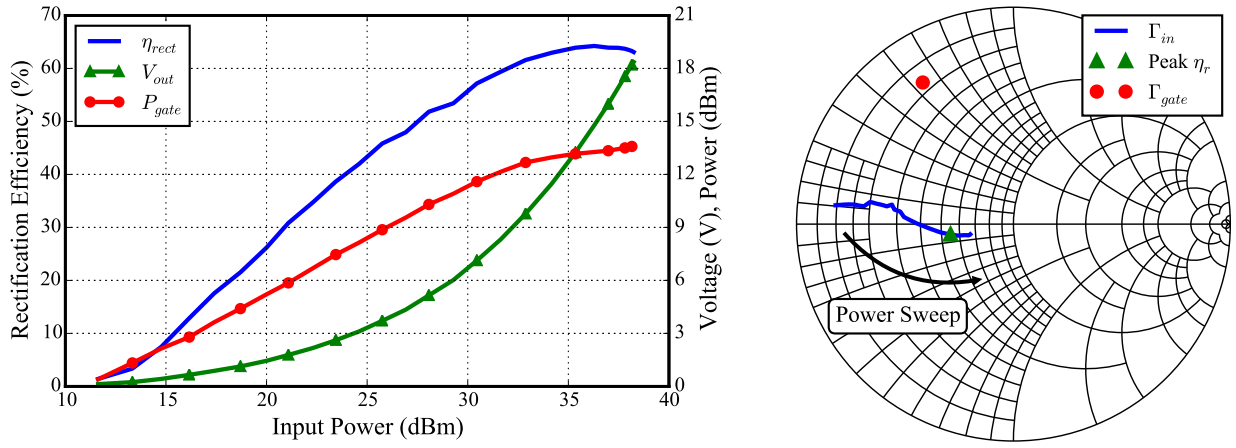


(a) (b)

Figure 6.17: Optimal circuit-A (a) rectification performance and (b) input impedance for swept input power at 10.1 GHz with $V_G = -4.7$ V, $R_D = 100\,\Omega$, and $Z_{gate} = 8.47 + j24.88\,\Omega$, demonstrating a peak efficiency of 64.4%.

phase edges of the active loop sweep. A more complete contour would better display the high sensitivity of the efficiency to the gate termination.

Fig. 6.17a shows the optimal performance for circuit-A operating as a rectifier at 10.1 GHz and biased in deep pinch-off at -4.7 V. The peak rectification efficiency achieved is 64.4% with a DC drain resistance of $100\,\Omega$ and a gate termination of $8.47 + j24.88\,\Omega$, which is achieved with the active loop. The input power required at peak efficiency is 34.1 dBm, which is only 0.7 dB from the output power at peak PAE during PA



(a) (b)

Figure 6.18: Optimal circuit-B (a) rectification performance and (b) input impedance for swept input power at 10.1 GHz with $V_G = -4.7$ V, $R_D = 800\,\Omega$, and $Z_{gate} = 8.18 + j26.8\,\Omega$, demonstrating a peak efficiency of 62.5%.

operation. As the rectifier is saturated and reaches peak efficiency, the DC drain voltage approaches 18 V, close to the optimal drain supply voltage of the power amplifier, 20 V. The 18 V output across the 100 Ω resistor corresponds to 180 mA of output DC drain current, which is also quite close to the 192 mA drawn by the PA at peak efficiency. The power coupled to the gate is shown to do so by a factor that steadily decreases from -9 to -22 dB. The gate power is shown to saturate around the efficiency peak. Fig. 6.17b shows the input impedance variation with input power; the input becomes better matched as the input power increases. The gate termination achieved by the active loop is shown as well.

Fig. 6.18a shows the optimal performance for circuit-B operating as a rectifier at the same frequency and gate bias as circuit-A. The peak rectification efficiency is 62.5% with a DC drain resistance of 80 Ω and a gate termination of 8.18 + j26.8 Ω, which is again achieved with the active loop. The input power required at peak efficiency is 36.6 dBm, which is only 1.2 dB from the output power at peak PAE during PA operation. As the rectifier is saturated and reaches peak efficiency, the DC drain voltage approaches 21 V, close to the optimal drain supply voltage of the power amplifier, 20 V. The 21 V output across the 80 Ω resistor corresponds to 260 mA of output DC drain current, which is also quite close to the 225 mA drawn by the PA at peak efficiency. The power coupled to the gate is shown to do so by a factor that steadily decreases from -9 to -22.4 dB. Again, the gate power is shown to saturate around the efficiency peak. Fig. 6.17b shows

Table 6.1: Comparison of power amplifier and rectifier operation

Measurement	Power Amplifier		Rectifier	
	Circuit-A	Circuit-B	Circuit-A	Circuit-B
Efficiency (%)	68.0	63.1	64.4	62.5
Input Power (W)	3.8 (DC)	4.2 (DC)	2.6 (RF)	4.6 (RF)
Output Power (W)	3.0 (RF)	3.4 (RF)	1.7 (DC)	2.9 (DC)

the same input impedance variation with input power discussed for circuit-A as well as the gate termination achieved by the active loop.

A comparison of the measured PA and rectifier operation is summarized in Table 6.1. As the rectifier is driven into saturation and to peak efficiency, the input power approaches the peak output power of the PA, while the output voltage approaches the drain supply of the PA at peak efficiency. The duality is also present in the DC drain currents drawn by the PA and produced by the rectifier, both reaching the same approximate value at peak efficiency. It is shown that a circuit designed as a high-efficiency power amplifier can be operated as a high-efficiency rectifier with the proper DC drain load, gate termination, and gate bias voltage. Taking two of either circuit presented and arranging them such that a PA sourced a rectifier, a high-efficiency microwave DC-DC converter would be obtained, as shown in [141]. The conversion efficiency would be approximately the multiplication of the PA and rectifier efficiencies.

6.5 Power Recycling LINC GaN MMIC PA

The time reversal duality principle presented and confirmed by X-band MMIC measurements in Section 6.3 plays a critical role in the implementation of a full power recycling LINC PA on a GaN MMIC, which is designed in the 0.15μm GaN process from Qorvo detailed in subsection 2.2.1.

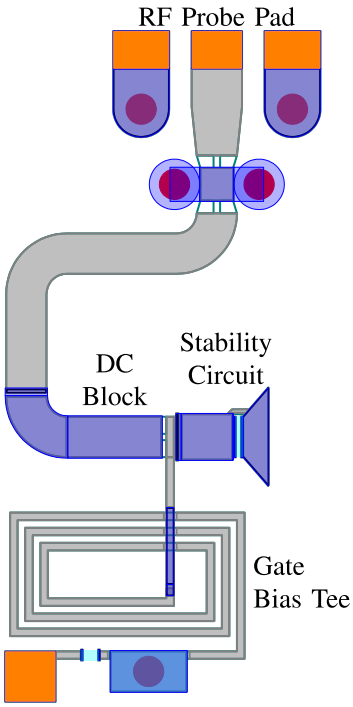


Figure 6.19: Layout of the input matching network for the internal PA and rectifier circuits. Meandering the input line is used to reduce the circuit area and utilize previously empty vertical space.

6.5.1 MMIC Design

6.5.1a Internal Power Amplifier & Rectifier Circuit Design

In this design, the same circuit is used for both the internal PAs and the rectifier, since the available transistor model does not include operation in the third quadrant. Without such modeling, rectifier simulations cannot be performed. Fortunately, the PA-rectifier duality, verified experimentally in Section 6.4, can be utilized to ensure a highly efficiency rectifier based on the design of a highly efficient power amplifier.

The internal PA circuit is based on the previously designed and measured MMIC described in subsection 2.2.2. In order to fit three of these circuits along with a combiner on a single MMIC, the circuit size has to be reduced. Because the original design demonstrated desirable results, the adjustments made are fine tuned to minimize changes in loss or impedance matching. The main difference in the layout can be observed in the input matching network, shown in Fig. 6.19. The network has been meandered to consume less horizontal space by utilizing available vertical space. Additionally, a small adjustment has been made

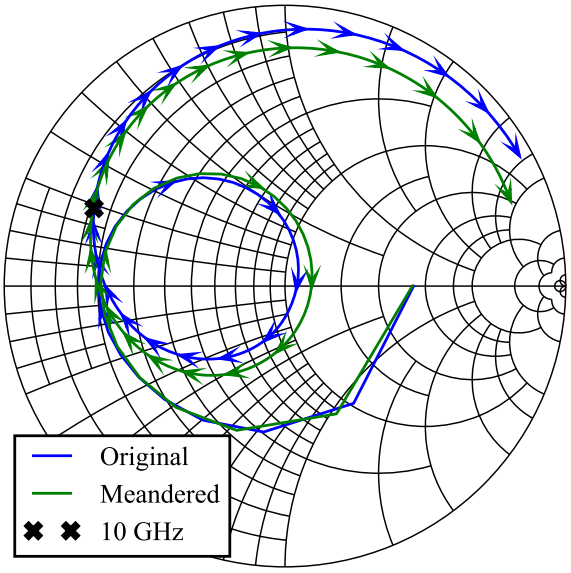


Figure 6.20: Input match (S_{22} of IMN) comparison between the original MMIC design and the new compact layout. The layout changes do not significantly affect the impedance presented to the gate of the transistor.

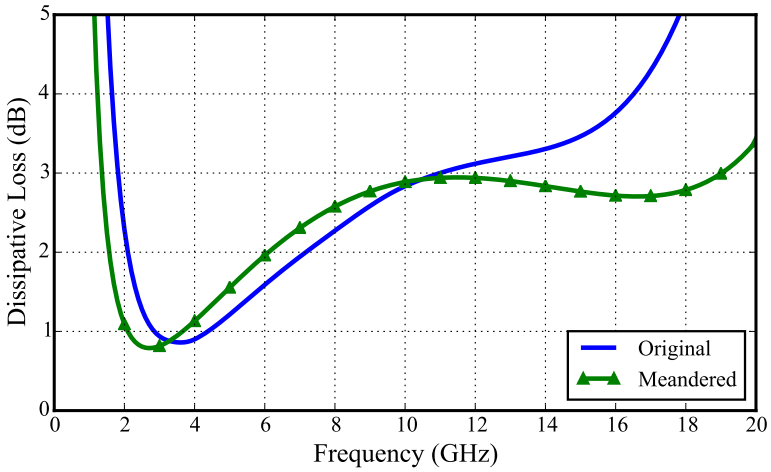


Figure 6.21: Input matching dissipative loss comparison between the original MMIC design and the new compact layout. The meandering of the IMN has increased the loss by 0.052 dB.

to the RF choke inductor, and the shunt matching capacitor has been changed to a capacitor-over-via.

The effects of the layout adjustments on the input match and loss of the input matching network are demonstrated in Figs. 6.20 and 6.21 respectively. At the fundamental frequency of 10 GHz, the impedance presented to the transistors is virtually unchanged. The loss of the input matching network has varied, but only slightly at the fundamental, increasing by 0.052 dB. Therefore, the meandering of the input matching network should not have any significant effects on the fabricated internal power amplifier.

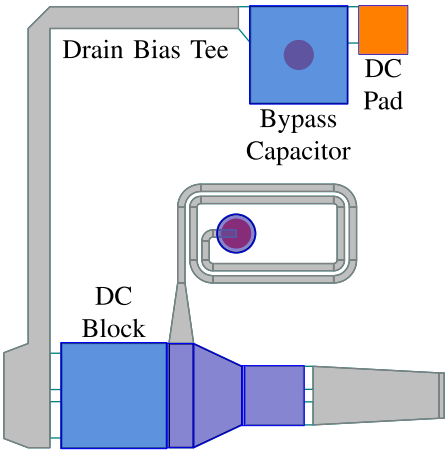


Figure 6.22: Layout of the output matching network for the internal PA and rectifier circuits. The inductor has been shrunk and moved to conserve vertical space.

A similar approach has been taken with the output matching network (OMN), as shown in Fig. 6.22. In the original design, the OMN was 1.8 mm in height, due to the bias tee and the shunt inductor. The new chip length is 3.1 mm vertically, but only 3.075 mm when the saw street is taken into account. To replicate this circuit three times on the chip, its vertical dimension must be less than half of this chip dimension. Unfortunately, the 1.8 mm OMN is larger than the vertical allotment of 1.5375 mm. Therefore, the shunt inductor is shortened and moved to the top side of the signal path, nestled into the opening below the bias tee.

As with the input matching network, the adjustments made to the output matching network are optimized to maintain the performance measured in the original design. Figs. 6.23 and 6.24 demonstrate the effects of the layout adjustments to the output match and loss of the output matching network respectively. At the fundamental frequency as well as harmonics, the transistor is loaded by the almost the same exact impedances as in the original design. Although the harmonic impedances were not intentionally controlled in the original design, replicating them is still important. The new output matching network has actually improved the amount of loss by 0.044 dB.

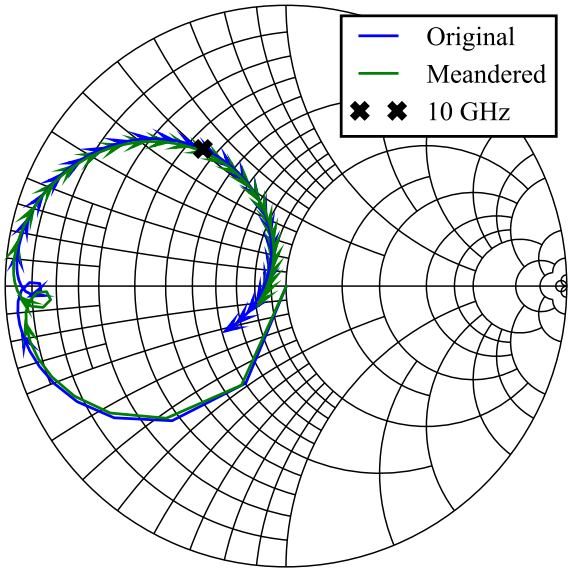


Figure 6.23: Output match (S_{11} of OMN) comparison between the original MMIC design and the new compact layout. The layout changes do not significantly affect the impedance presented to the drain of the transistor.

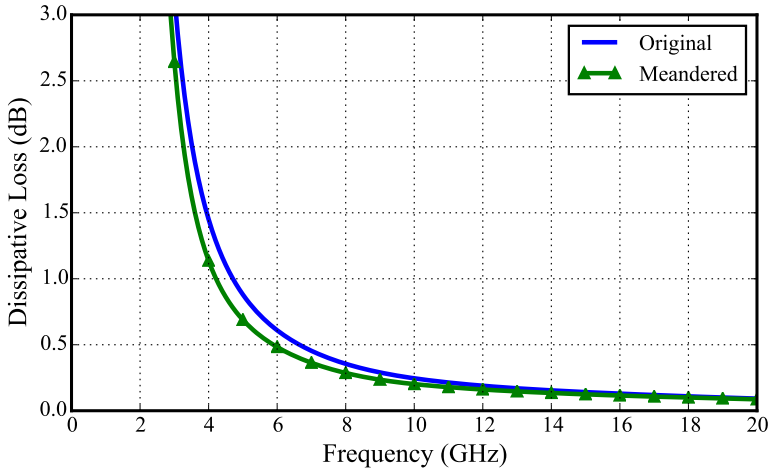


Figure 6.24: Output matching dissipative loss comparison between the original MMIC design and the new compact layout. Adjustments to the inductor have actually decreased the loss by 0.044 dB.

The layout of the internal PA, shown in Fig. 6.25, has been reduced from the original design size of 3548×1793 μm^2down to 1577×1480 μm^2, a much smaller footprint which allows the circuit to be replicated three times on a chip that is 4×3.1 mm^2. The internal PA can be simulated in a 50 Ω environment, since the combiner is expected to be matched to 50 Ω. Of course, at the output of the internal PA, the probe pads and bond wire are left out, since the PA will be connected directly to the combiner. A power swept simulation at

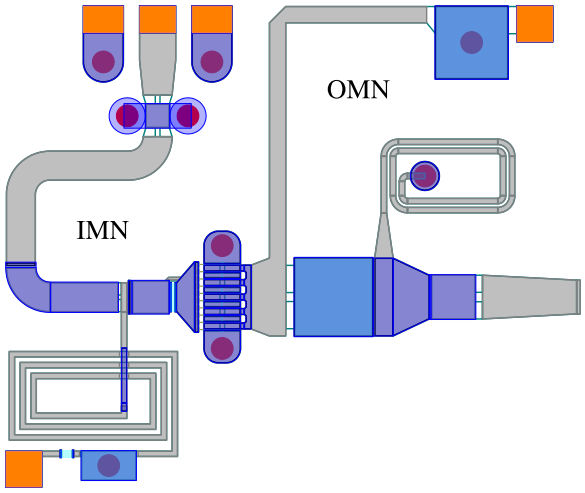


Figure 6.25: Layout of power amplifier circuit, which is also used as the rectifier circuit, appearing three times in the full MMIC layout.

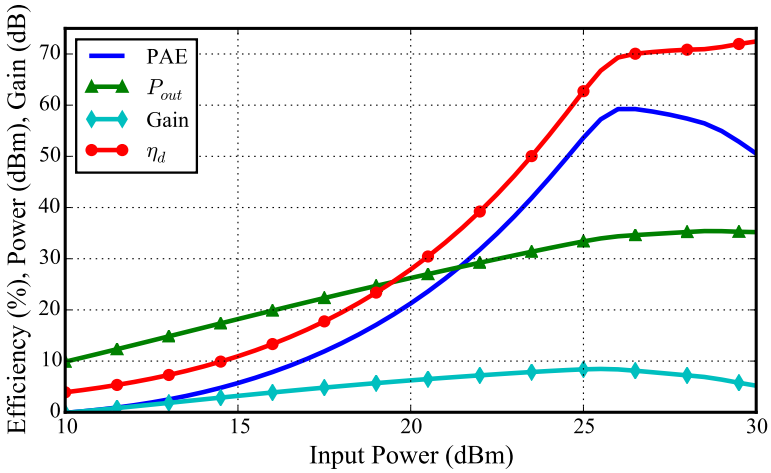


Figure 6.26: Power swept simulation of the internal PA at 10 GHz, showing a peak PAE of 59.2% with an output power of 34.6 dBm and 8.1 dB of gain.

10 GHz is performed from 10 to 30 dBm, as shown in Fig. 6.26. A peak PAE of 59.2% is achieved with an output power of 34.6 dBm at an input power of 26.5 dBm, resulting in 8.1 dB of saturated gain. A frequency swept simulation is performed from 8 to 12 GHz at an input power of 26.5 dBm. The results shown in Fig. 6.27 demonstrate about 2.2 GHz of bandwidth where the peak PAE is above 50%, and even broader bandwidth for reasonable output power and gain. These simulations confirm the minimal effect of the layout changes made for this design as compared to the original design.

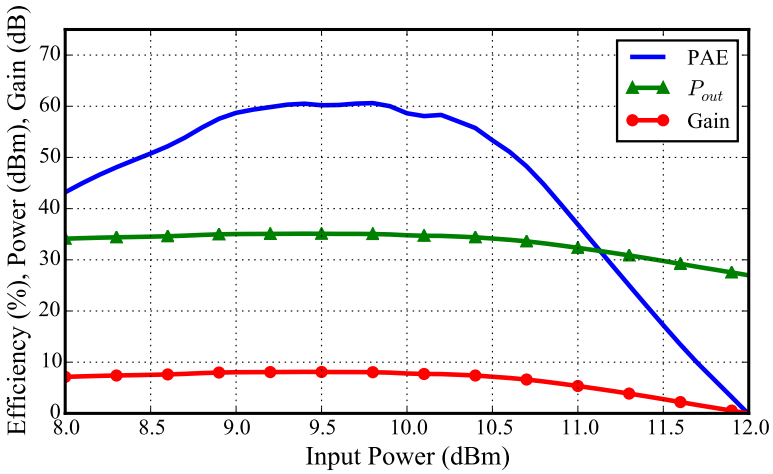


Figure 6.27: Frequency swept power simulation of the internal PA from 8 to 12 GHz at an input power of 26.5 dBm. More than 50% PAE is achieved over 2.2 GHz of bandwidth.

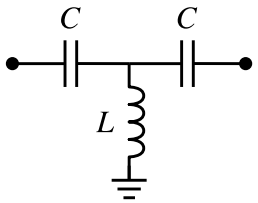


Figure 6.28: High-pass lumped element equivalent T-network.

6.5.1B Combiner Design

A 180°rat-race combiner is utilized for its isolation as well as accessibility to power dumped into the isolated port. Lumped elements can be utilized to shorten the length of transmission lines or fully approximate them as described in [142], and specifically for rat-race combiners in [117, 118]. In this design, a high-pass T-network, shown in Fig. 6.28, is used to approximate the 270°transmission line in the rat-race combiner. The equivalent inductance and capacitance are related to the characteristic impedance of the 270°transmission line by the following [117]:

$$L = \frac{Z_0}{\omega_0} \tag{6.12}$$

$$C = \frac{1}{\omega_0 Z_0} \tag{6.13}$$

The high-pass T-network matches the performance of a long transmission line with only a single inductor, which is beneficial since the spiral inductors in this MMIC process incur more loss than the capacitors. The

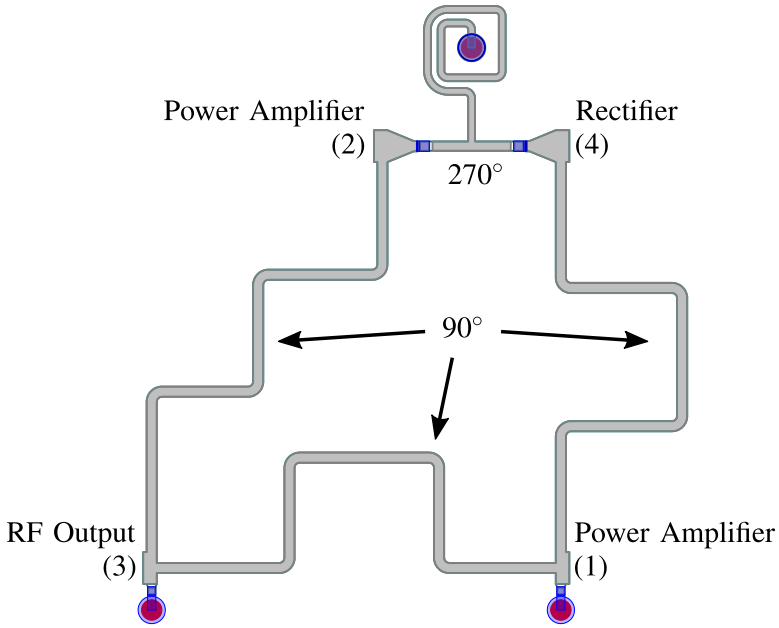


Figure 6.29: Layout of the rat-race combiner. The 90°lines have been shortened using shunt capacitors and the 270°line has been approximated by a T-network, lumped element equivalent circuit.

90°transmission lines not fully approximated by a lumped element network, but simply shortened with a shunt capacitance at the two connection nodes between the three 90°lines.

The layout of the rat-race combiner is shown in Fig. 6.29. The approximate 270°line is at the top, while the others are shortened 90°lines, with the shunt capacitances at the bottom. The 90°lines are meandered to minimize coupling effects, which act to reduce the electrical length, causing more length to be required and increasing losses. The overall size of the combiner is 1600×1815 μm^2.

The combiner is optimized for performance at 10 GHz. Fig. 6.30 shows the through loss from each of the PA input ports (1,2) to the output port (3) and the rectifier port (4), which varies between 0.2 and 0.3 dB at 10 GHz. The phase between the internal PAs and the output ($\angle S_{31}$, $\angle S_{32}$) as well as the rectifier ($\angle S_{41}$, $\angle S_{42}$) and more importantly the difference between those paths ($\angle S_{32} - \angle S_{31}$, $\angle S_{42} - \angle S_{41}$) are shown in Fig. 6.31. At 10 GHz the phase difference between the internal PAs and the output is only 1.7°, while the phase difference between the internal PAs and the rectifier is 179.5°. Therefore, the internal PAs will sum at the output and subtract at the rectifier. The phase exhibits a broader bandwidth than the magnitude. The match presented to each of the internal PAs and the isolation between them is shown in Fig. 6.32. At 10 GHz, the match presented to each PA is better than 31 dB, while the isolation is 46 dB.

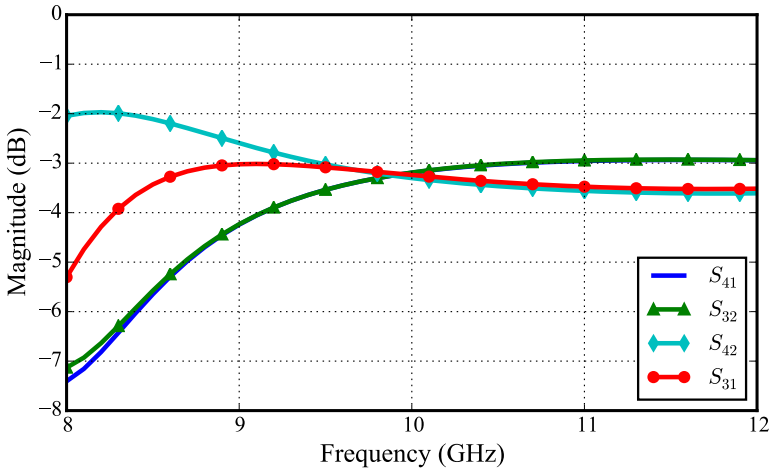


Figure 6.30: Simulated through loss from each of the PA input ports (1,2) to the output port (3) and the rectifier port (4).

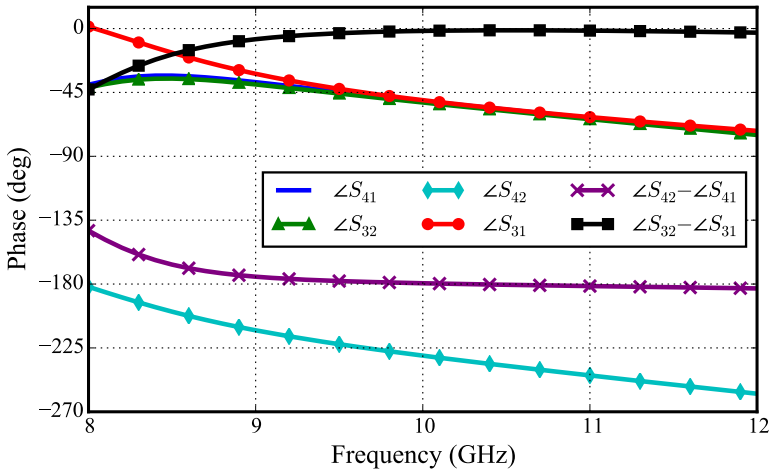


Figure 6.31: Simulated phase between the input and output ports, and the difference between those baths.

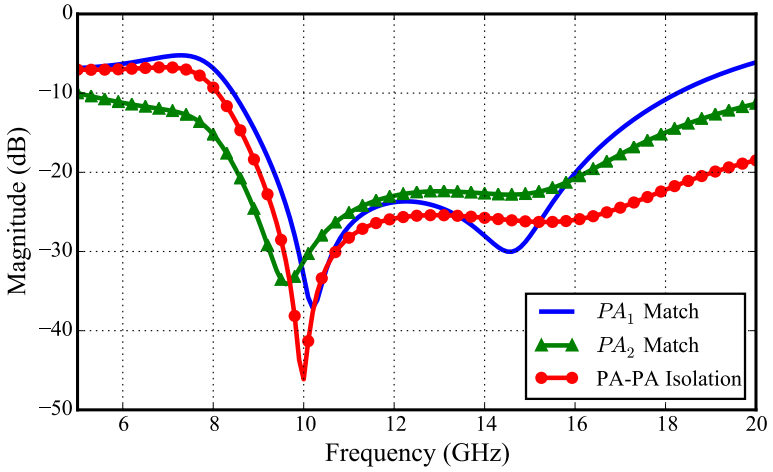


Figure 6.32: Simulated input match and isolation between inputs.

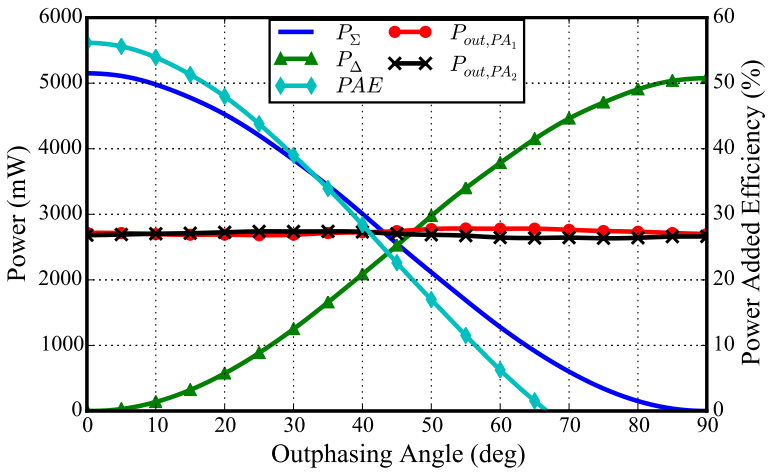


Figure 6.33: Swept outphasing angle simulation of the final MMIC, excluding the rectifier. A peak PAE of 56.3% is achieved with 5.2 W of output power.

6.5.1c Final Simulations

To confirm the design, outphasing simulations are performed without the rectifier, since it cannot be simulated. Outphasing performance is demonstrated in Fig. 6.33 at 10 GHz for an outphasing angle sweep. A peak power of 5.2 W is achieved with a peak PAE of 56.3% when the internal PAs are driven in-phase. A minimum output power of 0.26 mW is achieved with a peak rectifier input power at the difference port of the combiner of 5.2 W. Because the rectifier has half the total periphery of the internal PAs, rectification efficiency should peak when the envelope is half of its maximum, at an outphasing angle of 45°, and remain high as the difference port power increases with the decreasing envelope.

Two concerns arise in the utilization of the rectifier that can be informed by the measurements performed in Section 6.4. Depending on the power handling capabilities of the technology, the rectifier could be overdriven to failure. During previous testing, more than twice the PA output power was driven into the same circuit operating as a rectifier without failure. Another concern is the input impedance variation of the rectifier with input power, which could detune the combiner and cause load modulation or suboptimal performance. In the measurements of subsection 6.4.2, the input impedance varied significantly, but in this case, the variation is unknown. A circuit that can be used to reduce this variation is called a resistance compression network (RCN) [130], which has been implemented in transmission line for high frequencies

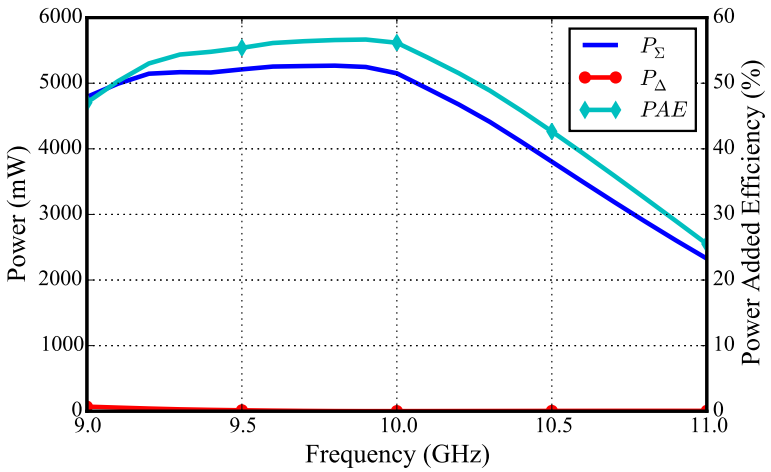


Figure 6.34: Swept frequency simulation of the final MMIC, excluding the rectifier. A peak PAE of 56.3% is achieved at 10 GHz, while PAE remains above 50% for a little over 1 GHz of bandwidth.

in [134]. Unfortunately, these networks require at least two rectifier circuits as identically varying loads, which will not fit within the given chip size. Therefore, nothing is done to mitigate the potential negative effects of the impedance variation in the rectifier other than improving the isolation.

A frequency swept simulation is performed with in-phase drive at 26.5 dBm in each branch. The results shown in Fig. 6.34 demonstrate peak performance at 10 GHz. Furthermore, the PAE remains above 50% for 1.12 GHz. The optimal performance is on the high end of the amplifier pass band, which is a slight concern.

6.5.2 Measurement Setup and Method

The fabricated GaN MMIC PA is shown in Fig. 6.35, and is 4×3.1 mm^{2}in size. The PA circuit is replicated three times, twice as a PA and once as a rectifier. These three circuits are then combined in the center of the chip by the rat-race combiner. Two test devices are included in the bottom left corner of the MMIC. The MMIC is mounted in a similar fashion to the single-stage MMIC PAs previously measured, as shown in Fig. 6.36, and requires four connectorized launchers.

In the measurement setup in Fig. 6.37, a phase shifter sweeps the differential phase, φ, which is twice the outphasing angle, θ. The variable attenuation of the phase shifter is overcome by adjusting the source amplitude on that branch. Constant available power is maintained to within 0.1 dB after calibration, whereby offsets are calculated for each phase shifter control voltage. The available power of the second source is

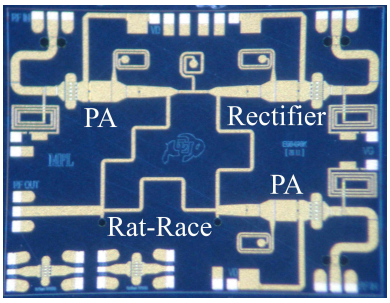


Figure 6.35: Photograph of the outphasing GaN MMIC PA with integrated rectifier. The internal PAs and rectifier utilize 10×100 µm pHEMTs. A shrunken 180°rat-race provides isolation and combining.

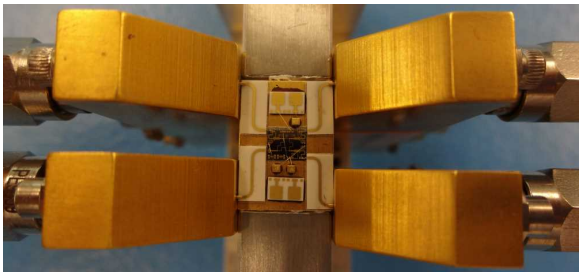


Figure 6.36: Photograph of fixtured GaN MMIC PA. The chip is mounted on a CuMo tab and bonded to alumina transmission lines, on which connectorized launchers land. DC pads are bonded to off-chip bypass capacitors and pads on which to land spring loaded DC pins.

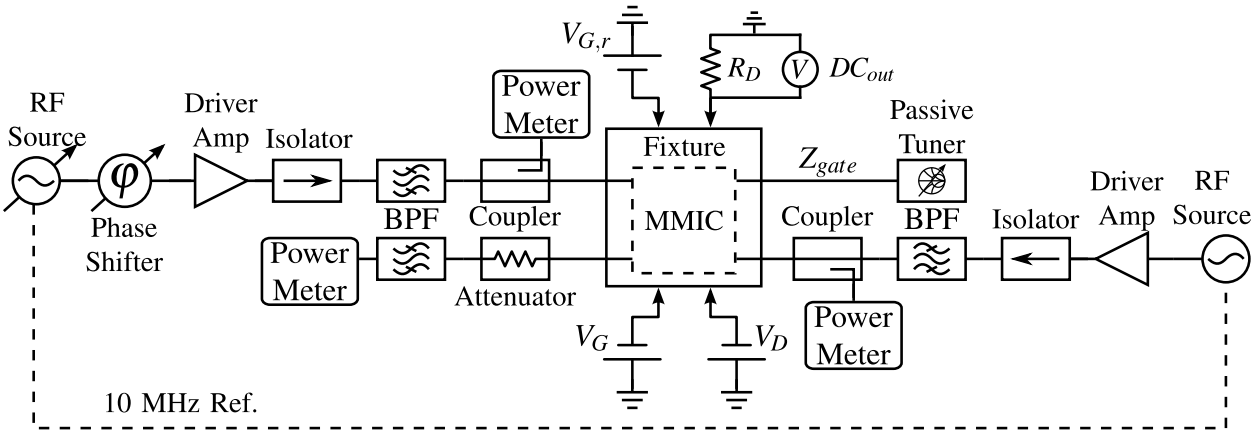


Figure 6.37: Measurement setup sweeps differential phase while maintaining balanced available power (<0.1 dB). The rectifier parameters (R_D, $V_{G,r}$, and Z_{gate}), and PA parameters (Freq, P_{avail}, V_G, V_D) are tunable.

calibrated to match that of the first, in order to maintain balance (<0.1 dB) between the two inputs. These power meter calibrations are performed at the coaxial connector of the launcher, and are detailed further in subsection 5.3.2. A single frequency load-pull tuner is connected to the gate through a short cable in

order to sweep the gate termination Z_{gate}. All measurements are de-embedded from the coaxial connector of the launchers to the MMIC bond wire reference plane in post-processing using the S-parameterss of the fixture transitions. Unfortunately, the fixture transitions are measured only for straight alumina transmission lines, and this fixture required curved lines to space the launchers appropriately. Therefore, the loss through the straight alumina line is simulated and subtracted from the fixture transmission loss, and the loss of the curved alumina line is simulated and added to the fixture transmission loss. At 10 GHz, the longer, curved alumina lines add approximately 0.08 dB of insertion loss to the fixture transitions, which is even less than the uncertainty of a power meter measurement.

As discussed in subsection 6.4.2 and shown in Fig. 6.37, the rectifier has three parameters: R_D, $V_{G,r}$, and Z_{gate}, which are the DC load, the bias voltage, and the RF gate termination, respectively. Note that a circuit to interface the rectifier with the power supply is not implemented in this work, and the rectified power is dissipated in the DC load. Additionally, several PA parameters must be determined: frequency, available power, and PA bias. Due to the large number of unknown parameters, a method is developed to find optimal operation.

First, the optimal internal PA operation is determined with frequency, power, and bias swept measurements. For each combination of these variables, a full differential phase sweep is performed. Because performance at peak output power is evaluated here, the rectifier parameters are set to conservative values. Typically, transistor rectifiers are biased at pinch-off for optimal efficiency. The DC load is initially set to 100 Ω, which was the optimal value measured in subsection 6.4.2. The RF gate termination is 50 Ω to turn off the rectifier. Fig. 6.38 illustrates performance at peak power across frequency for the optimally found available input power of 26.2 dBm and bias of -4.0 V. The MMIC achieves $\eta_{tot} > 50\%$ and $P_{out} >$ 5 W over at least 400 MHz bandwidth. The bandwidth limitation was due to that of the driver amplifier as well as the filters. A finer sweep revealed the optimal operating frequency to be 10.35 GHz. Next, the rectifier parameters are swept with those of the PA fixed at optimal values. Rectified power is measured while load-pull is performed on the gate of the rectifier over various bias conditions and DC loads. The differential phase is set to produce the minimum RF output power prior to the load-pull, to ensure that the rectifier is being driven hardest. Fig. 6.39 shows an optimal rectifier load-pull measurement for R_D = 50 Ω

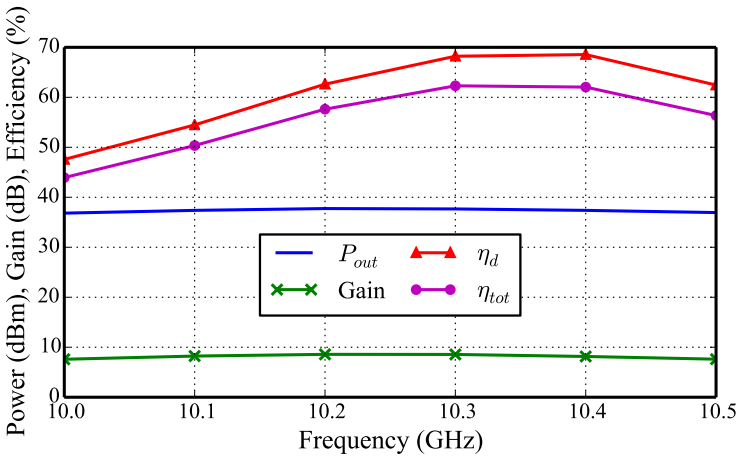


Figure 6.38: Power, gain and efficiency across frequency with in-phase drive. $\eta_{tot} > 50\%$ and $P_{out} > 5\,\mathrm{W}$ achieved over at least 400 MHz bandwidth.

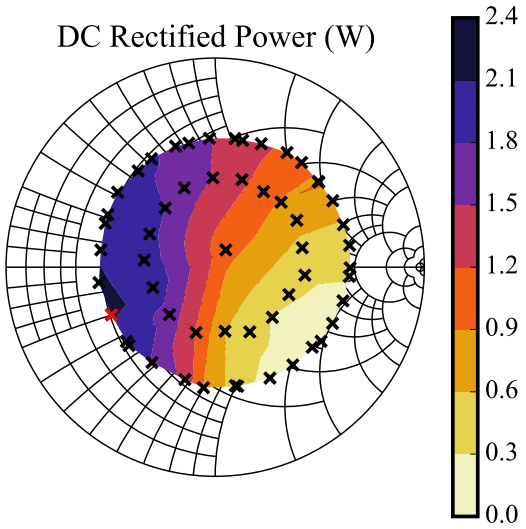


Figure 6.39: Rectifier load-pull (Z_{gate}) for DC rectified power reaches a sensitive peak of 2.24 W. Because $|\Gamma|$ is limited to 0.6, optimal rectified power and efficiency cannot be achieved. Smith chart is normalized to $50\,\Omega$.

and $V_{G,r} = -4.0\,\mathrm{V}$, with 2.24 W of rectified power. Each black 'x' corresponds to a measured impedance. Although the rectified power is most sensitive to Z_{gate}, it is quite insensitive to variation of R_D and $V_{G,r}$. Losses between the MMIC and tuner in the fixture transition and cable are significant at X-band (1.25 dB at 10.35 GHz) and limit the tuning range to $|\Gamma| \leq 0.6$. Improved performance is expected with a higher reflection coefficient magnitude, which can be achieved by active load-pull or on-chip termination.

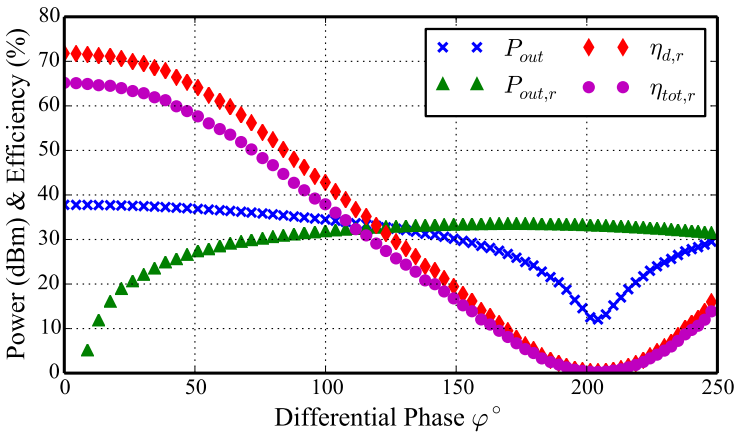


Figure 6.40: RF output power, DC rectified power, $\eta_{d,r}$, and $\eta_{tot,r}$ with optimal PA and rectifier parameters. A peak η_{tot} of 62.5% is achieved with 6 W of RF output power at 10.35 GHz.

6.5.3 Outphasing Measurement Results

With all of the optimal PA and rectifier parameters set, the measured system performance is shown in Fig. 6.40. Both the drain and total efficiencies include rectified power, and reach peaks of 71.80% and 65.2%, respectively, at a peak output power of 37.78 dBm or 6 W at 10.35 GHz. As expected the output power and efficiency peak when driven in-phase, and decrease with differential phase, opposite of the rectified power. Minimum output power is achieved with a differential phase a little greater than the expected 180°due to some branch imbalances most likely caused by the rectifier detuning the combining network.

The efficiency improvement achieved through the addition of the rectifier is demonstrated in Figs. 6.41 and 6.42, with up to 2.24 W of rectified power. η_d and η_{tot} do not include the rectified power, while $\eta_{d,r}$ and $\eta_{tot,r}$ include the rectifier contributions. The differences in efficiency with and without rectification, labeled $\Delta\eta_d$ and $\Delta\eta_{tot}$, reach peak values of 8.1 and 6.5 points at -3.5 dB normalized output power, respectively. The efficiency improvement is confined to the middle region of the normalized output power, as described theoretically.

The agreement between measurement and theory shows that the highly idealized assumptions are realistic. An internal PA drain efficiency of 71.8% and gain of 8.5 dB are extracted from measurement and used in theoretical calculations. Although it cannot be measured, a rectification efficiency of 51% is found to match

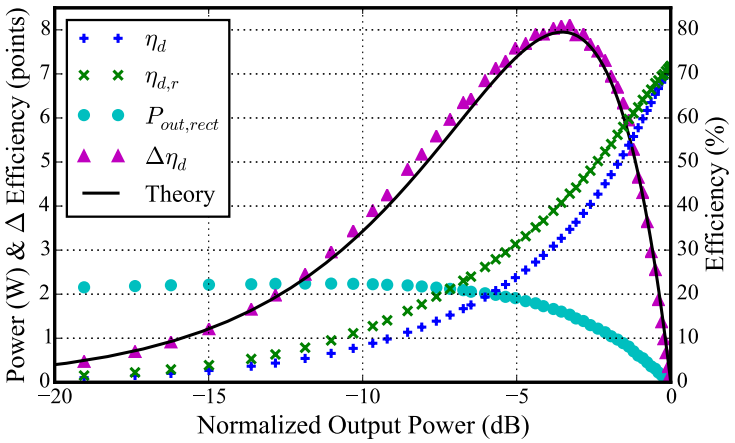


Figure 6.41: Measured η_d, $\eta_{d,r}$, DC rectified power, $\Delta\eta_{d,r}$, and theoretical $\Delta\eta_{d,r}$ demonstrating efficiency improvement through power recycling as envelope amplitude is decreased. Up to 2.24 W of rectified power improves the system drain efficiency by up to 8.1 points at 3.5 dB back-off, matching theory.

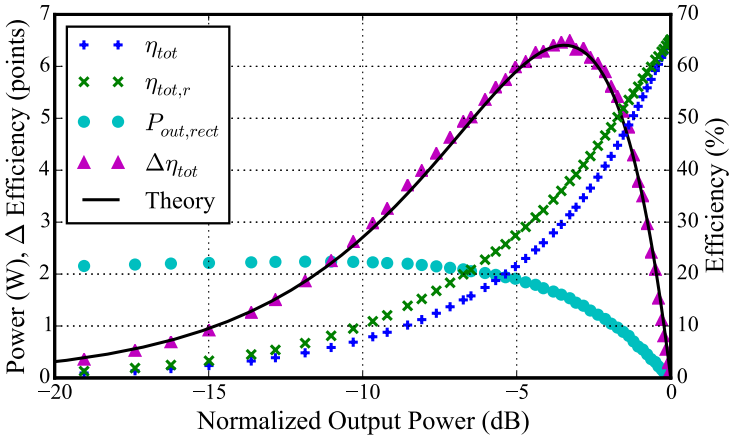


Figure 6.42: Measured η_{tot}, $\eta_{tot,r}$, DC rectified power, $\Delta\eta_{tot,r}$, and theoretical $\Delta\eta_{tot,r}$ demonstrating efficiency improvement through power recycling as envelope amplitude is decreased. Up to 2.24 W of rectified power improves the system total efficiency by up to 6.5 points at 3.5 dB back-off, matching theory.

theory to measurement. Based on experience presented in subsection 6.4.2, this rectification efficiency is reasonable given the reduced tuning range in this measurement. The rectification efficiency is expected to improve to the peak internal PA drain efficiency (> 70%) by increasing the magnitude of the gate reflection coefficient through active load-pull, or on-chip termination. In that case, the peak improvement in system drain and total efficiencies would be 12.9 points and 10.2 points, respectively.

6.6 Conclusion

The utilization of rectification to improve the efficiency roll-off characteristic of the LINC power amplifier is developed theoretically. The duality between high efficiency power amplifiers and high efficiency rectifiers is confirmed experimentally at 10.1 GHz on two GaN MMIC PAs described in [35] and leveraged for this architecture, which is especially critical due to the lack of accurate modeling in the third quadrant (rectification). The entire architecture is implemented on a GaN MMIC (internal PAs, rectifier, and isolated combiner) at X-band. This design is one of three LINC PAs with power recycling, and operates at the highest frequency, 10.35 GHz, among its peers through the use of a high-efficiency, self-synchronous transistor rectifier and GaN integration. Original contributions in this chapter include the following:

- The experimental validation of the high efficiency PA-rectifier duality at 10.1 GHz with two GaN MMIC PAs, which achieved between 62.5% and 68% efficiency in both modes of operation [126, 143].
- The design and measurement of a GaN power recycling LINC MMIC PA, demonstrating a peak drain efficiency of 71.8% with 6 W of output power at 10.35 GHz with a peak rectified power of 2.25 W, leading to a drain efficiency improvement of 8.1 points at 3.5 dB back-off [144].

Chapter 7

Harmonically Terminated Interstage Matching Network

Contents

The effect of internal PA gain in outphasing is most obvious when using the PAE definition of efficiency, because the PAE drops below zero when the output power becomes less than the input power, which is equivalent to the gain in terms of normalized output power in decibels. For example, the PAE will become negative for an outphasing amplifier with 10 dB of gain at 10 dB back-off. While most authors prefer to use the total efficiency definition to avoid the unintuitive negative PAE, or ignore input power altogether with the drain efficiency definition, the internal PA gain concern substantiated by the PAE definition is both present and relevant.

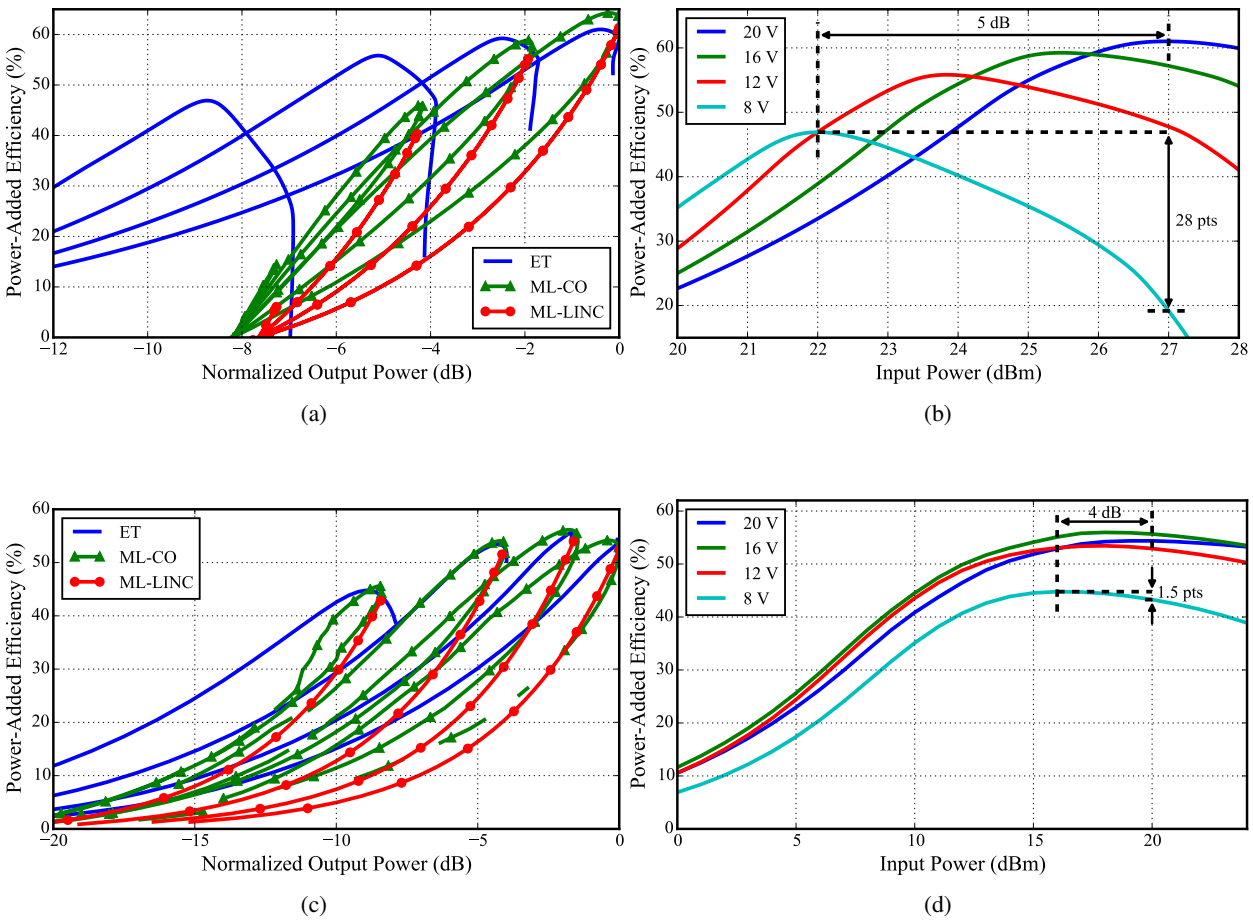


Figure 7.1: (a), (c) PAE comparison between ET, ML-CO, and ML-LINC for single-stage and two-stage PAs, respectively. (b), (d) ET characteristic as a function of input power for single-stage and two-stage PAs, respectively.

The internal PA gain also affects the efficiency of supply modulated outphasing. In simulation, a comparison is made between envelope tracking (ET), ML-CO, and ML-LINC, shown in Fig. 7.1a. Interestingly, the efficiency peaks of ML-CO and ML-LINC occur at approximately the same output power levels, but this is not the case for ET, where the efficienciey peaks extend lower in output power, which is desirable for efficiently amplifying high PAR signals. The difference between ET and ML-CO/ML-LINC is the output power control variable (aside from the supply voltage); input power and outphasing angle, respectively. As shown in Fig. 7.1b, a highly compressed, single-stage PA is sensitive to input power. A 5 dB input power difference exists between the peak PAE at 8 V and 20 V drain voltages. More importantly, the PAE at 8 V has dropped by 28 points from its peak when driven with the optimal input power for 20 V, which is chosen

as the constant input power for the outphasing architectures in this thesis.

The same simulation is performed for a two-stage GaN MMIC PA. A comparison is shown in Fig. 7.1c between ET, ML-CO, and ML-LINC. In this case, the efficiency peaks for each architecture line up quite closely in output power, achieving similar efficiencies at back-off. While a 4 dB input power difference exists between the peak PAE at 8 V and 20 V, the drop in PAE at 8 V when driven at the optimal 20 V input power is only 1.5 points, as shown in Fig. 7.1d. This insignificant drop is due to the two-stage PA having a flatter compression characteristic. Therefore, for optimal supply modulated outphasing performance, the internal PAs should have multiple stages. The increased gain of additional stages reduces the influence and significance of the constant input power.

Note that the roll-off beyond the last peak is not of primary concern. It is common to stop outphasing operation at low output powers, and reduce the input power to improve the poor roll-off of outphasing. This is called mixed-mode outphasing [40, 66, 145, 146]. The same technique is used at low output power levels in ET [96].

The output matching network is most critical to the performance of any high efficiency PA, but in multi-stage PAs, the interstage matching network (ISMN) dictates the overall performance of the cascaded amplifier stages. The cascade of multiple stages can be leveraged to improve linearity [147, 148]. Most often though, amplifier stages are cascaded to increase gain. Historically, this has reduced ISMN design to a fundamental frequency complex matching problem, on which many design analyses have been based [149–152]. Even some high efficiency PA designs only consider the fundamental frequency of the ISMN [153–155].

In order to keep improving PA efficiency, the ISMN must be optimized at harmonic frequencies. Very little work has been published in this area. One approach is to utilize the driver stage to shape the intrinsic gate waveform of the output stage, as done in [156], where an inverse class-F stage drives a class-F power stage. Compared to the class-F power stage alone (without input harmonic terminations), the two stage PA achieves a peak efficiency 4 points higher, and 200 MHz more bandwidth with the PAE greater than 60%. This excellent work is based on the study of input harmonic injection [157, 158]. Unfortunately, it necessitates a custom model with access to the intrinsic gate. Another approach is to harmonically terminate the driver stage to improve its efficiency [159, 160]. Still, few details are given concerning the ISMN design.

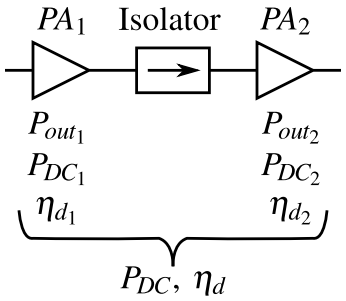


Figure 7.2: Two-stage PA analysis diagram

This chapter aims to improve the understanding of harmonically terminated ISMN design. In Section 7.1, a theoretical basis for the efficiency of cascaded amplifiers is formed. The approach to ISMN design begins with an understanding of the complex, bi-directional, independent matching it must perform in Section 7.2. Eleven lumped-element and transmission line ISMNs are derived in Section 7.3 as starting points for design, one of which is substantiated by a design example in Section 7.4.

7.1 Cascaded Efficiency Analysis

A useful starting point is to evaluate, theoretically, how the addition of a driver stage affects the performance of the power stage. To accomplish this, the circuit in Fig. 7.2 is considered. The isolator represents the assumption that the two stages do not interact with each other, therefore its loss is not considered as this architecture will not actually be implemented. This assumption will be true if the transistors are sized properly, and the ISMN is designed well.

7.1.1 Cascaded Drain Efficiency

The drain efficiency of the cascaded stages is defined as:

$$\eta_d = \frac{P_{out_2}}{P_{dc}} \tag{7.1}$$

The DC power consumed by each stage is defined independently as:

$$P_{dc_1} = \frac{P_{out_1}}{\eta_{d_1}} \tag{7.2}$$

$$P_{dc_2} = \frac{P_{out_2}}{\eta_{d_2}} \tag{7.3}$$

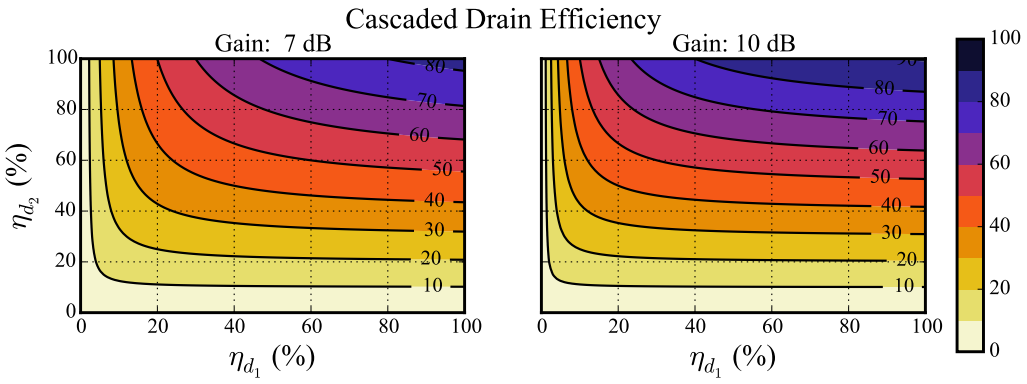


Figure 7.3: Cascaded drain efficiency of the circuit in Fig. 7.2 as a function of the efficiency of each stage, shown for output stage gains of 7 and 10 dB.

The total DC power consumed is the sum of each individual PA consumption:

$$P_{dc} = P_{dc_1} + P_{dc_2} = \frac{P_{out_1}}{\eta_{d_1}} + \frac{P_{out_2}}{\eta_{d_2}} \tag{7.4}$$

Since the isolator is assumed to be lossless, the input power of PA_2 is equal to the output power of PA_1, yielding:

$$P_{out_2} = G_2 P_{out_1} \tag{7.5}$$

Substituting (7.4) and (7.5) into (7.1), and simplifying yields:

$$\eta_d = \frac{\eta_{d_1}\eta_{d_2}}{\eta_{d_1} + \frac{\eta_{d_2}}{G_2}} \tag{7.6}$$

as found in [159].

The cascaded drain efficiency is plotted in Fig. 7.3 as a function of the drain efficiency of each stage for output stage gains of 7 and 10 dB. Given an expected gain and efficiency of the output stage, the required efficiency of the driver stage can be determined for the desired cascaded efficiency. As the gain of the output stage increases, its efficiency increasingly influences the cascaded efficiency. Because of this, the contours in Fig. 7.3 are flatter in the right plot (10 dB) compared to the left (7 dB), decreasing the required driver stage efficiency and increasing the region of high efficiency.

7.1.2 Cascaded Power-Added Efficiency

Extending the analysis to consider the gain of the driver stage, the cascaded power-added efficiency is investigated. It is defined as:

$$PAE = \frac{P_{out_2} - P_{in_1}}{P_{dc}} \tag{7.7}$$

The DC power consumed by each stage is defined as:

$$P_{DC_1} = \frac{P_{out_1}}{\eta_{d_1}} \tag{7.8}$$

$$P_{DC_2} = \frac{P_{out_2}}{\eta_{d_2}} \tag{7.9}$$

The total DC power consumed is the sum of each individual PA consumption:

$$P_{DC} = P_{DC_1} + P_{DC_2} = \frac{P_{out_1}}{\eta_{d_1}} + \frac{P_{out_2}}{\eta_{d_2}} \tag{7.10}$$

Again, the isolator is assumed to be lossless, so the input power of PA_2 is equal to the output power of PA_1, yielding:

$$P_{out_2} = G_2 P_{out_1} \tag{7.11}$$

which can be related to the driver stage input power via the driver stage gain:

$$P_{out_2} = G_1 G_2 P_{in_1} \tag{7.12}$$

Substituting (7.10), (7.11), and (7.12) into (7.7) and simplifying, the cascaded PAE becomes:

$$PAE = \frac{G_2 - \frac{1}{G_1}}{\frac{1}{\eta_{d_1}} + \frac{G_2}{\eta_{d_2}}} \tag{7.13}$$

It may be preferable to find the cascaded PAE in terms of the PAE of each stage. If so, the total DC power can be defined in terms of PAE:

$$P_{DC} = P_{DC_1} + P_{DC_2} = \frac{P_{out_1}}{\eta_{d_1}} + \frac{P_{out_2}}{\eta_{d_2}} = \frac{P_{out_1} - P_{in_1}}{PAE_1} + \frac{P_{out_2} - P_{in_2}}{PAE_2} \tag{7.14}$$

Substituting (7.14), (7.11), and (7.12) into (7.7) and simplifying, the cascaded PAE is found in terms of the PAE of each stage as:

$$PAE = \frac{PAE_1 PAE_2 G_1 G_2 - 1)}{PAE_1 G_1 (G_2 - 1) + PAE_2 (G_1 - 1)} \tag{7.15}$$

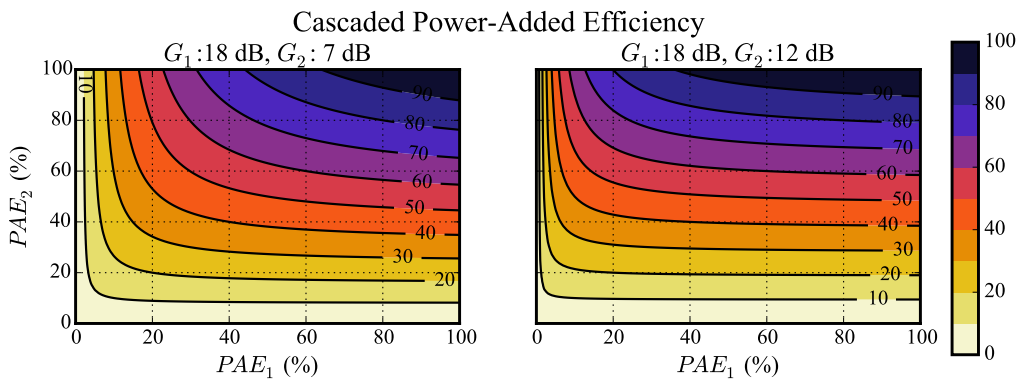


Figure 7.4: Cascaded PAE of the circuit in Fig. 7.2 as a function of the PAE of each stage, shown for 18 dB driver stage gain with 7 and 12 dB output stage gains.

The cascaded power-added efficiency is plotted in Fig. 7.4 as a function of the PAE of each stage for a driver stage gain of 18 dB and output stage gains of 7 and 12 dB. Now, the cascaded efficiency is a function of the gains of both stages. Typically, the driver stage has a higher gain because it is a smaller device and is often operated further from saturation. Given the expected gains of the two stages and the PAE of the output stage, the required PAE of the driver stage can be determined. The amount of influence each stage has on the cascaded efficiency is a function of the relative gain. As the gain of the output stage increases relative to that of the driver stage, the contours in Fig. 7.4 flatten in the right plot compared to the left, decreasing the required driver stage efficiency and increasing the region of high efficiency.

7.2 Bi-Directional Matching

The interstage matching network must perform bi-directional matching between the complex transistor impedances loading the network, as shown in Fig. 7.5. Minimally, the ISMN must match the two transistors at a single frequency for maximum power transfer, as traditionally done. However, for high efficiency, the transistors may be intentionally mismatched at the fundamental and harmonic frequencies, according to source- and load-pull characterization. Therefore, the ISMN must transform the output impedance of the driver stage into the desired reflection coefficient for the output stage, referenced to its impedance, and vice versa. The purpose of this section is to determine if a passive set of S-parameters exist for given complex reference impedances (transistors), which will yield the desired matching or mismatching.

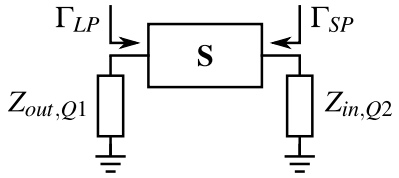


Figure 7.5: High efficiency interstage matching network circuit. $Z_{out,Q1}$ and $Z_{in,Q2}$ are the output and input impedances of the driver and power transistors, respectively.

Aside from proving the existence of valid S-parameters, this analysis provides a couple more uses. The desired S-parameters may be generated for 50 Ω reference impedances, enabling direct comparison with measured S-parameters. Additionally, a synthesized two-port network may be optimized to match the generated 50 Ω S-parameters, in order to achieve the desired performance when loaded with the complex impedance transistors. This analysis could be replicated at harmonic frequencies, providing the required harmonic S-parameters for a given set of terminations, and then synthesized in a circuit.

7.2.1 Change of Reference Impedance

In order to accomplish bi-directional impedance matching, a method for changing the reference impedances of an S-parameter defined network is commandeered from [161]. The authors of this excellent work utilize pseudo-waves, which are a mathematical construct without any physical meaning. Pseudo-waves can help accomplish the goal, but are rather unintuitive. For example, matching to a complex reference impedance does not make the pseudo-wave scattering matrix reflection coefficient zero. Therefore, the method presented in [161] is expanded to utilize power waves [162], which are also utilized by commercially available microwave simulation software. Power waves are also a mathematical construct, like pseudo-waves, but have direct physical meaning, like traveling waves. They are defined at a single port for a given reference impedance, Z_{ref}, as:

$$a(Z_{ref}) = \frac{v + Z_{ref} i}{2\sqrt{\left|\mathrm{Re}\left\{Z_{ref}\right\}\right|}} \tag{7.16}$$

$$b(Z_{ref}) = \frac{v - Z_{ref}^{*} i}{2\sqrt{\left|\mathrm{Re}\left\{Z_{ref}\right\}\right|}} \tag{7.17}$$

where v and i are the total voltage and current, respectively. The inverse relationships to (7.16) and (7.17) are:

$$v = \frac{\rho}{\sqrt{\left|\text{Re}\left\{Z_{ref}\right\}\right|}}\left(Z_{ref}^{*}a + Z_{ref}b\right) \tag{7.18}$$

$$i = \frac{\rho}{\sqrt{\left|\text{Re}\left\{Z_{ref}\right\}\right|}}(a - b) \tag{7.19}$$

where ρ is defined by:

$$\rho = \begin{cases} 1, & \text{when Re}\left\{Z_{ref}\right\} > 0 \\ -1, & \text{when Re}\left\{Z_{ref}\right\} < 0 \end{cases} \tag{7.20}$$

The convenience of the power wave definition is found when examining the available power from a generator, and power transferred from the generator to a load. The available power from a generator can be written as:

$$P_{av} = \rho|a|^2 \tag{7.21}$$

while the power transferred from the generator to the load is found to be:

$$P_L = \text{Re}\left\{vi^*\right\} = \rho\left(|a|^2 - |b|^2\right) \tag{7.22}$$

Clearly, the power wave definitions give an intuitive understanding of the incident, reflected, and transmitted powers. The reflection coefficient for these waves is defined as:

$$\Gamma = \frac{Z_L - Z_{ref}^{*}}{Z_L + Z_{ref}} \tag{7.23}$$

When the complex reference impedance and load impedances are conjugate matched, maximum power transfer occurs, and the reflection coefficient becomes zero.

The method for changing reference impedances of the two-port network is as follows:

(1) Define desired S-parameter matrix, **S**

(2) Convert **S** to the cascade matrix, **R**

(3) Multiply **R** by change of reference impedance matrices, **P**, on both sides

(4) Convert **R** with changed reference impedances back to **S**

First, the desired two-port network, **S**, must be defined by:

$$\begin{bmatrix} b_1\left(Z_{ref}^{i}\right) \\ b_2\left(Z_{ref}^{j}\right) \end{bmatrix} = \mathbf{S}^{ij} \begin{bmatrix} a_1\left(Z_{ref}^{i}\right) \\ a_2\left(Z_{ref}^{j}\right) \end{bmatrix} \tag{7.24}$$

where,

$$\mathbf{S}^{ij} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{7.25}$$

The matrix values are chosen for the function of the matching network, matched or intentionally mismatched. If mismatching the ports based on the source- and load-pull, the optimal impedances must be referenced to the proper impedances, Z_{ref}^{i} and Z_{ref}^{j}.

Next, the desired **S** is converted to the cascade matrix **R**, which relates the power waves as:

$$\begin{bmatrix} b_1\left(Z_{ref}^{i}\right) \\ a_1\left(Z_{ref}^{i}\right) \end{bmatrix} = \mathbf{R}^{ij} \begin{bmatrix} a_2\left(Z_{ref}^{j}\right) \\ b_2\left(Z_{ref}^{j}\right) \end{bmatrix} \tag{7.26}$$

The indices in the superscript of $\mathbf{R}^{ij}$ indicate that the reference impedance at port 1 is Z_{ref}^{i} and at port 2 is Z_{ref}^{j}. The general conversion between scattering and cascade matrices are:

$$\mathbf{R} = \frac{1}{S_{21}} \begin{bmatrix} S_{12}S_{21} - S_{11}S_{22} & S_{11} \\ -S_{22} & 1 \end{bmatrix} \tag{7.27}$$

and

$$\mathbf{S} = \frac{1}{R_{22}} \begin{bmatrix} R_{12} & R_{11}R_{22} - R_{12}R_{21} \\ 1 & -R_{21} \end{bmatrix} \tag{7.28}$$

Since the cascade matrix separates the power waves of each port, reference impedance transformations can be implemented by a matrix multiplication on each side. This transformation can be derived using the power wave, total voltage, and total current definitions. By expressing $a(Z_{ref}^{j})$ and $b(Z_{ref}^{j})$ in terms of v and i using (7.16) and (7.17), and v and i in terms of $a(Z_{ref}^{m})$ and $b(Z_{ref}^{m})$ using (7.18) and (7.19), a linear relationship between the power waves for each reference impedance is found:

$$\begin{bmatrix} a\left(Z_{ref}^{j}\right) \\ b\left(Z_{ref}^{j}\right) \end{bmatrix} = \mathbf{P}^{jm} \begin{bmatrix} a\left(Z_{ref}^{m}\right) \\ b\left(Z_{ref}^{m}\right) \end{bmatrix} \tag{7.29}$$

where

$$\mathbf{P}^{jm} \equiv \begin{bmatrix} P_{11} & P_{12} \\ P_{21} & P_{22} \end{bmatrix} = \frac{1}{2\sqrt{\mathrm{Re}\left\{Z^j_{ref}\right\}}\sqrt{\mathrm{Re}\left\{Z^m_{ref}\right\}}} \begin{bmatrix} Z^j_{ref} + Z^{m*}_{ref} & Z^m_{ref} - Z^j_{ref} \\ Z^{m*}_{ref} - Z^{j*}_{ref} & Z^{j*}_{ref} + Z^m_{ref} \end{bmatrix} \tag{7.30}$$

This equation provides the exact expression of the complex impedance transform. The reference impedance of port 2 can be transformed by substituting (7.29) into the right hand side of (7.26), yielding:

$$\begin{bmatrix} b_1\left(Z^i_{ref}\right) \\ a_1\left(Z^i_{ref}\right) \end{bmatrix} = \mathbf{R}^{ij}\mathbf{P}^{jm} \begin{bmatrix} a_2\left(Z^m_{ref}\right) \\ b_2\left(Z^m_{ref}\right) \end{bmatrix} \tag{7.31}$$

The impedance transformation on port 1 is more complicated. In order to substitute into the left hand side of (7.26), the vectors in (7.29) must be flipped. First, take the two equations held in (7.29):

$$a\left(Z^j_{ref}\right) = P_{11}a\left(Z^m_{ref}\right) + P_{12}b\left(Z^m_{ref}\right) \tag{7.32}$$

$$b\left(Z^j_{ref}\right) = P_{21}a\left(Z^m_{ref}\right) + P_{22}b\left(Z^m_{ref}\right) \tag{7.33}$$

Rewriting this to flip the vectors yields:

$$b\left(Z^j_{ref}\right) = P_{22}b\left(Z^m_{ref}\right) + P_{21}a\left(Z^m_{ref}\right) \tag{7.34}$$

$$a\left(Z^j_{ref}\right) = P_{12}b\left(Z^m_{ref}\right) + P_{11}a\left(Z^m_{ref}\right) \tag{7.35}$$

Unlike the case for the pseudo-wave transformation matrix, $\mathbf{Q}$, in [161], $\mathbf{P}$ is not symmetric. It is clear from (7.30), that $P_{11} = P^*_{22}$ and $P_{12} = P^*_{21}$. The expression relating the flipped vectors can be written simply as:

$$\begin{bmatrix} b\left(Z^j_{ref}\right) \\ a\left(Z^j_{ref}\right) \end{bmatrix} = \mathbf{P}^{jm*} \begin{bmatrix} b\left(Z^m_{ref}\right) \\ a\left(Z^m_{ref}\right) \end{bmatrix} \tag{7.36}$$

Now the left hand side of (7.31) can be replaced by (7.36) with the indices i and p, yielding:

$$\mathbf{P}^{ip*} \begin{bmatrix} b_1\left(Z^p_{ref}\right) \\ a_1\left(Z^p_{ref}\right) \end{bmatrix} = \mathbf{R}^{ij}\mathbf{P}^{jm} \begin{bmatrix} a_2\left(Z^m_{ref}\right) \\ b_2\left(Z^m_{ref}\right) \end{bmatrix} \tag{7.37}$$

Then, $\mathbf{P}^{ip*}$ can be moved to the right hand side by multiplying both sides by its inverse:

$$[\mathbf{P}^{ip*}]^{-1}\mathbf{P}^{ip} \begin{bmatrix} b_1\left(Z^p_{ref}\right) \\ a_1\left(Z^p_{ref}\right) \end{bmatrix} = [\mathbf{P}^{ip*}]^{-1}\mathbf{R}^{ij}\mathbf{P}^{jm} \begin{bmatrix} a_2\left(Z^m_{ref}\right) \\ b_2\left(Z^m_{ref}\right) \end{bmatrix} \tag{7.38}$$

Since,

$$\mathbf{P}^{nn*} = \mathbf{I} \tag{7.39}$$

where $\mathbf{I}$ is the identity matrix, the following is true:

$$[\mathbf{P}^{nm*}]^{-1} = \mathbf{P}^{mn*} \tag{7.40}$$

Now, (7.38) can be simplified to:

$$\begin{bmatrix} b_1\left(Z^p_{ref}\right) \\ a_1\left(Z^p_{ref}\right) \end{bmatrix} = \mathbf{P}^{pi*}\mathbf{R}^{ij}\mathbf{P}^{jm} \begin{bmatrix} a_2\left(Z^m_{ref}\right) \\ b_2\left(Z^m_{ref}\right) \end{bmatrix} \tag{7.41}$$

Finally, yielding the transformed cascade matrix:

$$\mathbf{R}^{pm} = \mathbf{P}^{pi*}\mathbf{R}^{ij}\mathbf{P}^{jm} \tag{7.42}$$

Lastly, the new cascade matrix $\mathbf{R}^{pm}$ can be converted back to an S-parameter matrix $\mathbf{S}^{pm}$ using (7.28).

7.2.2 Conjugate Match Example

First, an example showing the existence of S-parameters to perform simultaneous complex matching on the two complex impedance ports without loss is shown. The desired S-parameter matrix is chosen to be matched, lossless, and reciprocal:

$$\mathbf{S}^{ij} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \tag{7.43}$$

The cascade matrix is made by converting $\mathbf{S}^{ij}$ to $\mathbf{R}^{ij}$ and filling in the $\mathbf{P}$ matrices in (7.42) with the following values chosen for this example:

$$Z^p_{ref} = Z_0 = 50\,\Omega \tag{7.44}$$

$$Z^i_{ref} = Z_{ref,1} = 10 + j10\,\Omega \tag{7.45}$$

$$Z^j_{ref} = Z_{ref,2} = 75 + j25\,\Omega \tag{7.46}$$

$$Z^m_{ref} = Z_0 = 50\,\Omega \tag{7.47}$$

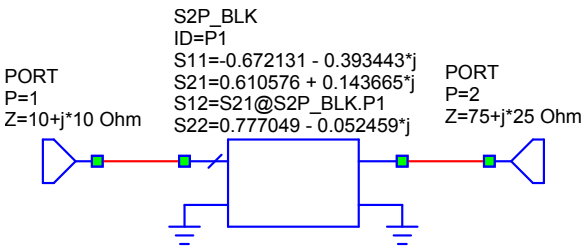


Figure 7.6: AWR simulation setup demonstrating validity of derived 50 Ω S-parameters for achieving desired complex conjugate match.

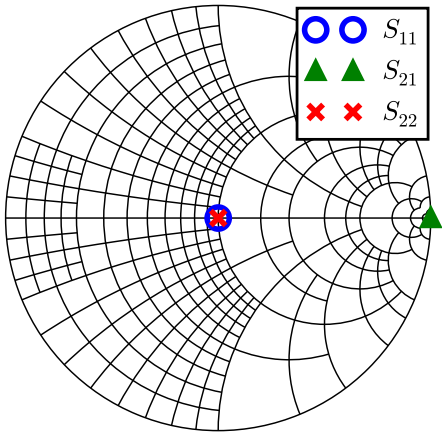


Figure 7.7: AWR simulation results demonstrating validity of derived 50 Ω S-parameters for achieving desired complex conjugate match.

Converting $\mathbf{R}^{pm}$ to $\mathbf{S}^{pm}$ yields:

$$\mathbf{S}^{pm} = \begin{bmatrix} -0.672131 - j0.393443 & 0.610576 + j0.143665 \\ 0.610576 + j0.143665 & 0.777049 - j0.052459 \end{bmatrix} \tag{7.48}$$

This matrix is the required 50 Ω scattering matrix to achieve the desired scattering when loaded with the complex reference impedances. $\mathbf{S}^{pm}$ is entered into the S2P_BLK component in the NI AWR Microwave Office simulator as shown in Fig. 7.6. The simulated results in Fig. 7.7 confirm the desired response.

7.2.3 Intentional Mismatch Example

Now, an example showing the existence of S-parameters to perform simultaneous mismatching on the two complex impedance ports without loss will be shown. This is the desired performance at the fundamental

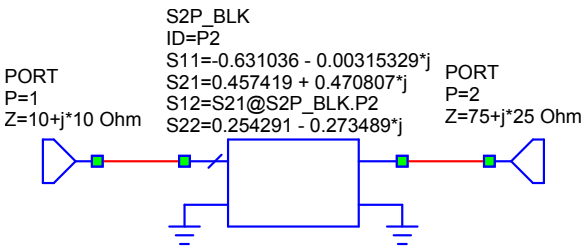


Figure 7.8: AWR simulation setup demonstrating validity of derived 50 Ω S-parameters for achieving desired mismatch.

frequency for the designed ISMN. The desired S-parameter matrix is chosen to be mismatched, lossless, and reciprocal:

$$\mathbf{S}^{ij} = \begin{bmatrix} 0.6\,e^{j60^\circ} & 0.8 \\ 0.8 & 0.6\,e^{j210^\circ} \end{bmatrix} \tag{7.49}$$

The cascade matrix is made by converting $\mathbf{S}^{ij}$ to $\mathbf{R}^{ij}$ and filling in the $\mathbf{P}$ matrices in (7.42) with the following values chosen for this example:

$$Z^{p}_{ref} = Z_0 = 50\,\Omega \tag{7.50}$$

$$Z^{i}_{ref} = Z_{ref,1} = 10 + j10\,\Omega \tag{7.51}$$

$$Z^{j}_{ref} = Z_{ref,2} = 75 + j25\,\Omega \tag{7.52}$$

$$Z^{m}_{ref} = Z_0 = 50\,\Omega \tag{7.53}$$

Converting $\mathbf{R}^{pm}$ to $\mathbf{S}^{pm}$ yields:

$$\mathbf{S}^{pm} = \begin{bmatrix} -0.631036 - j0.00315329 & 0.457419 + j0.470807 \\ 0.457419 + j0.470807 & 0.254291 - j0.273489 \end{bmatrix} \tag{7.54}$$

This matrix is the required 50 Ω S-parameters to achieve the desired S-parameters when loaded with the complex reference impedances. $\mathbf{S}^{pm}$ is simulated as shown in Fig. 7.8, with the results in Fig. 7.9. The network provides the desired reflection coefficient to each port, or transistor in the case of an ISMN.

7.3 Harmonically Terminated Interstage Matching Networks

Many techniques for synthesizing a circuit exist [163, 164]. One approach could be to generate a transfer function based on the desired harmonic frequency S-parameters generated by the method in the previous

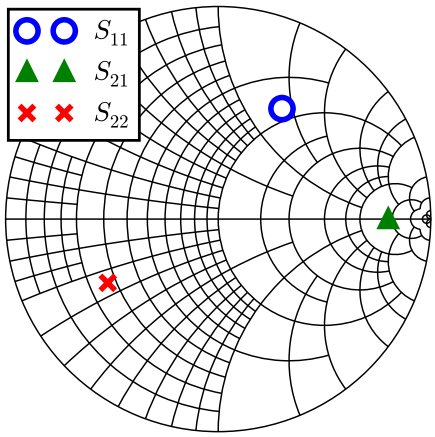


Figure 7.9: AWR simulation results demonstrating validity of derived 50 Ω S-parameters for achieving desired mismatch.

section. This transfer function could be realized by a circuit using a number of commercially available synthesis tools. Unfortunately, these tools are typically oriented toward filters and not well suited for matching to complex impedances.

Several works have sought to analytically find both lumped element [165, 166] and transmission line [167, 168] circuit implementations for class-F and inverse class-F output matching networks. These works are leveraged to derive a number of harmonically terminated interstage matching networks. The difference between the OMN and ISMN is the bi-directionality, meaning the harmonic terminations must be properly phased at both ports of the network, while bi-directional fundamental impedance matching occurs. The following analyses are referenced to the intrinsic drain, thus ignoring transistor parasitics and treating transistors as resistive loads. When parasitics are present, they must either be resonated, or more likely, the phase of each harmonic termination will need to be adjusted via series elements between resonators.

In the following subsections, eleven networks are provided as starting points for any harmonically terminated ISMN implementation. First, six lumped element networks that provide class-F (short circuit at $2f_0$, open circuit at $3f_0$) and inverse class-F (open circuit at $2f_0$, short circuit at $3f_0$) harmonic terminations to both ports are presented (three each). Next, five transmission line networks are derived, presenting class-F,

inverse class-F, and arbitrary phase harmonic terminations to each transistor. The aim of this work is to provide a starting point for implementing a harmonically terminated ISMN.

7.3.1 Lumped Element ISMNs

To generate these networks, the placement of resonators is first devised. These resonators are comprised of an inductor and capacitor with its subscript corresponding to the harmonic of its resonance. For example, C_2 and L_2 resonate at the second harmonic. Next, the network is examined at the fundamental and harmonic frequencies. To accomplish this, the characteristics of each resonator at frequencies of interest outside of resonance must be known. The value of the dominant element, which is designated with a prime superscript ($'$), of both series and parallel resonators at frequencies outside of resonance are provided in Appendix A. Finally, equations can be written based on the harmonic frequency circuits and desired terminations to constrain the element values, while leaving two degrees of freedom for performing fundamental matching for each network.

7.3.1a Class-F

The first class-F network makes use of series resonators, and is shown in Fig. 7.10a, along with the equivalent networks at the fundamental and harmonic frequencies in Figs. 7.10b, 7.10c, and 7.10d. Looking at the network at harmonic frequencies, the constraints take form. The resonant frequency of the series resonators contrains the capacitor in each, while the inductor is left as a degree of freedom for fundamental matching, since the quality factor is proportional to the inductor, yielding the following constraints:

$$C_2 = \frac{1}{(2\omega_2)^2 L_2} \tag{7.55}$$

$$C_3 = \frac{1}{(3\omega_3)^2 L_3} \tag{7.56}$$

where ω_1 is designated as the fundamental frequency in radians per second. At the second harmonic, the short circuits are in parallel with some capacitive load, and if the quality factor of the $2f_0$ resonators is high enough, then a short circuit will be enforced. At the third harmonic, L_2', which is the dominant inductance value of the $2f_0$ resonator, must resonate with C in parallel to provide an open circuit. The value of L_2' can

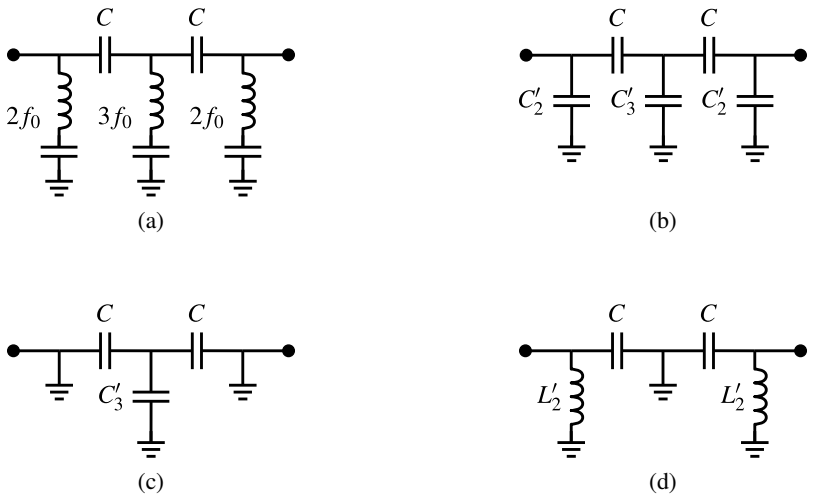


Figure 7.10: Class-F ISMN utilizing series resonators. (a) Circuit diagram, and equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

be found from:

$$L_2' = \frac{(\omega^2 - \omega_0^2)L_2}{\omega^2} = \frac{(x^2-1)L_2}{x} \tag{7.57}$$

where $x = 3/2$, since it is the value of the second harmonic resonator at the third harmonic. Then, C is forced to resonate with L_2' at $3f_0$:

$$C = \frac{1}{(3\omega_3)^2 L_2'} \tag{7.58}$$

Now, three of the five component values are constrained to the remaining two, which are free to perform fundamental impedance matching.

Another class-F network makes use of parallel resonators, as shown in Fig. 7.11a, along with the equivalent networks at the fundamental and harmonic frequencies in Figs. 7.11b, 7.11c, and 7.11d. In this case, the capacitors in each resonator are available to optimize for fundamental matching, since their values are proportional to the quality factors. This yields the following constraints:

$$L_2 = \frac{1}{(2\omega_2)^2 C_2} \tag{7.59}$$

$$L_3 = \frac{1}{(3\omega_3)^2 C_3} \tag{7.60}$$

At the third harmonic, the parallel $3f_0$ resonators provide the open circuit. At the second harmonic, the shunt capacitance must resonate with the sub-resonant inductance of the parallel $3f_0$ resonator, which can

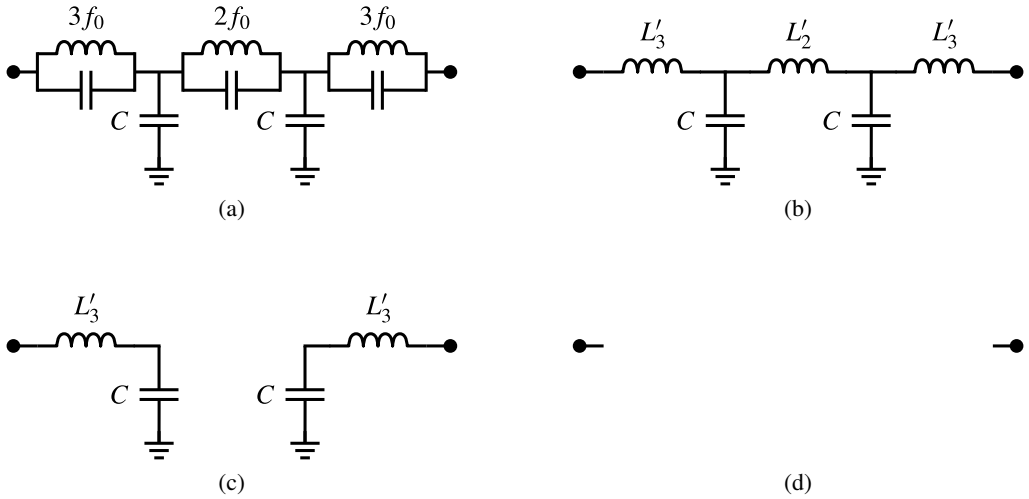


Figure 7.11: Class-F ISMN utilizing parallel resonators (a) Circuit diagram, and equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

be found by:

$$L_3' = \frac{\omega_0^2 L_3}{\omega_0^2 - \omega^2} = \frac{L_3}{1 - x^2} \tag{7.61}$$

where $x = 2/3$, since it is the value of the third harmonic resonator at the second harmonic. Then, C can be found from:

$$C = \frac{1}{(2\omega_2)^2 L_3'} \tag{7.62}$$

The third class-F network makes use of both parallel and series resonators, and is shown in Fig. 7.12a, along with the equivalent networks at the fundamental and harmonic frequencies in Figs. 7.12b, 7.12c, and 7.12d. This time, the capacitor in the $3f_0$ resonator and the inductor in the $2f_0$ resonator are the degrees of freedom for fundamental matching, as their values are proportional to the quality factor of their respective resonators. This yields the following constraints:

$$C_2 = \frac{1}{(2\omega_2)^2 L_2} \tag{7.63}$$

$$L_3 = \frac{1}{(3\omega_3)^2 C_3} \tag{7.64}$$

At the third harmonic, the parallel $3f_0$ resonators provide the open circuit, as in the previous network. At the second harmonic, the shunt resonator provides a short circuit in the center of the network. Thus, the

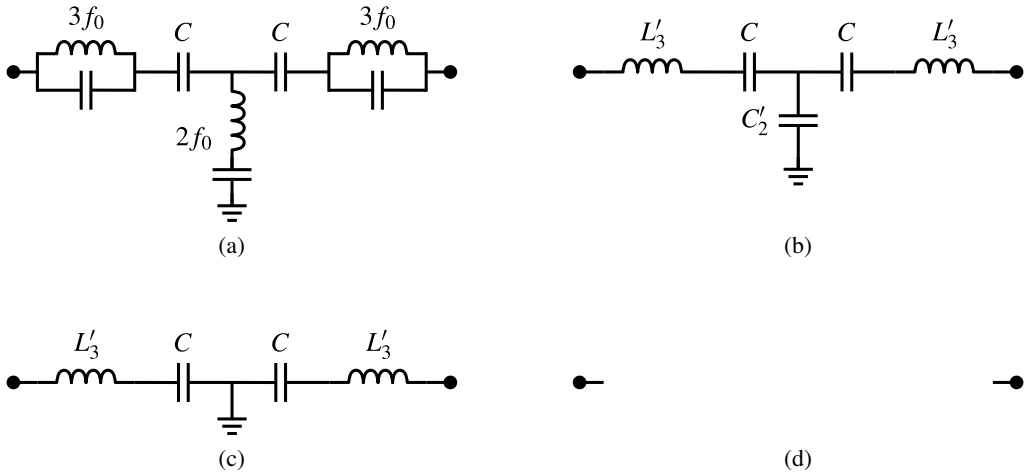


Figure 7.12: Class-F ISMN utilizing both series and parallel resonators. (a) Circuit diagram. Equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

capacitance must resonate with the sub-resonant inductance of the parallel $3f_0$ resonator, which can be found by:

$$L_3' = \frac{\omega_0^2 L_3}{\omega_0^2 - \omega^2} = \frac{L_3}{1 - x^2} \tag{7.65}$$

where $x = 2/3$, since it is the value of the third harmonic resonator at the second harmonic. Then, C can be found from:

$$C = \frac{1}{(2\omega_2)^2 L_3'} \tag{7.66}$$

7.3.1b Inverse Class-F

The first inverse class-F network makes use of series resonators, and is shown in Fig. 7.13a, along with the equivalent networks at the fundamental and harmonic frequencies in Figs. 7.13b, 7.13c, and 7.13d. The value of inductors will not be constrained, in order to perform fundamental matching, since the quality factor is proportional to their value, yielding the following constraints on the capacitors:

$$C_2 = \frac{1}{(2\omega_2)^2 L_2} \tag{7.67}$$

$$C_3 = \frac{1}{(3\omega_3)^2 L_3} \tag{7.68}$$

At the third harmonic, the series resonators provide short circuits at the transistor terminals. If the quality factor of the $3f_0$ resonators is high enough, then the inductive parallel load will not have a significant effect.

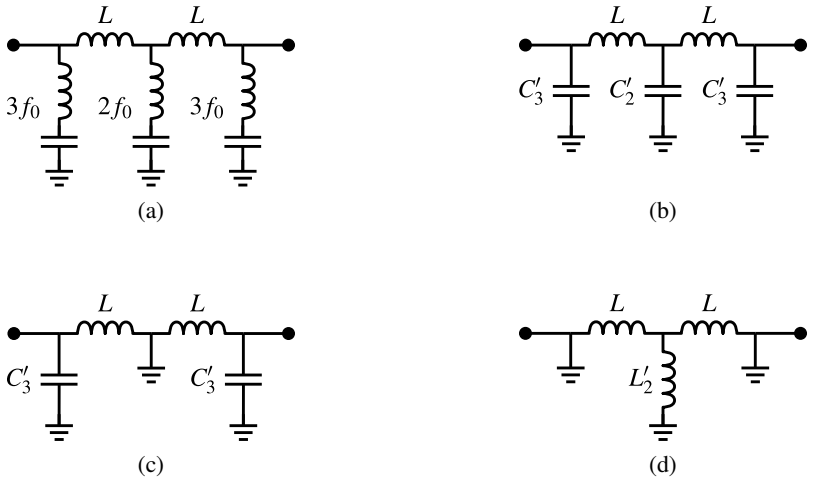


Figure 7.13: Inverse class-F ISMN utilizing series resonators. (a) Circuit diagram, and equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

At the second harmonic, the sub-resonant capacitance C_3' of the series $3f_0$ resonator must resonate with L in parallel to provide an open circuit. The value of C_3' can be found from:

$$C_3' = \frac{\omega_0^2 C_3}{\omega_0^2 - \omega^2} = \frac{C_3}{1 - x^2} \tag{7.69}$$

where $x = 2/3$, since it is the value of the third harmonic resonator at the second harmonic. Then, L can be found from:

$$L = \frac{1}{(3\omega_2)^2 C_2'} \tag{7.70}$$

Another inverse class-F network makes use of parallel resonators, and is shown in Fig. 7.14a, along with the equivalent networks at the fundamental and harmonic frequencies in Figs. 7.14b, 7.14c, and 7.14d. In this case, the capacitors in each resonator are left free to optimize for fundamental matching, since their value is proportional to the quality factor. This yields the following constraints:

$$L_2 = \frac{1}{(2\omega_2)^2 C_2} \tag{7.71}$$

$$L_3 = \frac{1}{(3\omega_3)^2 C_3} \tag{7.72}$$

At the second harmonic, the parallel $2f_0$ resonators provide the open circuit. At the third harmonic, the shunt inductance must resonate with the super-resonance capacitance of the parallel $2f_0$ resonator, which

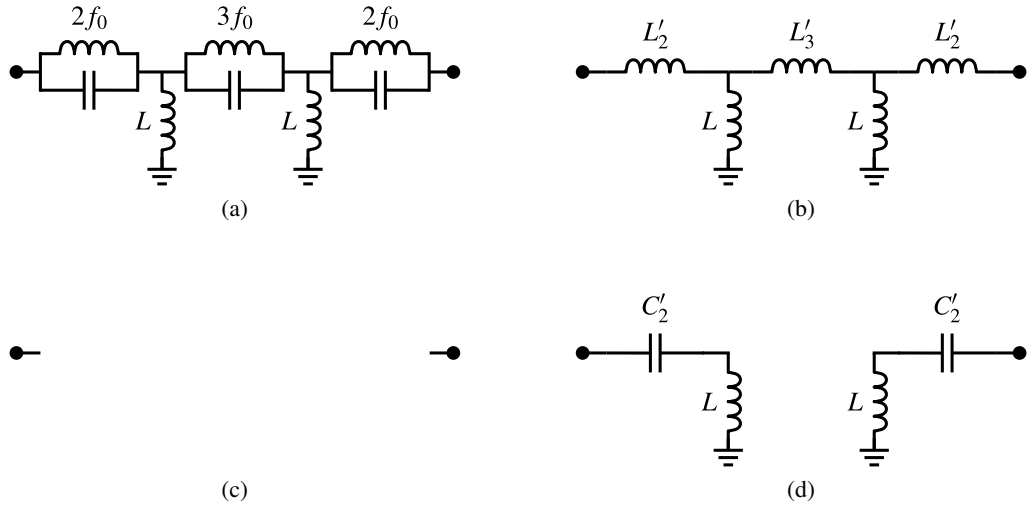


Figure 7.14: Inverse class-F ISMN utilizing parallel resonators. (a) Circuit diagram, and quivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

can be found by:

$$C_2' = \frac{(\omega - \omega_0^2)C_2}{\omega^2} = \frac{(x^2 - 1)C_2}{x^2} \tag{7.73}$$

where $x = 3/2$, since it is the value of the second harmonic resonator at the third harmonic. Then, L can be found from:

$$L = \frac{1}{(3\omega_3)^2 C_2'} \tag{7.74}$$

The third inverse class-F network makes use of both parallel and series resonators, and is shown in Fig. 7.15a, along with the equivalent networks at the fundamental and harmonic frequencies in Figs. 7.15b, 7.15c, and 7.15d. This time, the inductor in the $3f_0$ resonator and the capacitor in the $2f_0$ resonator are the degrees of freedom for fundamental matching, as their values are proportional to the quality factor of their resonators. This yields the following constraints:

$$L_2 = \frac{1}{(2\omega_2)^2 C_2} \tag{7.75}$$

$$C_3 = \frac{1}{(3\omega_3)^2 L_3} \tag{7.76}$$

At the second harmonic, the parallel $2f_0$ resonators provide the open circuit. At the third harmonic, the shunt series resonator provides a short circuit in the center of the network, according to its quality factor. In

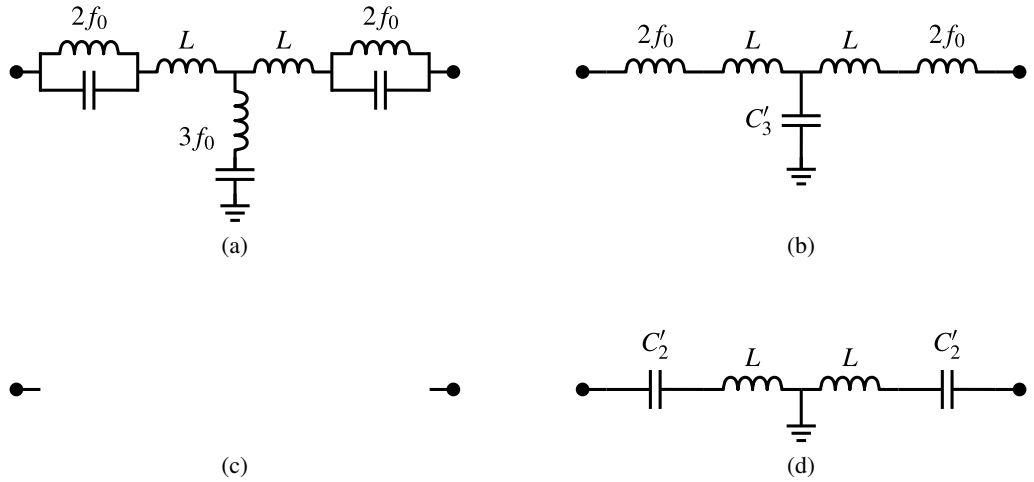


Figure 7.15: Inverse class-F ISMN utilizing both series and parallel resonators. (a) Circuit diagram, and equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

order to transfer this short circuit to the transistor terminals, the shunt inductance L must resonate with the super-resonant capacitance C_2' of the parallel $2f_0$ resonator, which can be found by:

$$C_2' = \frac{(\omega - \omega_0^2)C_2}{\omega^2} = \frac{(x^2 - 1)C_2}{x^2} \tag{7.77}$$

where $x = 3/2$, since it is the value of the second harmonic resonator at the third harmonic. Then, L can be found from:

$$L = \frac{1}{(3\omega_3)^2 C_2'} \tag{7.78}$$

For each network, three of the five component values are constrained by harmonic termination criteria. The remaining two components are optimized to match the fundamental impedances. During optimization for fundamental matching, reduction in the values of the two free components will lead to a decreased quality factor in the resonators and could reduce the effectiveness of the harmonic terminations.

7.3.2 Transmission Line ISMNs

The concepts behind the derivation of lumped element ISMNs is now extended to consider transmission line implementations. The placement of harmonic short circuits is first devised, then the network is analyzed at the fundamental and harmonic frequencies for component constraints. In most cases, the harmonic terminations are enforced only by the electrical lengths of the lines, otherwise conditions for their characteristic impedances

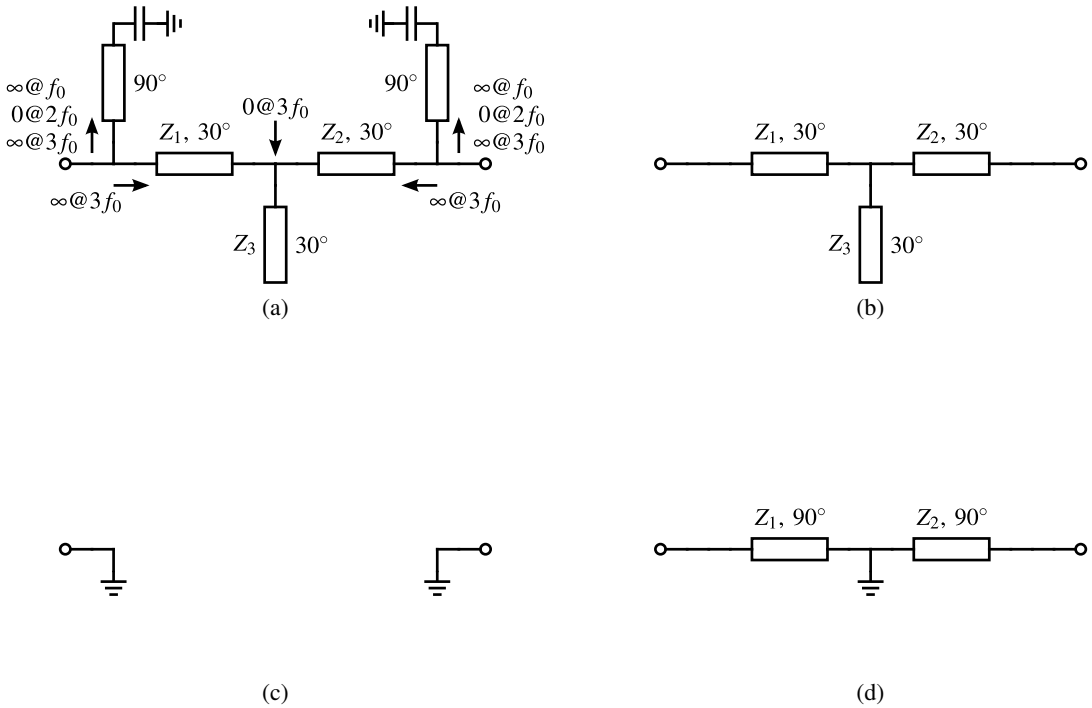


Figure 7.16: (a) Class-F ISMN circuit diagram. Equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

must also be solved. In all cases, the characteristic impedances of some or all of the transmission lines are free to perform fundamental matching. In the following subsections, two class-F ISMNs, two inverse class-F ISMNs, and an arbitrary phase ISMNs are analyzed.

7.3.2A Class-F

The first class-F network utilizes two RF shorted 90° transmission lines to simultaneously terminate the second harmonic and provide DC biasing to each transistor. An open circuit stub provides the third harmonic termination, as shown in Fig. 7.16a. The equivalent networks at the fundamental and harmonic frequencies are shown in Figs. 7.16b, 7.16c, and 7.16d.

This particular network fixes the harmonic terminations through the electrical length of each TL, independent of the characteristic impedances. At the fundamental frequency in Fig. 7.16b, the characteristic impedances of the single stub network are optimized for fundamental matching, because the bias lines appear as high impedances and do not affect the fundamental impedance. At the second harmonic in Fig. 7.16c, the 90° bias line is effectively 180°, transforming the RF short circuit into an RF short circuit, which must have

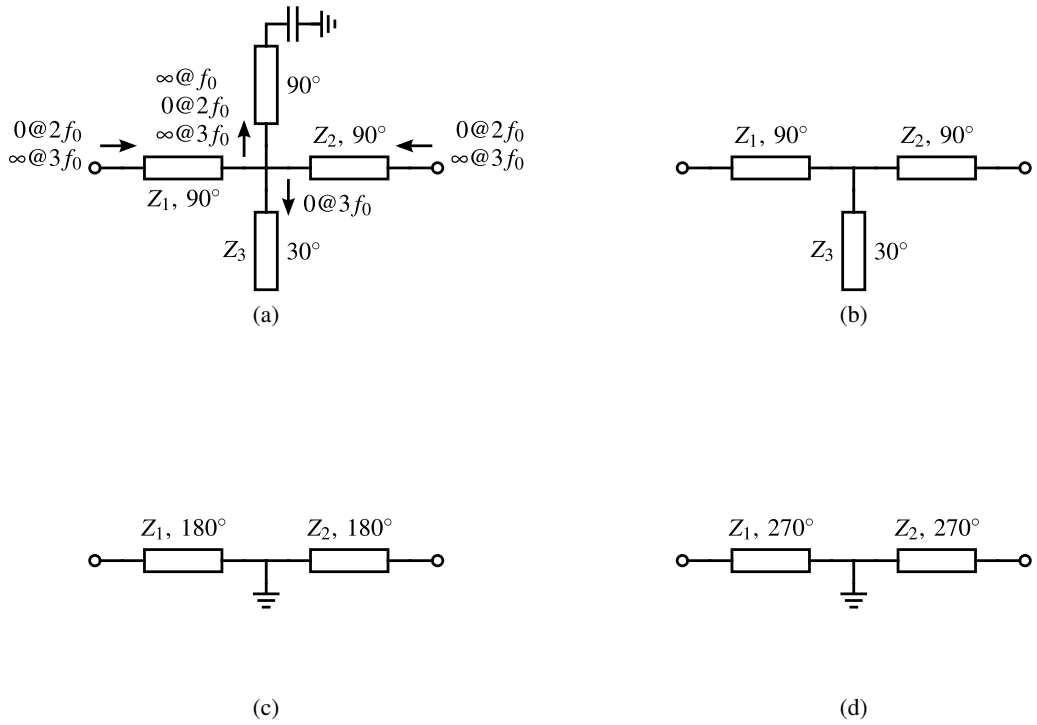


Figure 7.17: (a) Class-F ISMN circuit diagram. Equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

a high enough quality factor so as to short the parallel impedance of the transformed shunt stub. At the third harmonic, the 30° stub is effectively 90°, transforming the open circuit into a short circuit at the center node. The 30° series TLs are effectively 90°, and transform this short circuit to an open circuit at each transistor.

Although the second class-F network has only a single bias line, a second 90° shorted stub could be added without affecting RF performance (if it is ideal) directly at either device. This circuit utilizes the same elements as the previous one, as shown in Fig. 7.17, along with the equivalent networks at the fundamental and harmonic frequencies in Figs. 7.17b, 7.17c, and 7.17d.

This network also fixes the harmonic terminations through the electrical length of each TL, independent of the characteristic impedances. At the fundamental frequency in Fig. 7.17b, the characteristic impedances of the single stub network are optimized for fundamental matching, since the bias line appears as a high impedance, and does not affect the fundamental impedance. Again, the 90° short and 30° open circuit stubs provide short circuits at the second and third harmonics, respectively. The 90° series TLs are effectively 180° and 270° at the second and third harmonics, transforming the short circuits at the center node to short

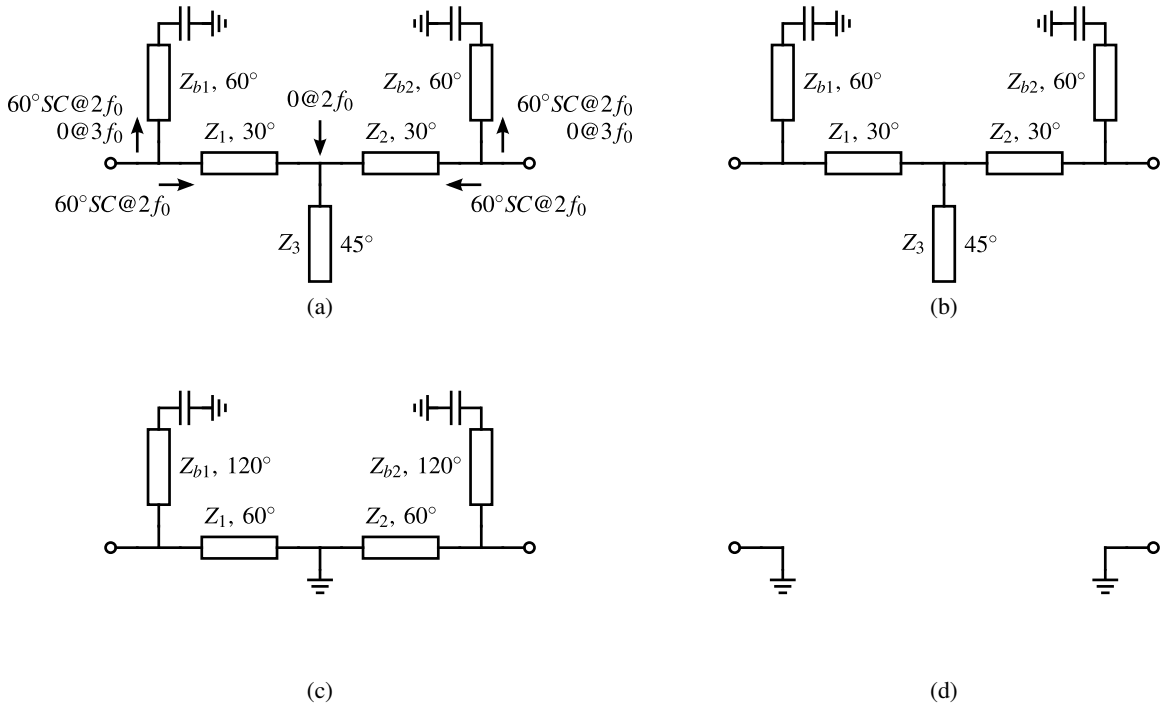


Figure 7.18: (a) Inverse class-F ISMN circuit diagram. Equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

and open circuits, respectively, at each transistor.

7.3.2B Inverse Class-F

The first inverse class-F network, shown in Fig. 7.18a, is slightly more complicated than the class-F ISMNs. The 90° shorted TLs (bias lines) from the first class-F ISMN are shortened to 60°, and the 30° open circuit stub is extended to 45°. In this analysis, only the left side of the network is examined, since the network is symmetric and equations describing the right side are equivalent. At the fundamental frequency in Fig. 7.18b, all TLs are used to perform matching. At the second harmonic in Fig. 7.18c, the 45° open circuit stub is effectively 90°, transforming the open to a short circuit at the center node. From either transistor, the impedance at the second harmonic is the parallel combination of two shorted TLs, 60° and 120° in electrical length, whose input impedances are:

$$Z_{in}(60^\circ) = jZ_1 \tan(60^\circ) = jZ_1\sqrt{3} \tag{7.79}$$

$$Z_{in}(120^\circ) = jZ_{b1} \tan(120^\circ) = -jZ_{b1}\sqrt{3} \tag{7.80}$$

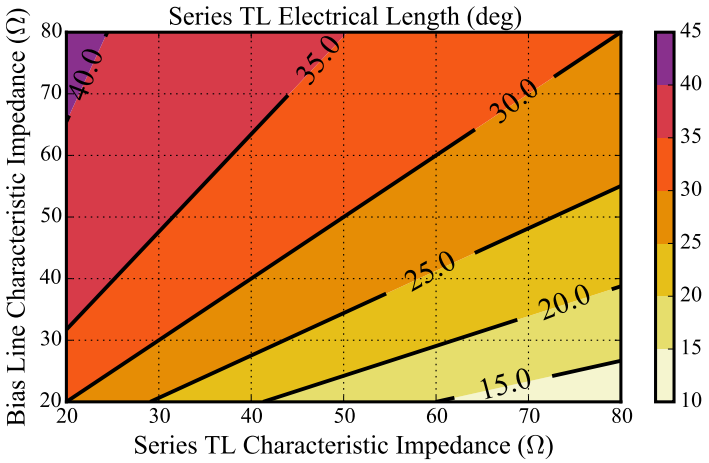


Figure 7.19: Required relationship for second harmonic open circuit termination for first inverse class-F ISMN.

The impedance seen by the device is the parallel combination:

$$Z_{in} = \frac{(jZ_1\sqrt{3})(-jZ_{b1}\sqrt{3})}{jZ_1\sqrt{3} - jZ_{b1}\sqrt{3}} = \frac{3Z_1Z_{b1}}{j\sqrt{3}(Z_1 - Z_{b1})} \tag{7.81}$$

which is infinite when the characteristic impedances of the two TLs are equal, $Z_1 = Z_{b1}$. Of course, if the characteristic impedances are very close, then the impedance can be sufficiently large. The 30° electrical length of the series TL could be adjusted (θ_1) to allow for unequal TL impedances, $Z_1 \neq Z_{b1}$. If the input impedance of the series TL is written more generally:

$$Z_{in}(2\theta_1) = jZ_1\tan(2\theta_1) \tag{7.82}$$

The impedance seen by the device can be written as:

$$Z_{in} = \frac{(jZ_1\tan(2\theta_1))(-jZ_{b1}\sqrt{3})}{jZ_1\tan(2\theta_1) - jZ_{b1}\sqrt{3}} = \frac{Z_1Z_{b1}\sqrt{3}\tan(2\theta_1)}{j\left(Z_1\tan(2\theta_1) - Z_{b1}\sqrt{3}\right)} \tag{7.83}$$

which will be infinite when:

$$Z_1\tan(2\theta_1) = Z_{b1}\sqrt{3} \tag{7.84}$$

This relationship is plotted graphically in Fig. 7.19, where the characteristic impedances of the two TLs are defined from 20 Ω to 80 Ω on the axes, and the color corresponds to the required series TL electrical length. Two of these three values can be utilized to perform fundamental matching, along with the characteristic

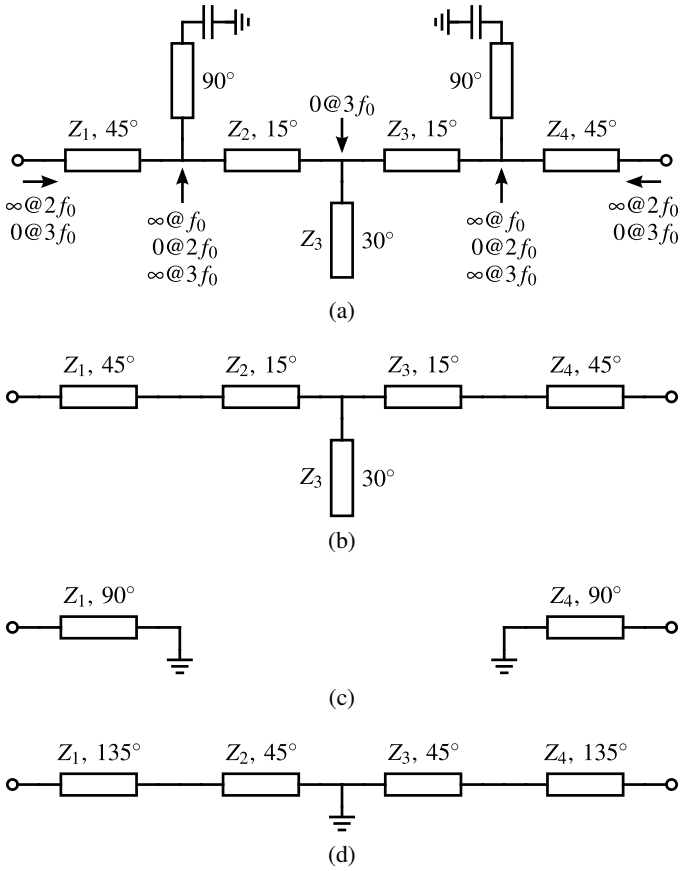


Figure 7.20: (a) Inverse class-F ISMN circuit diagram. Equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

impedance of the open circuit stub. At the third harmonic in Fig. 7.18d, the 60° shorted stubs (bias lines) are effectively 180°, presenting a short circuit to the transistor.

The second inverse class-F network, shown in Fig. 7.20a, is a slightly modified version of the first class-F network. At the fundamental frequency in Fig. 7.20b, the characteristic impedances of the single stub TLs are optimized to perform matching. At the second harmonic in Fig. 7.20c, the 90° shorted TLs (bias lines) are 180° and translate the short circuit to the series path. The series 45°TL is effectively 90° and converts the short circuit to an open circuit. At the third harmonic in Fig. 7.17d, the 30° TL is effectively 90°, transforming the open circuit to a short circuit at the center node. The shunt 90° bias line is 270°and transforms the short circuit to an open circuit, so it does not affect matching. A total series electrical length of 180° translates the short circuit at the center node to each transistor, provided that the characteristic impedances of the two series TLs are equal. If those two impedances differ, the transformation gets a little more complicated, as

will be seen in the case for arbitrary phase harmonic terminations.

7.3.2c Arbitrary Phase Harmonic Terminations

The arbitrary phase network, shown in Fig. 7.21a, is especially useful for design with packaged devices. Often, access to the intrinsic drain is not available for packaged device models, so optimization of harmonic termination phases can be performed at the package reference plane. In this case, the arbitrary phase harmonically terminated ISMN allows direct design for the given, non-classified, harmonic terminations. The 90° shorted TLs (bias lines) provide a short circuit at the second harmonic, while the 30° stub provides a short circuit at the center node at the third harmonic. The electrical lengths of the four series TLs can be solved to enforce the desired phase of the second and third harmonic terminations presented to each device, independently. Afterward, the characteristic impedances of the TLs can be optimized to perform fundamental matching. The analysis below leaves out the left/right distinction to for brevity.

From Fig. 7.21c, the input impedance at the second harmonic can be written as:

$$Z_{in}(2f_0) = jZ_1 \tan(2\theta_1) \tag{7.85}$$

The reflection coefficient is defined only for a purely real reference impedance as:

$$\Gamma_{in}(2f_0) = \frac{Z_{in} - R_{ref}}{Z_{in} + R_{ref}} = \frac{Z_1^2 \tan^2(2\theta_1) - R_{ref}^2 + j2R_{ref}Z_1 \tan(2\theta_1)}{R_{ref}^2 + Z_1^2 \tan^2(2\theta_1)} \tag{7.86}$$

Solving for the phase of the reflection coefficient yields:

$$\phi_{2f_0} = \angle\Gamma_{in} = \arctan\left(\frac{2R_{ref}Z_1 \tan(2\theta_1)}{Z_1^2 \tan^2(2\theta_1) - R_{ref}^2}\right) \tag{7.87}$$

Constraining θ_1:

$$\theta_1 = \frac{1}{2}\left[\arctan\left(\frac{R_{ref}\cot\left(\frac{\phi_{2f_0}}{2}\right)}{Z_1}\right) + \pi n\right] \tag{7.88}$$

If $Z_1 = Z_2$, the input impedance at the third harmonic can be found from Fig. 7.21d as:

$$Z_{in}(3f_0) = jZ_1 \tan[3(\theta_1 + \theta_2)] \tag{7.89}$$

The reflection coefficient is:

$$\Gamma_{in}(3f_0) = \frac{Z_{in} - R_{ref}}{Z_{in} + R_{ref}} = \frac{Z_1^2 \tan^2[3(\theta_1 + \theta_2)] - R_{ref}^2 + j2R_{ref}Z_1 \tan[3(\theta_1 + \theta_2)]}{R_{ref}^2 + Z_1^2 \tan^2[3(\theta_1 + \theta_2)]} \tag{7.90}$$

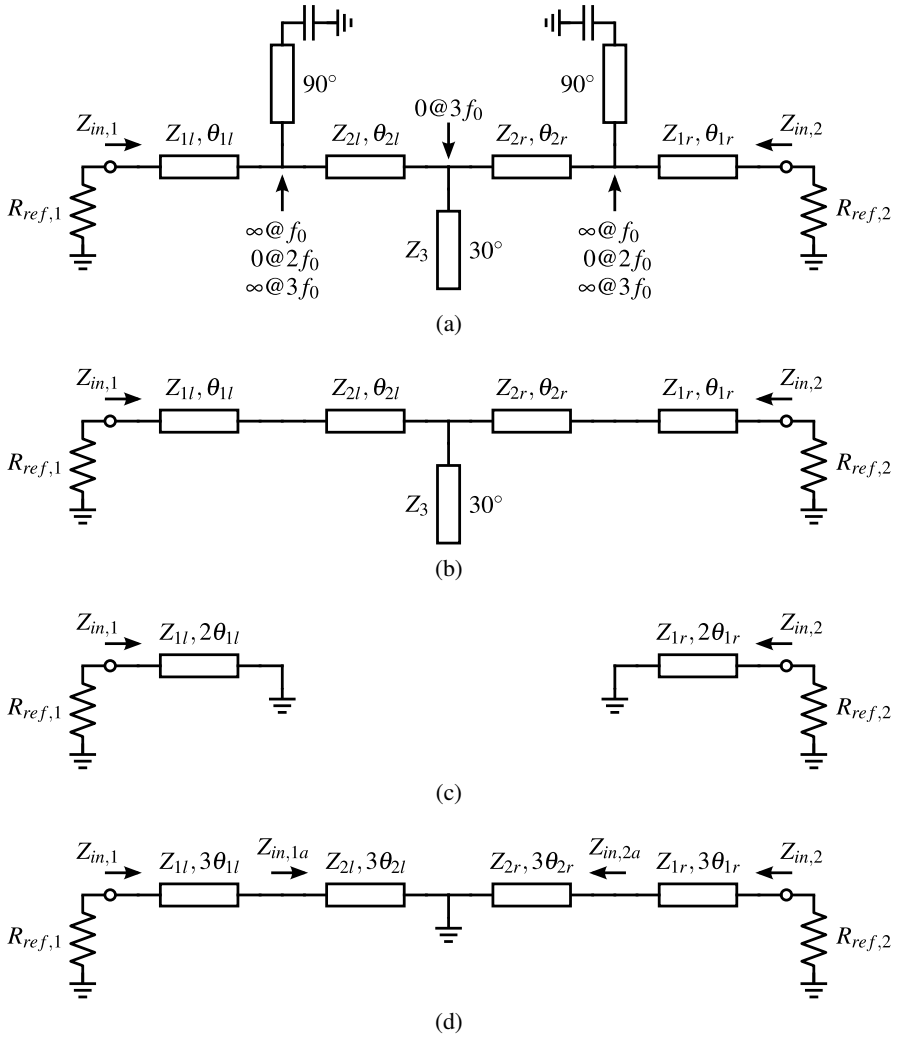


Figure 7.21: (a) Arbitrary phase harmonic termination ISMN circuit diagram. Equivalent circuits at (b) f_0, (c) $2f_0$, and (d) $3f_0$.

Solving for the phase of the reflection coefficient yields:

$$\phi_{3f_0} = \angle\Gamma_{in} = \arctan\left(\frac{2R_{ref}Z_1\tan[3(\theta_1+\theta_2)]}{Z_1^2\tan^2[3(\theta_1+\theta_2)] - R_{ref}^2}\right) \tag{7.91}$$

Constraining θ_2:

$$\theta_2 = \frac{1}{3}\left[-3\theta_1 + \arctan\left(\frac{R_{ref}\cot\left(\frac{\phi_{3f_0}}{2}\right)}{Z_1}\right) + \pi n\right] \tag{7.92}$$

If $Z_1 \neq Z_2$, the input impedance in between the two series TLs at the third harmonic can be written as:

$$Z_{in,a}(3f_0) = jZ_2\tan(3\theta_2) \tag{7.93}$$

Translating this impedance to the transistor node yields:

$$Z_{in}(3f_0) = Z_1 \frac{Z_{in,a} + jZ_1 \tan(3\theta_1)}{Z_1 + jZ_{in,a} \tan(3\theta_1)} = Z_1 \frac{jZ_2 \tan(3\theta_2) + jZ_1 \tan(3\theta_1)}{Z_1 - Z_2 \tan(3\theta_1) \tan(3\theta_2)} \tag{7.94}$$

The reflection coefficient can be written:

$$\Gamma_{in}(3f_0) = \frac{Z_{in} - R_{ref}}{Z_{in} + R_{ref}} = \frac{\left[Z_1(Z_1 \tan(3\theta_1) + Z_2 \tan(3\theta_2)) + jR_{ref}(Z_1 - Z_2 \tan(3\theta_1) \tan(3\theta_2))\right]^2}{\left[R_{ref}(Z_1 - Z_2 \tan(3\theta_1) \tan(3\theta_2))\right]^2 + [Z_1(Z_1 \tan(3\theta_1) + Z_2 \tan(3\theta_2))]^2} \tag{7.95}$$

The phase of the reflection coefficient is:

$$\phi_{3f_0} = \angle\Gamma_{in} = \arctan\left(\frac{Z_1^2 \left[Z_1 \tan(3\theta_1) + Z_2 \tan(3\theta_2)\right]^2 - R_{ref}^2 \left[Z_1 - Z_2 \tan(3\theta_1) \tan(3\theta_2)\right]^2}{2Z_1 R_{ref} \left[Z_1 Z_2 \tan(3\theta_2) - Z_1 Z_2 \tan^2(3\theta_1) \tan(3\theta_2) + \tan(3\theta_1)(Z_1^2 - Z_2^2 \tan^2(3\theta_2))\right]}\right) \tag{7.96}$$

Constraining θ_2:

$$\theta_2 = \frac{1}{3}\left[\arctan\left(\frac{Z_1 \left[\zeta \tan^2(3\theta_1) - \zeta - \zeta \sec^2(3\theta_1) \sec(\phi_{3f_0}) + (Z_1^2 + R_{ref}^2) \tan(3\theta_1) \tan(\phi_{3f_0})\right]}{Z_2 \left[R_{ref}^2 \tan^2(3\theta_1) \tan(\phi_{3f_0}) - Z_1^2 \tan(\phi_{3f_0}) - 2\zeta \tan(3\theta_1)\right]}\right) + \pi n\right] \tag{7.97}$$

where $\zeta = Z_1 R_{ref}$. These long equations require the periodicity to be represented in the $+\pi n$ term at the end. Depending on the reference impedances and TL characteristic impedances, the constrained electrical length may become negative, and will require an additional electrical length to reach the minimal positive value. The characteristic impedance of every TL can be optimized in this ISMN for fundamental frequency matching.

7.3.3 Discussion

In this section, six lumped element and five transmission line ISMNs have been derived. It may appear inadequate to only analyze these networks for real reference impedances, when transistors have complex impedances. However, these networks will most likely be used to present fundamental and harmonic impedances based on source- and load-pull simulation or measurement, which are almost always referenced to a real impedance. Therefore, the complex reference impedances of the transistors loading the network must be taken into account only when performing the desired fundamental matching optimization. More details are given through a design example in the next section.

Table 7.1: Optimal ISMN harmonic impedances

Harmonic Frequency	Optimal Driver Stage Load Reflection Coefficient (50 Ω)	Optimal Output Stage Source Reflection Coefficient (10 Ω)
f_0	0.7 ∠60°	0.95 ∠-162°
$2f_0$	0.95 ∠84°	0.95 ∠260°
$3f_0$	0.95 ∠-45° to 120°	0.95 ∠300°

7.4 ISMN Design Example

In this section, the ISMN portion of a two-stage PA design is discussed to give instruction for utilizing the derived harmonically terminated interstage matching networks and bi-directional matching analysis. The example is for a two-stage base station PA, centered at 2.14 GHz. The power stage must be capable of producing 100 W of power, and the driver stage should be able to produce the power required to saturate the output stage (36-38 dBm). In this hybrid design, two GaN transistors fabricated by Cree are selected. The power device is the DC-3 GHz, 100 W, 50 V CGHV40100F packaged GaN HEMT, which has a low output capacitance of only 7.3 pF due to its very high drain voltage. The driver transistor is the DC-18 GHz, 6 W, 40 V packaged GaN HEMT, the CGHV1F006S, which has an extremely low output capacitance of 0.31 pF, allowing for highly efficient operation. Both devices will be biased near pinch-off, below 10% of the peak current.

In order to design the ISMN, the optimal harmonic loading conditions for each transistor must be known, as well as the impedances of each transistor loading the ISMN. The former is found through iterative, harmonic source- and load-pull simulation (or measurement) for both devices. In Table 7.1, the optimal harmonic loading conditions for the output of the driver stage and the input of the power stage are found from simulation. A 10 Ω reference impedance is used for the power transistor to provide higher Smith chart resolution near peak power and efficiency impedances.

Of course, the designer must be aware of the effectiveness of each harmonic termination. In this case, the third harmonic termination at the input of the power stage provides a negligible efficiency improvement (<1 point). Therefore, the overall performance may improve by disregarding the phase of this harmonic

Table 7.2: ISMN series TL electrical lengths constrained by harmonic termination phases.

Transmission Line (θ)	Harmonic	Stage	Harmonic Phase (deg)	Electrical Length (deg)
θ_{1l}	2	Driver	84°	3.7°
θ_{2l}	3	Driver	66°	59.6°
θ_{1r}	2	Output	260°	65.7°
θ_{2r}	3	Output	300°	46.5°

termination in favor of better optimization at the fundamental frequency. Note also, that a range of phases at a particular harmonic may be acceptable. For example, the driver stage efficiency due to the third harmonic termination remains high over a significant phase range.

Next, the transistor impedances loading the ISMN at the fundamental frequency must be found: the output impedance of the driver device and the input impedance of the power device. Both of these are found from small-signal S-parameter simulations, which only use bias tees and small-signal ports. At 2.14 GHz, the output impedance of the driver transistor is $5.88 - j76.4\,\Omega$ while the input impedance of the power device is $0.22 + j1.43\,\Omega$.

Starting with an ISMN topology from Section 7.3, the harmonic terminations are constrained. The arbitrary phase TL ISMN from Fig. 7.21 is chosen for this design, since it allows for harmonic terminations referenced to the package. The electrical lengths of each series TL are given by (7.88) and (7.97) considering the desired harmonic phases in Table 7.1, as detailed in Table 7.2. These are confirmed in simulation with the port impedances set to the reference impedances of the source- and load-pull simulations. In actuality, the opposite port will be loaded with the transistor impedance. However, this does not affect the harmonic termination due to the high quality factor resonators.

With the harmonic termination phases constrained, now the fundamental frequency matching is performed in one of two ways: using the bi-directional matching analysis, or directly optimizing in simulation. This design will start with the former to demonstrate how to utilize the previous equations, and end with the latter. First, the desired fundamental reflection coefficients for each stage must be converted to the transistor reference impedance in order to properly select the desired $\mathbf{S}$. The optimal source-pull reflection coefficient for the power device of 0.95 $\angle$ -162° is converted to an impedance using its reference impedance of $10\,\Omega$,

and then back to a reflection coefficient again using the input impedance of the power device as the reference impedance, resulting in a reflection coefficient of 0.313 ∠ -56.78°. The same is done for the optimal load-pull reflection coefficient for the driver device, resulting in a reflection coefficient of 0.692 ∠ 0.23°. These two reflection coefficients will now be used as the desired S_{22} and S_{11} respectively.

The selection of the 'through' parameters in **S** is unclear, since $|S_{11}| \neq |S_{22}|$, meaning the network must be lossy. In order to minimize the loss, the through parameters are chosen such that:

$$|S_{21}| = |S_{12}| = \sqrt{1 - \max(|S_{11}|, |S_{22}|)} \tag{7.98}$$

Therefore, the desired S-parameters are set to:

$$\mathbf{S}^{ij} = \begin{bmatrix} 0.692\, e^{j0.225^\circ} & \sqrt{1 - 0.69^2} \\ \sqrt{1 - 0.69^2} & 0.313\, e^{-j56.8^\circ} \end{bmatrix} \tag{7.99}$$

The cascade matrix is made by converting $\mathbf{S}^{ij}$ to $\mathbf{R}^{ij}$ and filling in the **P** matrices in (7.42) with the following values chosen for this example:

$$Z^p_{ref} = Z_0 = 50\,\Omega \tag{7.100}$$

$$Z^i_{ref} = Z_{ref,1} = 5.88 - j76.4\,\Omega \tag{7.101}$$

$$Z^j_{ref} = Z_{ref,2} = 0.22 + j1.43\,\Omega \tag{7.102}$$

$$Z^m_{ref} = Z_0 = 10\,\Omega \tag{7.103}$$

Converting $\mathbf{R}^{pm}$ to $\mathbf{S}^{pm}$ yields:

$$\mathbf{S}^{pm} = \begin{bmatrix} 0.631115 + j1.7926 & -0.311081 + j0.405599 \\ -0.311081 + j0.405599 & -1.21639 - j0.286412 \end{bmatrix} = \begin{bmatrix} 1.9\angle 70.6^\circ & 0.5 \\ 0.5 & 1.25\angle \text{-}166.75^\circ \end{bmatrix} \tag{7.104}$$

Interestingly, the ISMN should have S-parameters with magnitudes greater than one, meaning the network cannot be passive. Fortunately, the ISMN is not really a passive network, as it is loaded with two generators. Though not performed in this work, the application of active load-pull theory, as in appendix B of [169], could bring clarity to this viewpoint of the ISMN. The resulting S-parameters are confirmed in simulation. Fig. 7.22 shows the simulation setup while Fig. 7.23 shows the results, demonstrating the desired S-parameter performance when loaded with the proper transistor impedances.

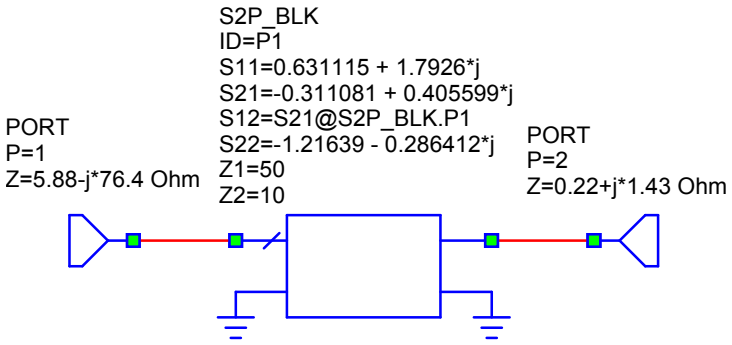


Figure 7.22: AWR simulation setup to confirm ISMN S-parameters.

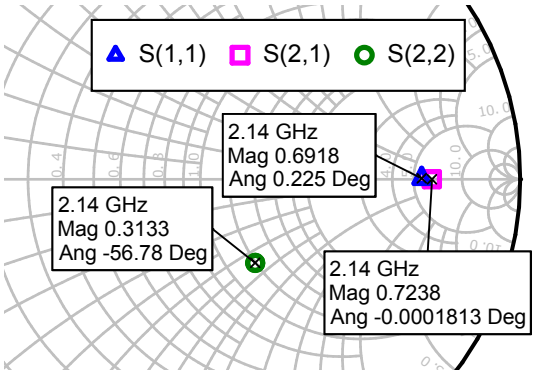


Figure 7.23: Simulation of ISMN S-parameters showing desired results.

Now, the free parameters (Z_{1l}, Z_{2l}, Z_{1r}, Z_{2r}, and Z_3) of the constrained ISMN are optimized such that the large-signal S-parameters match the desired S-parameters transformed to the 10 Ω and 50 Ω reference impedances, as shown in Fig. 7.24. The power supplied by each generator to the ISMN is taken from simulation of each transistor under the expected bias and harmonic loading conditions. Afer optimization, the following S-parameters are realized:

$$\mathbf{S}^{pm} = \begin{bmatrix} 1.64\angle 70.6^\circ & 0.5 \\ 0.76 & 1.52\angle -166.75^\circ \end{bmatrix} \tag{7.105}$$

The optimized ISMN must be simulated in the two-stage PA to determine if the realized S-parameters are close enough to those desired, by evaluating the cascaded PA performance.

The second way to optimize the ISMN for fundamental matching is purely passive. Two simulations, one for the reflection coefficient of each transistor, must be simultaneously optimized, as shown in Fig. 7.25. For the power stage, port 1 of the ISMN is loaded with the driver transistor impedance, while port 2 is set to

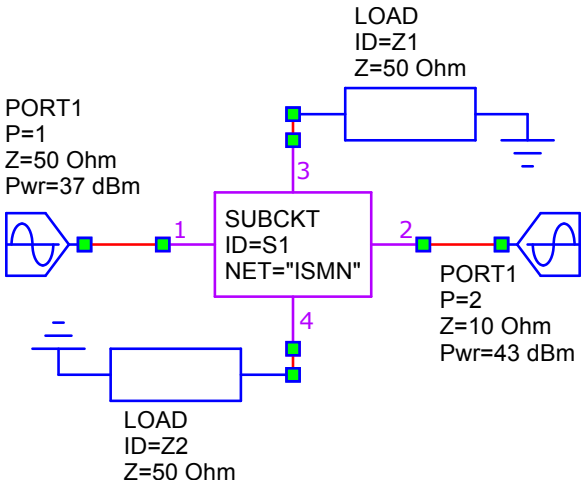


Figure 7.24: AWR simulation setup for the optimization of the ISMN at the fundamental frequency, considering the transistors as generators.

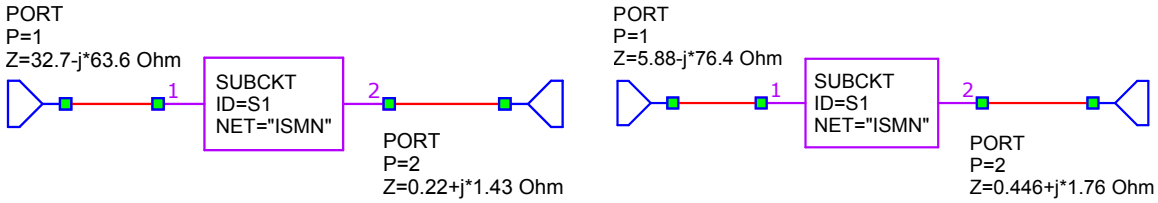


Figure 7.25: AWR simulation setup to optimize the ISMN performance passively for (a) the driver stage load, and (b) the power stage load.

the conjugate of the desired load impedance. For the driver stage, port 1 is set to the conjugate of the desired load impedance, while port 2 is loaded with the power transistor impedance. The magnitude of the input match of each simulation, port 2 for the power stage and port 1 for the driver stage, is optimized to achieve the desired impedance transformation in both directions.

7.5 Conclusion

The interstage matching network is currently the weak link in the design of high efficiency, multi-stage PAs, which are necessary for outphasing due to the constant, significant input power levels. Therefore, the requirements of the interstage matching network to terminate harmonics at both ports and perform fundamental matching were explored theoretically and in simulation. Eleven, minimum loss, harmonically terminated in-

terstage matching networks were derived for lumped element and transmission line implementation. Original contributions in this chapter include:

- The derivation and analysis of harmonically terminated interstage matching networks implemented with lumped elements and transmission lines, which utilized a minimal number of elements to decrease loss. Equations were derived to constrain the harmonic terminations for each transistor loading the network, while some were degrees of freedom for fundamental frequency matching.

Unfortunately, a base station PA is a poor application for the harmonically terminated ISMNs developed in this chapter. The main reason is the parasitics of the large, packaged transistors required, especially in the output stage. The gate-to-source capacitance at the input of the CGHV40100F transistor is 29.3 pF. At the second (4.28 GHz) and third (6.42 GHz) harmonics, this capacitance presents 1.27 Ω and 0.85 Ω paths to ground, respectively, reducing the impact of the input harmonic terminations provided by the ISMN. A large, bare-die transistor does not provide a better opportunity. The CGH60120D is the bare-die transistor within the CGH40120F, a 120 W GaN packaged transistor, which have 34 pF and 35 pF gate-to-source capacitances respectively. Apparently, the package does not contribute significant input capacitance.

MMICs or smaller bare-die transistors can make use of harmonically terminated ISMNs, due to lower input capacitances and reduced parasitics in general. The 10×100 μm transistor used by several MMIC designs in this thesis has a gate-to-source capacitance of only 0.77 pF, which represents an impedance to ground of 48.3 Ω and 32.2 Ω at 4.28 GHz ($2f_0$) and 6.42 GHz ($3f_0$), respectively. Even at harmonics of 10 GHz, this capacitance presents 10.3 Ω and 6.9 Ω paths to ground at the second and third harmonics, respectively.

The theoretical development in this chapter gives a basis for designing bidirectional matching networks for complex loads, that include matching at the harmonic frequencies. This approach is useful for interstage matching of multi-state power amplifiers and this chapter lays down the foundation for future designs.

Chapter 8

Conclusion and Future Work

Contents

8.1 Summary

The research presented in this thesis focused on the understanding and development of the outphasing PA architecture for efficiently amplifying high PAR signals. In order to expand understanding on an architecture created in 1935, the internal PA performance and load modulation were examined in measurement. A quasi-MMIC outphasing PA architecture was constructed from high efficiency GaN MMIC internal PAs and an off-chip combiner, which included bi-directional couplers for the direct measurement of power waves internal to the architecture. Using three different off-chip combiners, both non-isolated and isolated, five variations of the outphasing power amplifier were measured at 10.1 GHz: Chireix outphasing, LINC, multi-level LINC, asymmetric multilevel outphasing, and multi-level Chireix outphasing.

Each architecture was characterized in measurement in terms of internal PA performance (power and

efficiency), load modulation, system performance (ΔP_{out}), and linearity indicators. Due to the consistent use of the same internal MMIC PAs, comparisons can be made between each architecture. The addition of discrete supply modulation was shown to be crucial for efficiency enhancement, with the AMO and ML-CO PAs achieving the highest efficiency at back-off. While both architectures need signal processing to linearize the signal split between outphasing angle and supply modulation, the AMO PA exhibited significantly less nonlinear phase transformation than the ML-CO PA, and should be much easier to linearize. A GaN ML-CO MMIC PA was designed and measured at 9.7 GHz, achieving state-of-the-art average efficiency for a 6 dB PAR signal.

The concept of high efficiency PA-rectifier duality was verified experimentally at 10.1 GHz with two GaN MMIC PA circuits, and leveraged into a power recycling LINC PA architecture. The duality proved critical, because the rectifier could not be simulated with the available model. A GaN power recycling LINC MMIC PA was designed and measured at 10.35 GHz. The power recovered by the self-synchronous rectifier improved the system efficiency by 8.1 points at 3.5 dB back-off.

Finally, the focus turned to the PAs internal to the outphasing architecture. Harmonically terminated interstage matching networks were developed in lumped element and transmission line implementations, to further improve high efficiency power amplifier classes.

8.2 Future Work

Several avenues are available for the continuation of the work presented in this thesis. Most obvious is performing modulated measurements with the most promising outphasing PA architectures developed: AMO and ML-CO. Linearized, modulated measurements have been performed on the AMO PA already [100, 106], demonstrating its practical feasibility, as well as competitive performance. Significant work is required to demonstrate the practicality of the ML-CO PA. Two signal generation and upconversion paths are required in this case. Static characterization must be performed considering the imbalances in the PA itself as well as the upconversion paths, similar to [91]. The optimal signal split between outphasing angle and supply modulation must be determined, before the input signal can be decomposed into branch signals and

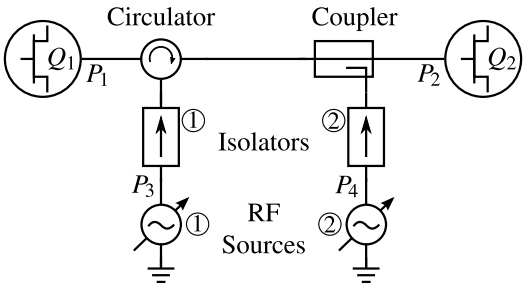


Figure 8.1: Active interstage load-pull network.

presdistorted digitally at baseband.

The GaN power recycling LINC MMIC PA could be refined in one of two ways. A third quadrant model could be made for a transistor available on a test chip, so that a design could be fully simulated, enabling the self-synchronous gate termination to be implemented on-chip. An alternative would be to overcome the losses in the tuner with an active loop, as done in the measurements in subsection 6.4.2, to find the optimal gate termination. A design iteration could then be performed, implementing the termination on-chip. In either case, power circuitry could be developed to boost the voltage of the rectifier and interface the recovered power with a power supply.

The harmonically terminated interstage matching network analysis performed in this thesis barely cracks the surface of possible research in this area. In the ISMN design example in Section 7.4, the s-parameters required to optimally match the transistors at the fundamental frequency were not passive. Upon further reflection, the ISMN is not really passive, since it is loaded with two generators. This would be a useful application and extension of the active load-pull theory presented in [169]. Additionally, a more generalized lumped-element implementation of a harmonically terminated ISMN could be beneficial to develop.

Lastly, an interstage active load-pull measurement could be devised using the network shown in Fig. 8.1. The benefit of such a measurement is accurately capturing the interaction between the two transistors, especially at harmonic frequencies. To do so, the through path has minimal loss, but the circulator and coupler must be broadband to pass harmonic power. The RF sources must be able to vary both amplitude and phase. Additionally, sources operating at the fundamental and harmonic frequencies must be combined to synthesize harmonic impedances at the transistors, which is already done on commercially available active

load-pull systems.

The 50 Ω S-parameters of this network are the following:

$$\mathbf{S} = \begin{bmatrix} 0 & I_{circ} & \approx 1 & I_{circ} + I_{coup} \\ \approx 1 & 0 & I_{circ} & C \\ I_{circ} + I_1 & I_2 & 0 & I_2 + I_{coup} \\ I_{coup} + I_3 & I_3 + C & I_3 + I_{coup} & 0 \end{bmatrix} \tag{8.1}$$

where I_{circ} and I_{coup} are the isolations of the circulator and coupler, respectively. C is the coupling factor of the coupler. I_1 and I_2 are the isolations of isolators 1 and 2, respectively. The focus of this network is to provide low loss paths between the transistors, and between one RF source and a corresponding transistor. The characteristic impedance of the transistor, along with the loss between it and the RF source will determine the power and phase required by the source to synthesize impedances covering the Smith chart. This network will not take into account power reflected by Q_2 back into Q_1 due to the isolation of the circulator.

Finally, the ML-CO MMIC PA could be directly integrated with the power-DAC MMIC, as well as a signal component separator MMIC, as developed on CMOS in [31]. The combination of these three would yield a fully integrated ML-CO MMIC PA, requiring only digital control signals and supply voltages. DARPA is working toward this type of integration through the Diverse Accessible Heterogeneous Integration (DAHI) program, which is aiming at transistor-scale heterogeneous integration of CMOS, GaN, GaAs, InP, MEMS and more [170].

8.3 Contributions

Original contributions from the material presented in this dissertation are summarized by chapter below.

Chapter 2 developed the understanding of load modulation operation within the Chireix outphasing power amplifier both theoretically and experimentally. A hybrid Chireix outphasing PA was developed with GaN MMIC internal PAs and off-chip combining that included bi-directional couplers to measure the internal PA performance and load modulation directly. A brief introduction to the fundamentals of GaN MMIC design was presented, along with the practical issues of designing a Chireix combiner for desired load modulation.

Original contributions in this chapter include the following:

- The design and measurement of a 70% efficient (PAE) GaN MMIC PA with 2.7 W of output power [35].
- The derivation of equations predicting the load modulation of a three-port combiner under outphasing excitation with small-signal analysis to aid in Chireix combiner design [83].
- The development of an internal PA performance and load modulation measurement setup at 10.1 GHz, along with a hybrid Chireix outphasing PA enabling the measurement of absolute power waves internal to the architecture [83, 93, 94].
- The extension of the upper frequency of any outphasing PA implementation from 5 GHz [51] to 10.1 GHz [83, 93, 94].
- The load modulation internal to a Chireix outphasing PA was measured [83, 93, 94], demonstrating the variation of internal PA power and efficiency.

Chapter 3 developed the understanding of the linear amplification in the LINC PA architecture, a subset of outphasing amplifiers. The theoretical foundation for the input signal processing common to all outphasing amplifiers was presented. The measurement setup developed in chapter 2 was extended to the LINC PA through the use of an isolated combiner. Original contributions in this chapter include the following:

- The extension of the internal PA performance and load modulation measurement setup to isolated outphasing or LINC [83, 93, 94].
- The measurement of load modulation internal to a LINC PA was demonstrated [83, 93, 94]. In this cases, it was minimal, yet nonzero, due to the finite isolation of the combiner.
- Direct comparison between the LINC and Chireix outphasing PAs was enabled by this measurement setup, which utilizes the same internal PAs. The efficiency improvement of Chireix outphasing, and the linear amplification of LINC are both highlighted [83, 93, 94].

Chapter 4 combined discrete supply modulation with isolated outphasing (LINC) for efficiency improvement. The theoretical understanding of this combination was developed for symmetric and asymmetric

supply modulation. The internal PA performance and load modulation measurement setup from chapter 3 was extended through static variation in the drain voltage of each internal PA, symmetrically and asymmetrically. Original contributions in this chapter include the following:

- The extension of the internal PA performance and load modulation measurement setup to supply modulated LINC [94], demonstrating the efficiency improvement caused by minimized both RF and DC power dissipation.
- The measurement of load modulation internal to the supply modulated LINC PA [94], which became significant when the asymmetric supplies were separated by several volts, and led to decreased internal PA efficiency.

Chapter 5 combined discrete supply modulation with Chireix outphasing for the first time in literature. The internal PA performance and load modulation measurement setup from chapter 2 was extended to include static variation in the drain voltage. An integrated GaN MMIC implementation was shown to mitigate imbalances seen in the hybrid prototype. The supply modulated Chireix outphasing MMIC PA was tested with a GaN discrete supply modulator, demonstrating improved efficiency for high PAR signals. Original contributions in this chapter include the following:

- The extension of the internal PA performance and load modulation measurement setup to supply modulated Chireix outphasing [94], demonstrating efficiency improvement, along with significant imbalances of internal PA output power with swept supply, leading to load modulation distortion.
- The prediction of load modulation distortion caused by internal PA output power imbalance was demonstrated to match measurement [83].
- Design of a GaN MMIC PA incorporating all of the RF components of the architecture (class-F internal PAs and Chireix combiner) that achieved 48% average total efficiency for a 6 dB PAR QPSK signal at 9.7 GHz with 5 W of output power [108]. This work won the student paper design competition at the Compound Semiconductor and IC Symposium.

- Testing of supply modulated Chireix outphasing GaN MMIC PA with a real supply modulator, implemented in GaN [120].

- Study of optimal supply levels under quantity restriction [108, 120], demonstrating a 12 point improvement only a single additional level.

Chapter 6 incorporated microwave rectification with the LINC PA architecture in order to recycle dissipated RF power and improve efficiency. The duality between high efficiency power amplifiers and high efficiency rectifiers was confirmed experimentally at 10.1 GHz on two GaN MMIC PAs described in [35] and leveraged for this architecture. The entire architecture was implemented on a GaN MMIC (internal PAs, rectifier, and isolated combiner) at X-band. Original contributions in this chapter include the following:

- The experimental validation of the high efficiency PA-rectifier duality at 10.1 GHz with two GaN MMIC PAs, achieved between 62.5% and 68% efficiency in both modes of operation [126, 143].

- The design and measurement of a GaN power recycling LINC MMIC PA, demonstrated a peak drain efficiency of 71.8% with 6 W of output power at 10.35 GHz with a peak rectified power of 2.25 W, leading to a drain efficiency improvement of 8.1 points at 3.5 dB back-off [144].

Chapter 7 moved toward high efficiency multi-stage PA design, which is necessary for outphasing due to the constant input power. Because high efficiency output matching networks are well understood, the focus of this chapter was on the development of harmonically terminated interstage matching network. Original contributions in this chapter include:

- The derivation and analysis of harmonically terminated interstage matching networks implemented with lumped elements and transmission lines, which utilized a minimal number of elements to decrease loss. Equations were derived to constrain the harmonic terminations for each transistor loading the network, while some were degrees of freedom for fundamental frequency matching.

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Appendix A

Off-Resonance Lumped Element Resonator Equivalent Components

Often, lumped element resonators are useful as harmonic terminations in high efficiency PA design. At non-harmonic frequencies, though, these networks still contribute to impedance matching, and should be known. In the design of harmonically terminated, lumped element ISMNs in subsection 7.3.1, off resonance lumped element resonator values are required in order to utilize them in a resonator at another frequency, minimizing the number of components. In this appendix, the value of equivalent circuit elements (inductors and capacitors) for lumped element resonators at frequencies above and below resonance is derived for series and parallel resonators.

A.1 Series Resonator

The input impedance of the series resonator, shown in Fig. A.1, can be written as:

$$Z_{in}(\omega) = j\omega L + \frac{1}{j\omega C} = j\frac{(\omega^2 LC - 1)}{\omega C} \tag{A.1}$$

Using the relationship between L and C at the resonant frequency:

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{A.2}$$

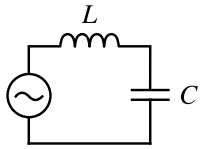


Figure A.1: Series LC resonator.

the input impedance can be written in terms of the capacitor or inductor only:

$$Z_{in}(\omega) = j\frac{(\omega^2 - \omega_0^2)}{\omega_0^2 \omega C} \tag{A.3}$$

$$Z_{in}(\omega) = jL\frac{(\omega^2 - \omega_0^2)}{\omega} \tag{A.4}$$

The ratio of the evaluated frequency to the resonant frequency is defined as:

$$x = \frac{\omega}{\omega_0} \tag{A.5}$$

A.1.1 Below Resonance ($x < 1$)

At low frequencies, an inductor approaches a short circuit while a capacitor approaches an open circuit. Thus, the series resonator is capacitive below resonance. Setting the input impedance, (A.3) or (A.4), equal to the that of an equivalent capacitor, C', yields the following:

$$C' = \frac{\omega_0^2 C}{\omega_0^2 - \omega^2} = \frac{C}{1 - x^2} \tag{A.6}$$

$$C' = \frac{-1}{L(\omega^2 - \omega_0^2)} = \frac{-1}{\omega_0^2 L(x^2 - 1)} \tag{A.7}$$

A.1.2 Above Resonance ($x > 1$)

Above resonance, the series resonator is inductive. Setting the input impedance, (A.3) or (A.4), equal to the that of an equivalent inductor, L', yields the following:

$$L' = \frac{\omega^2 - \omega_0^2}{\omega^2 \omega_0^2 C} = \frac{x^2 - 1}{x^2 \omega_0^2 C} \tag{A.8}$$

$$L' = \frac{(\omega^2 - \omega_0^2)L}{\omega^2} = \frac{(x^2 - 1)L}{x} \tag{A.9}$$

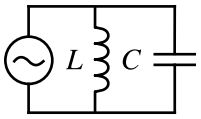


Figure A.2: Parallel LC resonator.

A.2 Parallel Resonator

The input impedance of a parallel resonator, shown in Fig. A.2, can be written as:

$$Z_{in}(\omega) = j\omega L // \frac{1}{j\omega C} = \frac{j\omega L}{1 - \omega^2 LC} \tag{A.10}$$

Using (A.2), the input impedance can be written in terms of the capacitor or inductor only:

$$Z_{in}(\omega) = \frac{j\omega}{(\omega_0^2 - \omega^2)C} \tag{A.11}$$

$$Z_{in}(\omega) = \frac{j\omega_0^2 \omega L}{\omega_0^2 - \omega^2} \tag{A.12}$$

A.2.1 Below Resonance ($x < 1$)

Below resonance, the parallel resonator is inductive. Setting the input impedance, (A.11) or (A.12), equal to the that of an equivalent inductor, L', yields the following:

$$L' = \frac{1}{(\omega_0^2 - \omega^2)C} = \frac{1}{\omega_0^2 C(1 - x^2)} \tag{A.13}$$

$$L' = \frac{\omega_0^2 L}{\omega_0^2 - \omega^2} = \frac{L}{1 - x^2} \tag{A.14}$$

A.2.2 Above Resonance ($x > 1$)

Above resonance, the parallel combination is capacitive. Setting the input impedance, (A.11) or (A.12), equal to the that of an equivalent capacitor, C', yields the followingr:

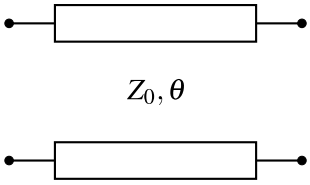
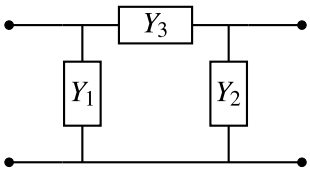
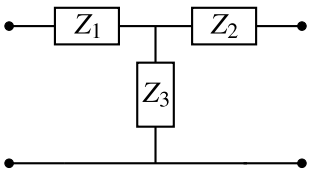
$$C' = \frac{(\omega - \omega_0^2)C}{\omega^2} = \frac{(x^2 - 1)C}{x^2} \tag{A.15}$$

$$C' = \frac{\omega^2 - \omega_0^2}{\omega^2 \omega_0^2 L} = \frac{x^2 - 1}{x^2 \omega_0^2 L} \tag{A.16}$$

Appendix B

Transmission Line Equivalent Networks

Table B.1: ABCD Parameters for Networks

Circuit	ABCD Parameters
	$A = \cos\theta$ $B = jZ_0 \sin\theta$ $C = jY_0 \sin\theta$ $D = \cos\theta$
	$A = 1 + \frac{Z_1}{Z_3}$ $B = Z_1 + Z_2 + \frac{Z_1 Z_2}{Z_3}$ $C = \frac{1}{Z_3}$ $D = 1 + \frac{Z_2}{Z_3}$
	$A = 1 + \frac{Y_2}{Y_3}$ $B = \frac{1}{Y_3}$ $C = Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3}$ $D = 1 + \frac{Y_1}{Y_3}$

Equivalent networks formed in the shape of a "T" or "π" can be used to approximate other networks over a narrow bandwidth, while only being exact at a single frequency. A desirable network to approximate in the context of MMIC design is the transmission line, since it can be difficult to fit a long line into the small

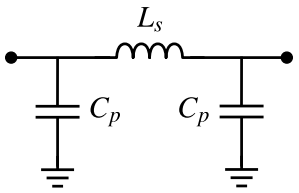


Figure B.1: Low-pass π-network

confines of a MMIC. Equivalences between the T- or π-network and a transmission line are only readily available for the 90°, 180°, and 270° electrical lengths common to passive combining structures [117, 118]. In MMIC design, the electrical length of a required transmission line may not be a multiple of 90°. Therefore, this appendix derives equivalent networks for a transmission line with any electrical length and characteristic impedances.

Table B.1 shows the ABCD parameters of the transmission line, T-network, and π-network [119]. The parameters Z_i and Y_i are impedances and admittances, respectively, where i distinguishes each of the three elements. The transmission line is defined by its characteristic impedance, Z_0, and its electrical length, θ. The following analysis solves for the equivalent network parameters by equating its ABCD parameters with that of a transmission line. Note that A and D are equal for the transmission line, forcing $Z_1 = Z_2$ and $Y_1 = Y_2$, leading to symmetric networks.

B.1 Low-Pass Equivalent Networks

The low-pass π-network makes use of a series inductor, L_s, and shunt capacitors, C_p, as shown in Fig. B.1. By filling in the corresponding Y-parameters, $Y_1 = Y_2 = j\omega C_p$ and $Y_3 = 1/j\omega L_s$, the ABCD matrix of this network is found:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 - \omega^2 L_s C_p & j\omega L_s \\ -j\omega C_p(\omega^2 C_p L_s - 2) & 1 - \omega^2 L_s C_p \end{bmatrix} \tag{B.1}$$

Equating this to the ABCD matrix of a transmission line in Table B.1, and solving for C_p and L_s yields:

$$L_s = Z_0 \frac{\sin\theta}{\omega} \tag{B.2}$$

$$C_p = \frac{1}{Z_0} \frac{1 - \cos\theta}{\omega \sin\theta} \tag{B.3}$$

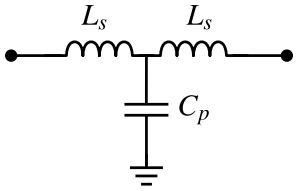


Figure B.2: Low-pass T-network

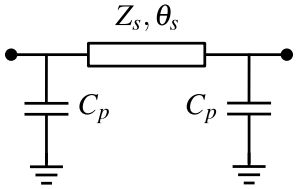


Figure B.3: Low-pass TL-π-Network

The low-pass T-network utilizes two series inductors, L_s, and a shunt capacitor, C_p, as shown in Fig. B.2. By filling in the corresponding Y-parameters, $Z_1 = Z_2 = j\omega L_s$ and $Z_3 = 1/j\omega C_p$, the ABCD matrix of this network is found:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1-\omega^2 L_s C_p & -j\omega L_s(\omega^2 C_p L_s - 2) \\ j\omega C_p & 1-\omega^2 L_s C_p \end{bmatrix} \tag{B.4}$$

Equating this to the ABCD matrix of a transmission line in Table B.1, and solving for C_p and L_s yields:

$$L_s = Z_0 \frac{1-\cos\theta}{\omega \sin\theta} \tag{B.5}$$

$$C_p = \frac{1}{Z_0}\frac{\sin\theta}{\omega} \tag{B.6}$$

In MMIC fabrication, spiral inductors can be quite lossy. In that case, a transmission line may be utilized to provide the series inductance. The low-pass TL-π network utilizes a series transmission line, Z_s, θ_s, and shunt capacitors, C_p, as shown in Fig. B.3. The equations given in Table B.1 are not valid for the series TL element. Therefore, the ABCD matrix of this network is calculated by cascading the ABCD matrices of the three elements, C_p - TL - C_p, as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C_p & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_s & jZ_s \sin\theta_s \\ \frac{j\sin\theta_s}{Z_s} & \cos\theta_s \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_p & 1 \end{bmatrix} \tag{B.7}$$

Leading to the following:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta_s - \omega Z_s C_p \sin\theta_s & jZ_s \sin\theta_s \\ j\left[2\omega C_p \cos\theta_s + \sin\theta_s \left(\frac{1}{Z_s} - \omega^2 C_p^2 Z_1\right)\right] & \cos\theta_s - \omega Z_s C_p \sin\theta_s \end{bmatrix} \tag{B.8}$$

Equating this to the ABCD matrix of a transmission line in Table B.1, two of the three unknown variables (C_p, Z_s, θ_s) can be solved for.

Solving for C_p and Z_s:

$$C_p = \frac{1}{Z_0} \frac{\cos\theta_s - \cos\theta}{\omega \sin\theta} \tag{B.9}$$

$$Z_s = Z_0 \frac{\sin\theta}{\sin\theta_s} \tag{B.10}$$

Solving for C_p and θ_s:

$$C_p = \frac{1}{Z_0} \frac{\sqrt{Z_s^2 - Z_0^2 \sin^2\theta} - Z_s \cos\theta}{\omega Z_s \sin\theta} \tag{B.11}$$

$$\theta_s = \arctan\left(\frac{Z_0 \sin\theta}{\sqrt{Z_s^2 - Z_0^2 \sin^2\theta}}\right) \tag{B.12}$$

Solving for Z_s and θ_s:

$$Z_s = \frac{Z_0 \sin\theta}{\sqrt{1 - \left(\omega C_p Z_0 \sin\theta + \cos\theta\right)^2}} \tag{B.13}$$

$$\theta_s = \arctan\left(\frac{\sqrt{1 - \left(\omega C_p Z_0 \sin\theta + \cos\theta\right)^2}}{\omega C_p Z_0 \sin\theta + \cos\theta}\right) \tag{B.14}$$

B.2 High-Pass Equivalent Networks

The high-pass π-network makes use of a series capacitor, C_s, and shunt inductors, L_p, as shown in Fig. B.4. By filling in the corresponding Y-parameters, $Y_1 = Y_2 = {}^{-j}/_{\omega L_p}$ and $Y_3 = j\omega C_s$, the ABCD matrix of this network is found:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \omega^2 L_p C_s - 1 & \frac{-j}{\omega C_s} \\ \frac{j\left(1-2\omega^2 L_p C_s\right)}{\omega^3 L_p^2 C_s} & \omega^2 L_p C_s - 1 \end{bmatrix} \tag{B.15}$$

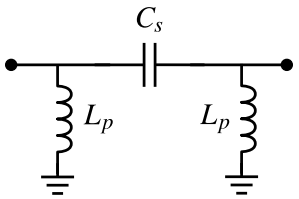


Figure B.4: High-pass π-network

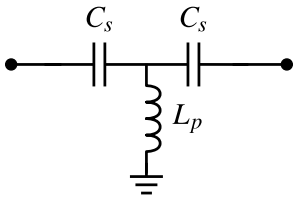


Figure B.5: High-pass T-network

Equating this to the ABCD matrix of a transmission line in Table B.1, and solving for L_p and C_s yields:

$$L_p = Z_0 \frac{\sin\theta}{\omega\left(\cos\theta - 1\right)} \tag{B.16}$$

$$C_s = \frac{-1}{Z_0}\frac{1}{\omega \sin\theta} \tag{B.17}$$

The high-pass T-network utilizes two series capacitors, C_s, and a shunt inductor, L_p, as shown in Fig. B.5. By filling in the corresponding Y-parameters, $Z_1 = Z_2 = {}^{-j}/_{\omega C_s}$ and $Z_3 = j\omega L_p$, the ABCD matrix of this network is found:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \omega^2 L_p C_s - 1 & \frac{-j}{\omega C_s} \\ \frac{j\left(1-2\omega^2 L_p C_s\right)}{\omega^3 C_s^2 L_p} & \omega^2 L_p C_s - 1 \end{bmatrix} \tag{B.18}$$

Equating this to the ABCD matrix of a transmission line in Table B.1, and solving for L_p and C_s yields:

$$L_p = -Z_0 \frac{1}{\omega \sin\theta} \tag{B.19}$$

$$C_s = \frac{1}{Z_0}\frac{\sin\theta}{\omega\left(\cos\theta - 1\right)} \tag{B.20}$$