

CARRIER AND ENVELOPE FREQUENCY MEASUREMENTS FOR
SUPPLY-MODULATED MICROWAVE POWER AMPLIFIERS

by

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B.S., Colorado School of Mines, 2010

A thesis submitted to the
Faculty of the Graduate School of the
University of Colorado in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
Department of Electrical and Computer Engineering
December 2015

This thesis entitled:

Carrier and Envelope Frequency Measurements for Supply-Modulated Microwave Power Amplifiers

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Carrier and Envelope Frequency Measurements for Supply-Modulated Microwave Power Amplifiers

Thesis directed by Professor Zoya Popović

Transmitters for high peak-to-average power ratio communication are increasingly using supply modulation to improve efficiency. In addition to a dc component, the dynamic supply may contain ac components up to 500 MHz. The signal envelope dynamic impedance of the supply terminal of a power amplifier (PA) is often unknown and available nonlinear transistor models are unable to predict dynamic low frequency effects required for design of wideband efficient supply modulators. This thesis investigates envelope frequency effects on nonlinear behavior of microwave transistors and PAs under supply-modulated conditions. A measurement setup is created to characterize multi-frequency large-signal excitation of GaN transistors and PAs at carrier frequencies in the 10 GHz range with 1-500 MHz low frequency excitation on the drain terminal. A novel method for multi-frequency analysis of nonlinear circuit components based on describing functions is developed. It is shown that the describing functions agree with simulation and measurements. In addition, the measurement setup is used to characterize the low frequency drain impedance of a MMIC PA when connected to a simple resonant supply modulator. The main motivation for this work is to obtain knowledge of the dynamic supply terminal in the low frequency regime (1-500 MHz) that can enable power amplifier and supply modulator co-design for very broadband signals.

DEDICATION

To my parents, Dave and Jan, for all the love and support they have given me.

ACKNOWLEDGMENTS

I am eternally thankful for my advisor, Zoya Popović. I cannot thank her enough for her unending effort to ensure that there are plenty of projects to keep us busy and fed; her advice and desire to send us out into the world as successful engineers; and most importantly providing an environment and expertly crafted group of motivated students to allow us to explore and learn RF technologies and techniques. It has been an honor to have her as an advisor.

Previous and current students in Zoya Popović's group that have helped me along in my degree work or simply who I had an engaging conversation with.

The donation of equipment from National Instruments (Dr. Takao Inoue and Dr. Truchard) helped complete the measurement bench for the majority of measurements presented in this thesis.

The many free software applications and libraries that facilitated the work of this thesis or just made my life easier:

- Python and multitude of packages. In particular: matplotlib, numpy, and scipy.
- The LaTeX ecosystem, in particular: MiKTeX and TeXstudio.
- JabRef
- Inkscape
- Notepad++
- Paint.net
- SumatraPDF

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CHAPTER 1

INTRODUCTION

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Wireless systems have increasingly complex modulation schemes and increasing signal bandwidths in order to improve capacity [1, 2]. Such signals have high peak to average power ratios (PAPR) and it is a challenge to design an efficient transmitter that meets linearity requirements, especially for signal bandwidths exceeding a few tens of MHz.

1.1 BACKGROUND AND MOTIVATION

1.1.1 COMMUNICATION MODULATED SIGNALS

A simplified block diagram of a transmitter is shown in Fig. 1.1. The desired digital data for transmission is encoded into a baseband or I/Q waveform. The amplitude and phase of a waveform can be used to denote symbols, or series of bits. For example, a 16 symbol quadrature amplitude modulation (16-QAM) is a particular modulation format which has 16 points in the complex plane that represent a single symbol (since

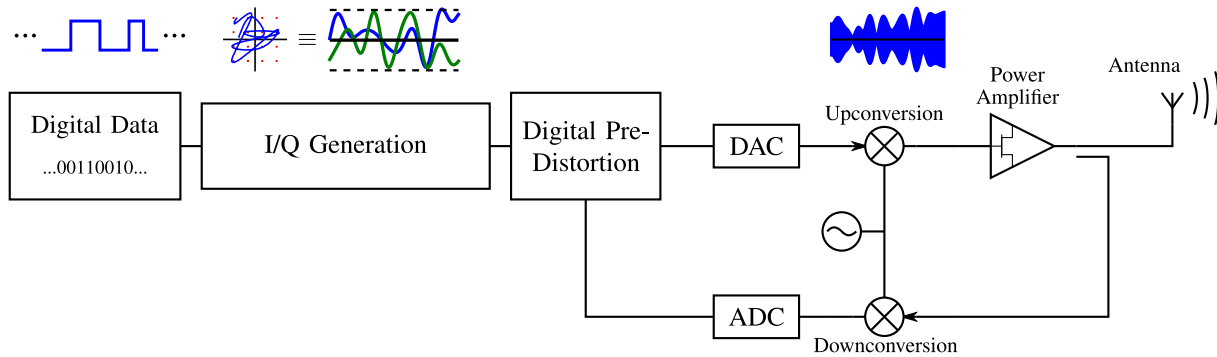


Figure 1.1: Simplified block diagram of a transmitter. A digital signal (0s and 1s) is encoded into a baseband signal, or I/Q, shown here as a 16-QAM. The baseband is then upconverted to RF frequencies and amplified. Finally, the RF signal is transmitted through free space by an antenna. The signal after the power amplifier is coupled, downconverted, and measured to compare to the original waveform. The difference between the original and output is used to inform the digital pre-distortion block.

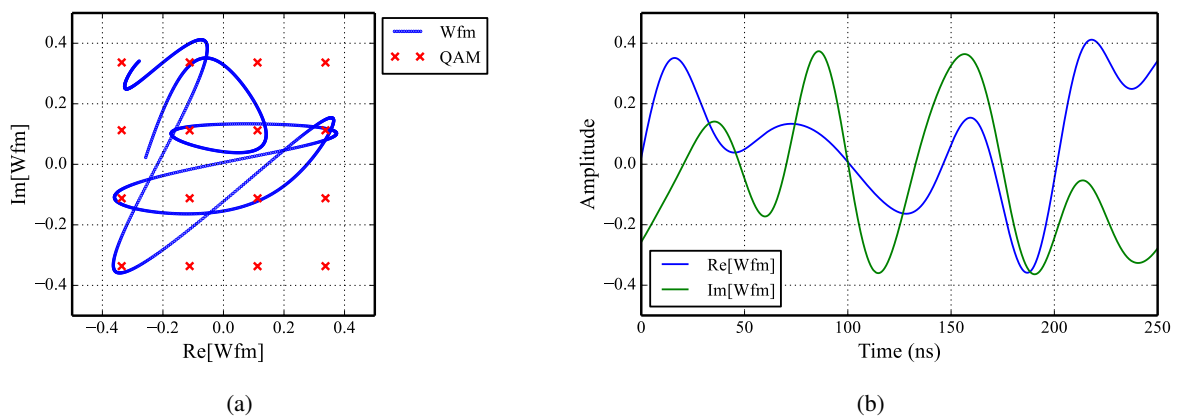


Figure 1.2: (a) Constellation diagram and trajectory of a 10 symbol waveform in 16-QAM modulation. The red x's denote the 16-QAM symbol positions in the complex plane. (b) Time domain waveform of the same signal snapshot in (a).

there are 16 total points, a single symbol represents a 4-bit binary number). Fig. 1.2a shows a 16-QAM constellation (red x's) and an example waveform in the complex plane. The movement in the complex plane from a symbol to another symbol is filtered to bound the frequency content of the signal. The desired filtered waveform of the channel (at the output of the antenna) is usually a root-raised-cosine which also has desirable properties for low inter-symbol-interference. Fig. 1.2b shows the same waveform in the time domain with the real and imaginary parts separate. The real and imaginary parts are known as the I and Q of the waveform. After the baseband I/Q signal is generated, a digital pre-distortion (DPD) algorithm acts on the waveform

to account for the nonlinear effects of the power amplifier. The pre-distorted waveform is then converted to an analog signal and up-converted to an RF frequency. The power amplifier increases the signal amplitude to provide a desired signal power upon radiation. If this amplification process is efficient, it also introduces signal distortion. The coupled path after the power amplifier is used to compare the desired and PA output waveform to inform the DPD algorithm. The signal radiated by the antenna is ideally the desired signal modulated onto an RF carrier.

As data rates increase for communication systems, either the symbol rate must increase (assuming the same baseband modulation format), or the baseband modulation must have a larger number of symbol points (for example 1024-QAM). The first option increases the RF bandwidth of the signal and the second puts stricter requirements on the linearity of the power amplifier. Increasing the symbol rate is not always an option because allocated frequency spectrum bandwidths are limited [3], resulting in more complex baseband modulations to achieve higher communication data rates. While this requires higher linearity for the system (consider more symbol points within the same amplitude range in Fig. 1.2a), this thesis focuses on the effect that a high-complexity baseband modulation has on the efficiency of the RF power amplifier (PA). Efficiency of a PA is defined in this thesis as the power-added-efficiency (PAE):

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{dc}} 100\%, \quad (1.1)$$

where the output, input and dc powers (P_{out} , P_{in} , and P_{dc}) are in watts.

Considering the 16-QAM signal shown in Fig. 1.2a, there are times when the amplitude of the signal is high and other times when the amplitude is low. A typical efficiency versus output power curve for a class-AB amplifier is shown in as the black solid curve in Fig. 1.3. The highest power of the amplifier must be reserved for the high amplitude symbols in Fig. 1.2a; if the amplifier cannot reach the correct amplitude (relative to the other symbol positions), the signal is clipped and the digital data may be lost.¹ This means that the PA is not always operating in peak power or at the highest efficiency when the signal is lower in amplitude. The average power of a particular modulation scheme can be characterized in simulation. Fig. 1.4 shows the complementary cumulative distribution function (CCDF) of various baseband modulations (which is the

¹ A limited amount of clipping is acceptable and is commonly done to increase the efficiency of the amplifier. The DPD algorithm and error correction after reception can mitigate moderately clipped signals.

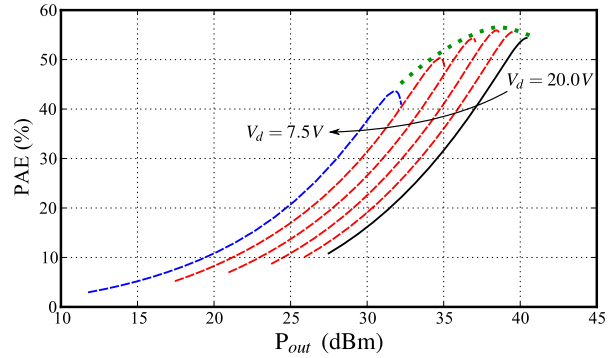


Figure 1.3: Efficiency versus output power of a power amplifier implemented in a 0.15 μm GaN on SiC process. The highest drain supply voltage of 20 V gives the highest output power and >50% PAE. Decreasing the supply voltage shifts the curve to a lower output power with similar efficiency. By changing the supply voltage (green dotted line), high efficiency can be kept while the output power varies with the signal amplitude.

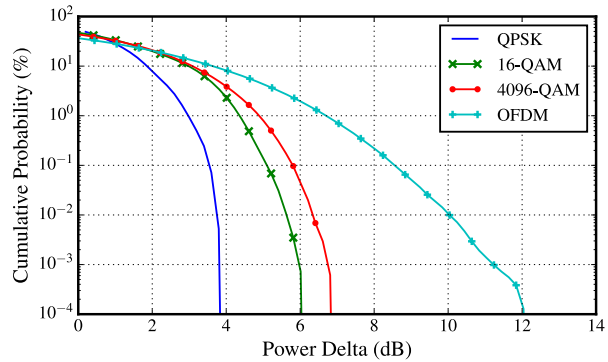


Figure 1.4: Complementary cumulative distribution function of various baseband modulation types. Note that the symbols are passed through a root-raise-cosine filter which modifies the simulated peak-to-average power ratio (PAR) here as compared to the theoretical PAR.

same as the upconverted complex RF waveform entering the PA). All of the digital modulations, QPSK and QAM in the figure, have a root-raised-cosine roll-off factor, α , of 0.35. The CCDF is a measure of the peak power as compared to the average power for long periods of time. Peak power of a particular modulation is usually classified as a probability of reaching that amplitude 0.0001% of the time. Quadrature phase shift keying (QPSK) which is composed of 4 symbols (can be thought as 4-QAM) has a low peak-to-average (PAR) of 3.7 dB. Adding symbols to the modulation increases the PAR to 6 dB for 16-QAM and 7 dB for 4096-QAM. While QPSK and QAM modulations can be used on the RF carrier (after up-conversion) there are multi-carrier modulation types; orthogonal frequency division multiplexing (OFDM) is one type.²

² OFDM can be thought as many narrowband channels that have slow modulation rates. The cumulative data transfer from

However, spectrally efficient modulations, such as LTE or other multi-carrier communication standards, have very high PAR, upwards of 11-12 dB. To amplify a 11 dB PAR signal with the example efficiency curve in Fig. 1.3, on average, the amplifier will be operating around 16% PAE (the efficiency value at 11 dB lower power than the maximum).

1.1.2 RADAR MODULATED SIGNALS

In addition to communication signals, radar signals can also have high PAR waveforms. Spectral masks and increasingly stringent requirements on emissions have limited the use of traditional class-C, rectangular pulse operation which creates large out-of-band emissions [4, 5]. Class-C amplifiers are primarily used in radar systems because of the high efficiency that can be achieved with rectangular pulses which have a constant amplifier saturation level [6]. To limit out-of-band emissions, one method is to shape the output pulse to a spectrally friendly waveform instead of a rectangular pulse [7–9]. A spectrally efficient envelope waveform is a Gaussian pulse which has been demonstrated in [10, 11]. Envelope amplitude modulation however encounters the same issues presented for communication waveforms: increasing the PAR of waveforms lowers the average efficiency of the power amplifier considerably.

1.1.3 TRANSMITTER ARCHITECTURES

To increase the efficiency of the PA in back-off there are various transmitter architectures that have better performance. Two transmitter architectures that address this problem is the Doherty amplifier [12] and outphasing amplifier [13]. Both use various forms of load modulation to add additional peaks in the output power versus PAE curve thereby increasing the efficiency at back-off. A third architecture is supply modulation which varies the bias point of the microwave device to increase efficiency over output power [14].

Doherty (Fig. 1.5) uses biasing with a quarter-wave transformer between two devices to give load modulation over input power. The devices are called the “carrier” and “peaking” amplifier which are biased as class-AB and class-C respectively. For low input powers, the “carrier” amplifier is the primary amplifying

all the channels gives a data rate similar to a single wide bandwidth channel. As such, OFDM has the ability to cope with poor channel conditions and can have much simpler equalization filters. LTE (4G), digital television, WiMAX, and other communication standards use OFDM or variations of OFDM.

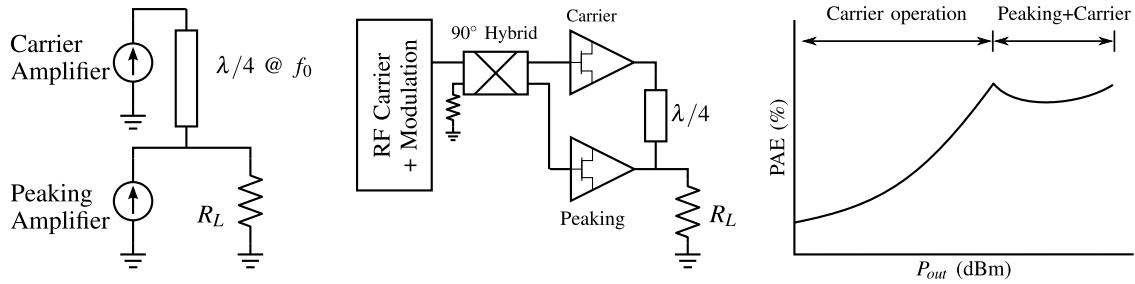


Figure 1.5: Doherty block diagram and operation. The Doherty topology combines two current sources that are out-of-phase by 90° by means of a quarter wave transformer. When the carrier is operating for low input powers, the peaking amplifier is off (ideally open circuit because it is a current source). As input power increases, the peaking amplifier turns on (due to input power) and provides an additional efficiency peak at saturation.

element and has a similar efficiency characteristic to that shown in Fig. 1.3. In this range, the “peaking” amplifier looks like an open circuit since it is pinched-off for class-C operation. As the input power increases, the “peaking” amplifier starts to turn on and when it saturates, gives another efficiency peak as shown in Fig. 1.5. The exact position of the first peak (corresponding to the “carrier” amplifier peaking in efficiency) depends on the relative sizes of the two devices. Since it uses a frequency dependent transformer, Doherty suffers from bandwidth limitations although there have been recent demonstrations with increased bandwidth operation [15, 16].

Outphasing (Fig. 1.6) uses a differential input phase between two amplifiers ($\phi_2 - \phi_1$ in the figure) to create an amplitude variation. The phase-to-amplitude conversion is best considered in a vector plot, shown in the right of Fig. 1.6. Each amplifier output has a certain amplitude, V , and a given phase, ϕ and $-\phi$. Adding the two vector outputs gives a third vector that has a larger amplitude. By varying ϕ , the amplitude of the output, V_{out} can be modified. By using a differential phase, this allows the amplifiers to always operate in a high efficiency operating point (saturated). The design of the combiner network (a Chireix combiner for best efficiency) is critical and determines how the devices load each other as the phase varies and the second efficiency peak for the architecture [17]. The combiner needs to be designed specifically for the loadpull contours of the devices so that the load modulation passes through high-efficiency regions.

The transmitter architecture used in this thesis is supply modulation [14]. Various forms of supply modulation include envelope elimination and restoration (EER) [14], envelope tracking (ET) [18], and

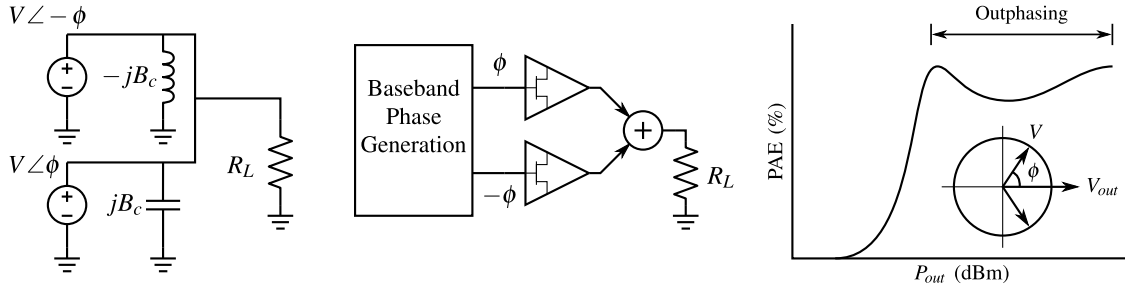


Figure 1.6: Outphasing block diagram. The outphasing topology combines two amplifiers that are fed constant amplitude signals with a differential phase between them, 2ϕ . The difference in phase causes the out-of-phase components to cancel giving a variation in amplitude as shown in the polar plot on the right. With a Chireix combiner (and an appropriate combiner network to align the loadpull contours of the two amplifiers) there is a secondary efficiency peak below the peak power.

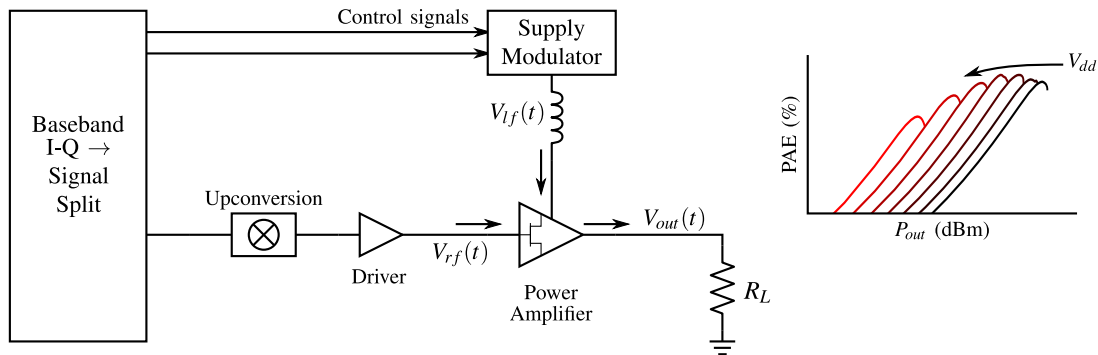


Figure 1.7: Simplified block diagram of a supply-modulated transmitter. In this configuration, the device is under multi-frequency excitation. The $PAE(P_{out})$ variation is shown for *static* V_{dd} , however, this variation of PAE is not necessarily true for a variation in supply voltage ($V_{lf}(t)$).

polar [19–21]. Supply modulation changes the supply voltage of the amplifier to increase the efficiency at lower output powers. Fig. 1.7 shows a general block diagram of a supply-modulated transmitter with an illustration of power-added-efficiency (PAE) versus output power (P_{out}), $PAE(P_{out})$, and its dependence on supply voltage (V_{dd}). Efficiency improvement by supply modulation comes from decreasing wasted dc power when the output power of the RF power amplifier (RFPA) is reduced. This can be seen in the family of supply voltage curves in Fig. 1.3 (dashed lines). As the supply voltage drops, the efficiency curve shifts to a lower output power while keeping a similar peak efficiency. For a 11 dB PAR signal, if the peak can be maintained over output power (dotted green line), the average efficiency is now close to 40% (30 dBm average output power with a 41 dBm peak power) instead of the 16% PAE of a traditional class-AB amplifier. Additionally,

supply modulation has also been shown to be beneficial to Doherty [22] and outphasing PAs [23].

For both Doherty and outphasing, the efficiency boost at back-off comes from specifically designed load modulation that comes (respectively) from sizing the devices in a particular ratio or the Chireix combiner network (which is dependent on the loadpull contours). The efficiency peak at back-off needs to be decided upon and designed into the transmitter which means that Doherty and outphasing transmitters are only optimal for signals of peak-to-average power ratios that its was designed for. On the other hand, supply modulation is a more flexible architecture and can operate under any signal modulation type without having to redesign the transmitter because it operates on modifying the bias for an efficiency boost. Wideband outphasing and Doherty amplifiers are difficult to design as they rely on frequency dependent parameters: a quarter-wave line for Doherty and the frequency dependence of the loadpull contours for outphasing. In contrast, the increase in efficiency for supply modulation is possible over any bandwidth as the supply modulator is concerned with the baseband while the RFPA deals with the carrier frequency. This allows a design of a wide bandwidth RFPA for use in a supply modulated transmitter that would be able to cover many frequency bands for the communication standards around the world. To achieve a high supply modulation transmitter efficiency the power amplifier and supply modulator each need to have high efficiencies.

1.1.3A HIGH-EFFICIENCY POWER AMPLIFIERS

The power amplifier is the primary amplifying element in the transmitter and will consume the most power. It is important to have a high-efficiency amplifier to have a highly efficiency transmitter. Each class of amplifier can be characterized by the voltage and current waveforms at the intrinsic drain of a device. Fig. 1.8 shows the ideal voltage and current waveforms for PA class-B, E, F, and F^{-1} which all have maximum theoretical (drain) efficiencies around 80% and above [24–26]. However, these classes are defined for a set input power: the amount required to give the waveforms shown. Lower input powers no long have the same waveforms and the efficiencies are lower, sometimes significantly. In fact, these high-efficiency amplifier modes nominally are “pinched-off” and have little to negative gain for small input powers (small-signal). The PAE curve for pinch-off devices in back-off would be worse because it lacks the gain that a more linear class-A or AB amplifier would have for small-signal input powers.

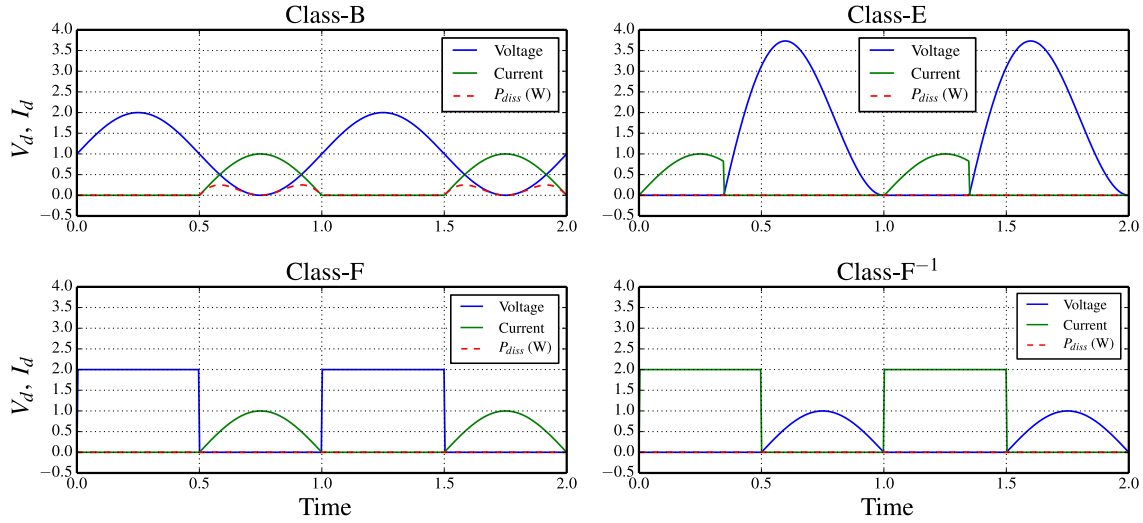


Figure 1.8: Ideal intrinsic drain voltage and current waveforms for class-B, E, F, and F^{-1} . Class-B has a small amount of power dissipation limiting the maximum efficiency. The other classes have no power dissipation giving a drain efficiency of 100%.

1.1.3B HIGH-EFFICIENCY SUPPLY MODULATORS

The supply modulator necessarily also needs to be highly efficient. The most straightforward efforts are based on buck converters with pulse-width modulation at very high sampling rates. Buck converters rely on switching very quickly with pulse-width-modulation (PWM) and filtering the output to give an average dc value that depends on the duty-cycle of the PWM [27]. There have been significant efforts in GaN integrated supply modulators to allow higher switching rates and higher breakdown voltages for increased power handling [28, 29]. Switchers with integrated gate drivers in the TriQuint $0.15\ \mu\text{m}$ RF GaN on SiC process have demonstrated over 90% peak efficiency, at up to 200 MHz switching frequency and up to 15 W peak power. Other, and more recent, efforts have investigated discrete voltage supply modulation which include multi-level or PowerDAC methods [30]. Although very efficient, discrete voltage level supply modulation requires significantly more signal conditioning and DPD as it must account for the large steps in gain and power that are caused by sudden changes in the drain bias voltage.

1.2 PREVIOUS RESEARCH IN MULTI-TONE MEASUREMENTS

Related previous work can be found in papers on low frequency measurements for device characterization [31–38], baseband impedance investigation for linearity [39–43], and bias line instabilities [44, 45]. Very few systems have been designed to characterize transistors under drive while simultaneously measuring or monitoring baseband (<500 MHz) performance or properties.

1.2.1 LF MEASUREMENT OF RF DEVICES FOR NONLINEAR MODELING

For literature in device characterization, device behavior at frequencies less than 1 MHz is important for accurate transistor modeling that takes into account thermal and trapping effects. In [31, 46], it is shown that low frequency 5 Hz to 1 GHz S-parameters of GaN transistors can be used to separate trapping from thermal effects. In [32, 33], active bias tees with very high low frequency impedances were implemented from about 5 Hz to 1 MHz to measure low frequency dispersion. Another application of LF in device characterization is the use of the baseband signal to control the RF impedance of a loadpull setup [35]. Here the baseband I/Q are used as the feedback in a closed loop active loadpull setup. More advance setups involve active envelope frequency loadpull to present a constant impedance across the baseband frequencies [36, 47].

1.2.2 LF MEASUREMENT FOR INVESTIGATING BASEBAND EFFECTS ON LINEARITY

To investigate baseband effects on linearity, a time-domain measurement on a 835 MHz class-B PA under two-tone excitation showed that there is an optimal IF impedance for linearity [39]. Gate voltage dependence and tone separation was investigated in [40], while [41] implements a control circuit to change the baseband impedance. A 6-port reflectometer was developed in [42] so that the baseband impedance can be varied, with variable gate and drain biases. While [39–42] showed useful data for linearity investigations, the results are usually limited to a single-tone RF excitation and no injected power into the drain/collector of the transistor.

A few papers monitor and control the low frequency stability of a transistor by varying capacitance and/or resistance values on the bias line [44, 45]. The methods presented in these papers accurately measure and account for bias line instabilities but are specific to the measured PA module and do not give any information

on the low frequency parameters of the transistor themselves.

1.2.3 CHARACTERIZATION FOR SUPPLY MODULATION

There are very few papers that characterize a device at the baseband and carrier frequency simultaneously for supply modulation. A basic mixer-like transfer function to model inter-modulation products mixed from a baseband injection at the drain was created in [48]. Also, efforts have been made to measure and model the nonlinear current source of a transistor by simultaneously exciting LF (<10 MHz) and RF on the gate of the device and measuring response at LF and RF [49–51].

A different set of papers investigate the possibility for taking advantage of the drain impedance at baseband frequency to provide “self-modulation” [52, 53]. A resonant network is placed on the bias line network of the power amplifier to provide a large voltage at high RF input powers.

A series of papers by a research group at Cardiff University investigate the effect of the baseband impedance on the performance of the PA at RF frequencies. The effect of the baseband impedance on ACPR (adjacent channel power ratio) for signals under 10 MHz in bandwidth initially was explored in [54] by injecting a waveform at the drain to present an arbitrary impedance. The paper found that the optimum impedance is a short-circuit for all baseband impedances. The impedance of the device itself was not explored. Another paper by the same group presents a method for linearization of a signal using a baseband injected signal [55]. An iterative software control loop was used to optimized the baseband injected waveform. The method for optimization and the resulting coefficients needed were not presented in detail leaving a gap between the voltage injection needed (presented impedance to the transistor) and the corresponding RF waveform. A follow up paper states that the coefficients at baseband are frequency independent [56]. However, the paper only presents a single RF waveform which leaves the same question as the previous paper: how does the RF waveform interact with the baseband impedance. A different paper measures a class-AB and class-F PA while under CW and injecting a waveform at baseband to linearized the waveform (flat gain and linear AM-PM distortion) [57, 58]. Aside from the lack of modulated signal measurements, the paper makes an incorrect assumption that, because it can be linearized with a CW measurement, a wideband signal will have the same linearity correction coefficients. The results from these papers contradict the

results from [39] and [42] for the optimum baseband impedance presented to the transistor for linearity and efficiency (both are impedances other than a short-circuit). This thesis has results showing that the relative phase between RF tones changes the baseband voltage that is mixed down. This means that the waveforms to linearize as presented in [54, 55] are specific to the RF signal.

The work in this thesis focuses on measurement and theory to describe the operation of a microwave transistor under baseband supply modulation. Measurements of the broadband drain supply impedance are performed while the PA is under normal large-signal operating conditions, possibly with modulation, and with low frequency power injected into the drain to model supply modulation. Both a single transistor and an amplifier are tested. The RF performance and LF impedance are measured in a nominal operating condition under multi-frequency excitation, which is an important difference from previous reported work. In addition to measurements, describing functions, nonlinear tool for analysis of elements, is developed to explain a couple of the measurements performed.

1.3 THESIS CONTENTS

This thesis focuses on three major topics related to supply modulation: nonlinear measurement, nonlinear theory, and nonlinear design. A measurement bench (Chapter 2) and numerous measurements are presented (Chapter 3 and Chapter 4) which covers nonlinear measurement of supply modulation. For nonlinear theory, describing functions are developed to explain some of the trends seen in the measurements in Chapter 5. Finally, Section 6.3 details a MMIC design specifically for supply modulation for nonlinear design.

- Chapter 1 introduces the concept of supply modulation and gives motivation why it is useful for communication and radar transmitters.
- Chapter 2 details the measurement bench for characterizing a device that is placed in a large-signal operating mode with the RF and simultaneously exciting the device on the drain to simulate supply modulation. Components used in the setup are discussed and a full calibration with equations is detailed.

- Chapter 3 presents measurements of two GaN devices in the TriQuint 0.15 μm process.
- Chapter 4 presents measurements of a power amplifier designed in the TriQuint 0.15 μm process. The same amplifier is used in a resonant modulator transmitter and interactions between the amplifier and supply modulator is discussed.
- Chapter 5 introduces the describing function method for analysis of nonlinear elements. Describing functions are then extended to electrical elements for multiple sinusoidal input and multi-dimensional nonlinearities.
- Chapter 6 discusses the pertinent information in this thesis and how it relates to supply modulated transmitters. A MMIC design specific to supply modulation is discussed. In particular, design decisions related to enabling wide bandwidth modulation are detailed. Finally, significant contributions and future work are also outlined.

The appendices detail some aspects of the thesis which would not have fit within the flow of the main text. Additionally, appendices B and D were done out of personal curiosity:

- Appendix A shows a coaxial calibration of the measurement setup. It is pertinent to show the accuracy of the measurement setup coaxially because most measurement instruments are calibrated coaxially. Comparisons to industry calibrated instruments are made.
- Appendix B derives relations for active impedance loadpull. These derivations are important for future steps as a device being driven with a wide bandwidth RF signal has mixing products at low frequency. The supply modulator will see this power and can present a particular wideband impedance using the equations presented.
- Appendix C details the Angelov model used in Chapter 5.
- Appendix D derives even and odd mode S-parameters for use in MMIC combiner networks. However, the theory is generalized so it can be used for any S-parameter network.
- Appendix E contains selected code used within this thesis.

CHAPTER 2

LF/RF MEASUREMENT BENCH

CONTENTS

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Simultaneous measurement of the low frequency (LF) and RF performance of a device requires careful consideration of equipment, components, and calibration in two disparate frequency ranges. This chapter will cover both the bench-top equipment, passive components used, and full calibration of the 2-port LF/RF setup. Most of the components are commercial, however, a frequency diplexer distinguishing between the LF in a wide bandwidth and the RF signal was designed for the measurement setup. As a result of the particular instruments being used, calibration consists of two distinct frequency ranges: LF from 0-500 MHz and RF at 10 GHz. At RF frequencies, a standard S-parameter power offset calibration is used. At low frequency, the calibration consists of two parts: an absolute coaxial calibration and a relative calibration to the probe tip plane.

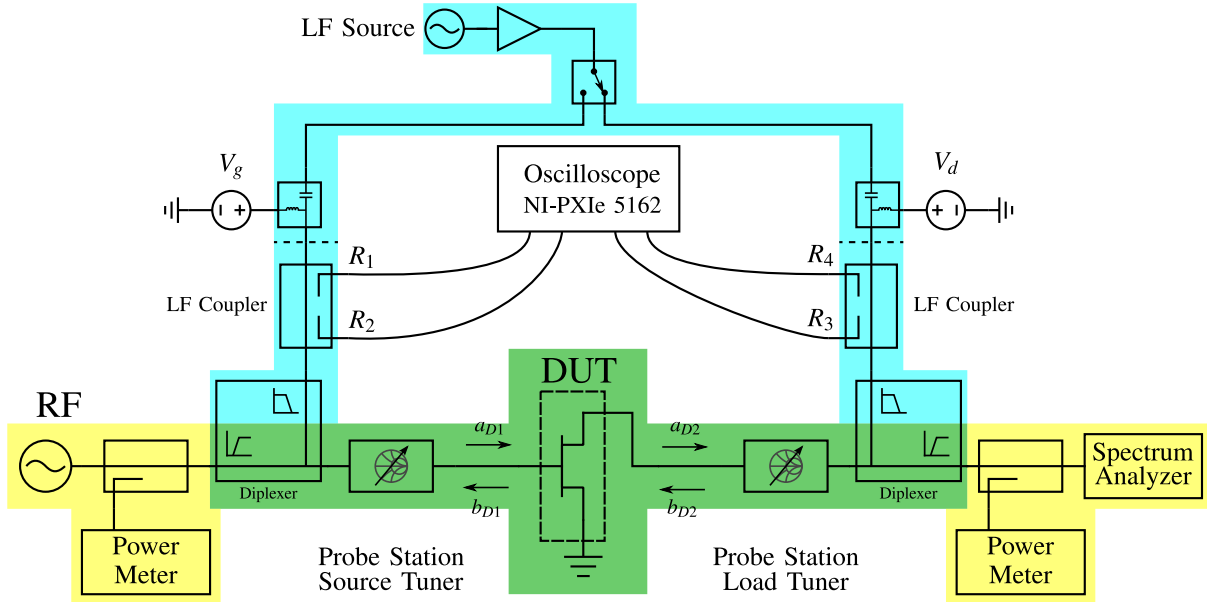


Figure 2.1: Simplified diagram of measurement setup for a transistor. The RF path uses power sensors to measure the performance of a device under test (DUT) under normal operating conditions. The tuners present RF loads to the DUT and are approximately short 50Ω transmission lines at low frequencies ($<1\text{GHz}$). The LF path generates a low frequency signal and includes biasing for the drain of the DUT. A coupler with an oscilloscope measures the forward and backward wave parameters of the LF path. The RF and LF paths are split with diplexers bias tee that differentiates the RF and LF signals. The DUT shown in the figure is a transistor, but can also be a power amplifier.

2.1 MEASUREMENT SETUP OVERVIEW

The test system shown in Fig. 2.1 was developed to measure low frequency impedances over a wide bandwidth ($\sim 0.010\text{-}500\text{ MHz}$) while simultaneously measuring the large-signal RF (10 GHz) performance of a device under test (DUT). The colors represent various overlapping frequency domains. The yellow is the RF path, the cyan is the LF path, and the green is the combined RF/LF path. A spectrum analyzer distinguishes multiple tones at RF frequencies in the RF path. Fundamental frequency tuners are used to adjust the RF loading of the transistor. In the low frequency path, an oscilloscope is used to acquire the time-domain waveform. The oscilloscope is the National Instruments NI PXIe-5162 which has 10-bit resolution with 1.25 GS/s real time simultaneous sampling on four channels. The sample rate is controllable with an external clock input and internal rate multipliers and dividers. The four coupled voltage waveforms ($R_1\text{-}R_4$) are digitized and the Fourier transform taken to find the voltage variable (which will be denoted as a_{R_i} and b_{R_i})

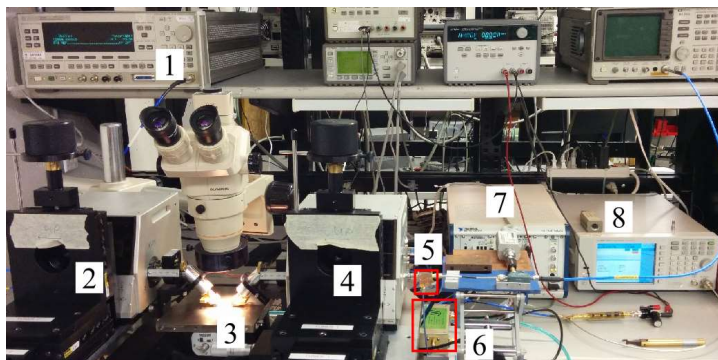


Figure 2.2: Photograph of setup with labeled 1) RF source, 2) gate tuner, 3) probe station with DUT, 4) drain tuner, 5) bias tee, 6) low frequency coupler, 7) oscilloscope, 8) low frequency source.

which can then be converted to pseudo-wave parameters [59]. The reference calibration impedance will be a $50\ \Omega$ load as a TRL calibration at low frequencies is infeasible. The LF signal is generated by a generic RF generator and amplified with a JDS Uniphase H301 optical modulator driver with 24 dB of gain down to 75 kHz. This allows a RF signal generator to provide a low frequency signal up to the bandwidth of the bias tee. The components above the dotted line in the LF path (cyan) can be replaced (without re-calibration) with a supply modulator which replicates the functions of bias tee and LF signal. A photograph of the setup is shown in Fig. 2.2.

The RF carrier frequency used in this measurement setup is 10 GHz, which is far from the LF of <500 MHz. This allows simpler filter design of the bias tee to differentiate the RF and LF signals.

2.1.1 BIAS NETWORK / LF COUPLER

Measurements at low frequency (<10 MHz) for microwave applications are difficult because of the desired 4+ decade bandwidth requirements (50 kHz-500 MHz) [32,33]. How does one observe/measure the performance of a circuit with a minimal amount of disruption? At higher frequencies this is easily solved by using a coupler; it allows the signal through it while coupling a small amount of power for measurement. Because of the large wavelengths at low frequencies, coupling a small amount of power can only be reliably done (in a wide bandwidth) with resistive components. However, a resistive coupling network presents a slew of other problems. In this particular case, the drain bias network needs to handle >300 mA of current (more if testing a power amplifier instead of a single transistor) requiring the resistors to be stable over temperature.

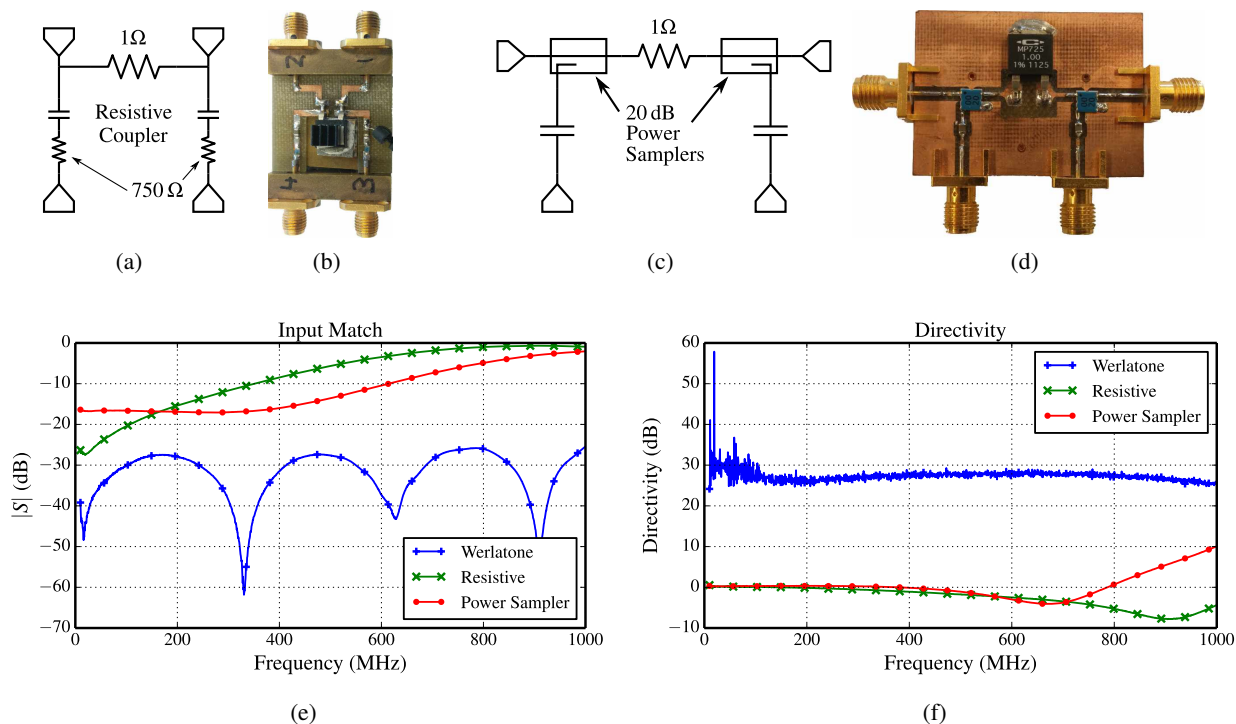


Figure 2.3: (a)-(d) Examples of resistive couplers using a $1\ \Omega$ resistor and either a large resistance or power samplers on the coupled ports. (e) Input match and (f) directivity comparison of the three coupling components including the wideband commercial Werlatone coupler.

Additionally, the dc voltage drop across the resistor requires additional compensation with instruments. Two resistive coupler networks, summarized in Fig. 2.3, were created and tested: a resistive coupler with large “coupling” resistors; and a coupler with a commercial 20 dB surface mount power sampler. The input match for the resistive couplers ($|S_{11}|$) is <15 dB but quickly degrades for higher frequencies. The directivity for both resistive couplers is around 0 dB which is not sufficient since the coupled port 1 wave is not isolated from the coupled port 2 wave, thus increasing error of the measurements.

Fortunately, a commercial directional coupler from Werlatone [60] that operates down to 10 kHz with 30 dB of coupling was used with the measured performance shown in Fig. 2.3. The input match is excellent over the entire bandwidth, and the directivity is around 25 dB. Two of these couplers are used to make the 2-port measurement system presented in this thesis.

With 10-bit resolution from the oscilloscope, the voltage bins are approximately $50\ \mu\text{V}$ (at 0.05 V pk-pk vertical scale) which is -82 dBm of power into a $50\ \Omega$ termination. Adding 30 dB of coupling gives a

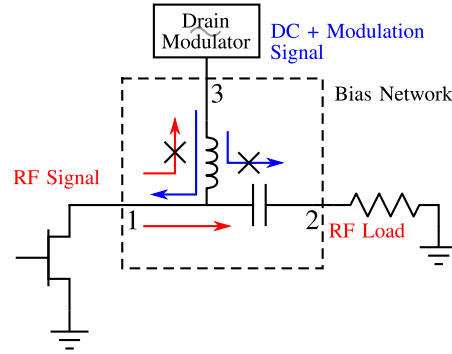


Figure 2.4: Diplexer simplified diagram showing the directions and blocking of the RF (red) and LF (blue) frequency paths.

theoretical minimum power through the LF path of -52 dBm. The maximum voltage into the PXIe-5162 oscilloscope is 5 V, giving an absolute maximum dynamic range of approximately 100 dB. Crosstalk within the instrument and the ADC spurs will reduce the dynamic range of the instrument to around 60 dB, as found with a rough power sweep measurement. Higher powers can be measured by adding attenuators on the coupled ports of the bidirectional coupler.

2.1.2 DIPLEXER

The diplexer is of particular interest for wide bandwidth signals as it must be designed to pass the low frequency content to the transistor while blocking the same content from leaking out to the RF load as shown by the red (RF signal) and blue (LF signal + dc) in Fig. 2.4. It effectively acts as a bias network with a wide bandwidth dc path, and is designed as a parallel combination of a small dc blocking capacitor (in the RF path) and a 7th order low-pass filter (in the LF path). The expected maximum current and voltage to pass through the low frequency path is 400 mA and 20 V. The maximum expected RF power is 5 W, which is well below the maximum ratings of the surface mount capacitors and inductors. The bandwidth of the low-pass filter is 1 GHz which is adequate to pass large bandwidth envelope signals. A small blocking capacitor is necessary to isolate the RF load from the LF signal. As the low-pass filter requires large inductance and capacitance values, parasitic reactances of the elements causing resonances in the RF band are the primary limitation for a wide bandwidth bias tee. Additional elements (an inductor and capacitor) were used in the RF path to help flatten the frequency response in the RF band. A photograph of the bias tee is shown in Fig. 2.5 along with

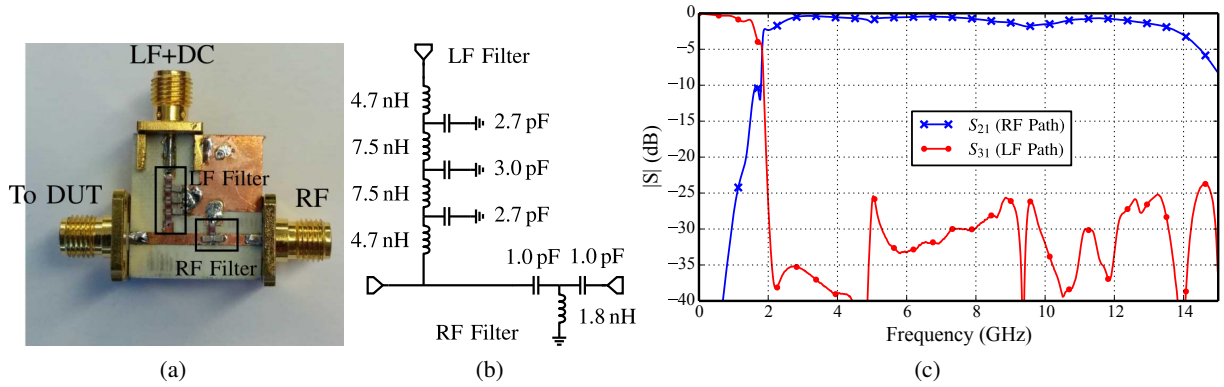


Figure 2.5: (a) Photograph and (b) circuit diagram of wideband bias tee which operates as a diplexer. (c) Measured performance of the bias tee.

its measured S-parameters. There is 1 dB of insertion loss through the RF path and <0.3 dB loss through the LF path. The match is better than 40 dB at LF and 10 dB at 10.7 GHz. This performance is adequate for LF measurements with 500 MHz bandwidth presented in this thesis.

2.2 LF CALIBRATION

The calibration setup in which the DUT is on-chip and contacted through a probe station involves two distinct calibrations (coaxial and probe tip) which are then combined to de-embed to the DUT reference plane in an absolute manner. Referring to Fig. 2.1, calibration to the coaxial reference plane located at one of the dotted lines in the LF path, includes a relative calibration and absolute calibration. The probe tip calibration only involves a relative calibration, such as for a traditional VNA, where ratios of measurements only allow for characterization of the impedance transfer of a device. Both impedance and other network parameters (i.e. S-parameters) are ratios of parameters; either voltage or current. Absolute calibration allows the computation of voltage or current individually, at the reference plane.

Fig. 2.6 shows a network diagram for a coupler-based LF measurement setup. The boxes represent error networks that need to be de-embedded and in the probe station setup, include the RF tuners, probes, diplexer, and couplers (from dotted line to dotted line in Fig. 2.1). The desired incident and reflected pseudo-wave parameters at the DUT are denoted by a_D and b_D respectively. The definition of pseudo-waves used in this

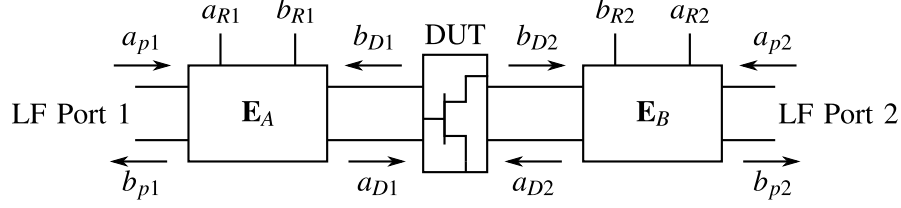


Figure 2.6: Block diagram of a general measurement setup with two unique measured parameters (a_R and b_R) on each port. The generator ports (a_p and b_p) can be the source of RF power or a termination. The DUT waves, a_D and b_D , are the desired parameters found through calibration.

thesis are:

$$a_i = \frac{\sqrt{\text{Re}[Z_{\text{ref}}]}}{2|Z_{\text{ref}}|} (v_i + i_i Z_{\text{ref}}) \quad b_i = \frac{\sqrt{\text{Re}[Z_{\text{ref}}]}}{2|Z_{\text{ref}}|} (v_i - i_i Z_{\text{ref}}) \quad (2.1)$$

$$v_i = \frac{|Z_{\text{ref}}|}{\sqrt{\text{Re}[Z_{\text{ref}}]}} (a_i + b_i) \quad i_i = \frac{1}{Z_{\text{ref}} \sqrt{\text{Re}[Z_{\text{ref}}]}} (a_i - b_i) \quad (2.2)$$

where the port is indicated by the subscript, i , and Z_{ref} is the reference impedance. The measured voltage variables are a_R and b_R , which represent the forward coupled wave and backward coupled waves with respect to the DUT. The generator and load port pseudo-waves are denoted by the a_p and b_p waves. Any circuitry or networks external to the RF ports do not play a role in the calibration and can be ignored. As a side note, this presents interesting possibilities to exchange RF sources and terminations external to the diagram in Fig. 2.6 (or above the dotted lines in Fig. 2.1) without having to recalibrate. The DUT can be any device or passive network.

The parameters are denoted by waves, a and b , but these deserve some further discussion. The measured variables a_R and b_R are not truly wave parameters (hence are called variables instead of waves) as there is no instrument that can directly measure voltage/power waves. The physical measurement is most often the digitization of a voltage, whether in a continuous manner by an ADC (oscilloscope) or by subsampling. The two measurements, a_R and b_R , can be of any parameter as long as they are *unique*; it can be measurement of voltage and current at a node or two voltages at different nodes but not two voltages at the same node. The digitized measurements are the mathematical window to the physical DUT wave parameters through the use of the calibration matrices. The use of a bidirectional coupler (assuming good directivity) for the setup described in Section 2.1 allows the use of an oscilloscope to digitize voltages for the measurement parameters a_R and b_R .

The calibration closely follows [61, 62] for the probe station calibration. However, the type of relative calibration and method for phase calibration is modified for the equipment used here.

2.2.1 SOLT / SOLR AT LF

The goal of the calibration is to determine waves a_{Di} and b_{Di} from the measured variables a_{Ri} and b_{Ri} as shown in Fig. 2.6. The measured variables denoted by the subscript R are captured with an oscilloscope which digitizes a time domain voltage waveform which is then Fourier transformed to find the frequency components. The relative calibration parameters can be found by any traditional calibration routine such as SOLT, SOLR [63], LRM [64], and TRL [65] among others [66, 67]. However, considering the frequency range of interest here (dc-500 MHz), any calibration that requires a specific length of transmission line (e.g. TRL), becomes unfeasible at low frequencies. Therefore, SOLT is covered in detail and an extension to SOLR is made. The only difference between the two is that one has a known defined *thru* standard while the other only requires rough knowledge of the phase of the *thru* standard.

The error parameter model has 7 relative calibration parameters, β_1 , γ_1 , δ_1 , α_2 , β_2 , γ_2 , δ_2 , and one absolute calibration parameter, K :

$$\begin{pmatrix} a_{D1} \\ b_{D1} \\ a_{D2} \\ b_{D2} \end{pmatrix} = K \begin{bmatrix} 1 & \beta_1 & 0 & 0 \\ \gamma_1 & \delta_1 & 0 & 0 \\ 0 & 0 & \alpha_2 & \beta_2 \\ 0 & 0 & \gamma_2 & \delta_2 \end{bmatrix} \begin{pmatrix} a_{R1} \\ b_{R1} \\ a_{R2} \\ b_{R2} \end{pmatrix}. \quad (2.3)$$

The absolute parameter is complex and as such contains information about the absolute magnitude and phase of a waveform. The first 3 calibration parameters, β_1 , γ_1 , and δ_1 , are found by a *short-open-load* calibration routine (SOL). The upper left corner of (2.3) is used to relate the measured variables and DUT waves,

$$\begin{pmatrix} a_{D1} \\ b_{D1} \end{pmatrix} = K \begin{bmatrix} 1 & \beta_1 \\ \gamma_1 & \delta_1 \end{bmatrix} \begin{pmatrix} a_{R1} \\ b_{R1} \end{pmatrix}. \quad (2.4)$$

Equation (2.4) can be solved for the ratio of a_{D1} and b_{D1} ,

$$\Gamma_{std} = \frac{b_{D1,std}}{a_{D1,std}} = \frac{\gamma_1 a_{R1,std} + \delta_1 b_{R1,std}}{a_{R1,std} + \beta_1 b_{R1,std}}. \quad (2.5)$$

where $_{std}$ denotes the measured wave parameter with the standard with a reflection coefficient of Γ_{std} connected to the DUT reference plane. Using three known calibration standards, three equations result and can be assembled as a matrix and solved for the calibration parameters:

$$\begin{bmatrix} \Gamma_S b_{R1,S} & -a_{R1,S} & -b_{R1,S} \\ \Gamma_O b_{R1,O} & -a_{R1,O} & -b_{R1,O} \\ \Gamma_L b_{R1,L} & -a_{R1,L} & -b_{R1,L} \end{bmatrix} \begin{pmatrix} \beta_1 \\ \gamma_1 \\ \delta_1 \end{pmatrix} = \begin{pmatrix} -\Gamma_S a_{R1,S} \\ -\Gamma_O a_{R1,O} \\ -\Gamma_L a_{R1,L} \end{pmatrix}. \quad (2.6)$$

Another SOL calibration can be done using (2.6) for port 2 to give “relative” parameters for the lower right half of (2.3). The parameters are “relative” because the SOL calibration assumes that $\alpha_2 = 1$. The relationship between the two is given by

$$\begin{bmatrix} \alpha_2 & \beta_2 \\ \gamma_2 & \delta_2 \end{bmatrix} = k \begin{bmatrix} 1 & \beta_{r2} \\ \gamma_{r2} & \delta_{r2} \end{bmatrix} \quad (2.7)$$

where k is the scaling parameter. Each port is now calibrated as a 1-port and the next step is to determine the scaling k between the two 1-port error parameters. This is done by measuring a transmission standard (passive element that has low reflection and loss). Two common methods are to use a known line (*short-open-load-thru* or SOLT) or an unknown reciprocal network (*short-open-load-reciprocal*, “unknown thru”, or SOLR).

2.2.1A SOLT

SOLT is the simpler of the two calibrations where the *thru* line has a pre-defined delay. For a *thru*, the waves at the DUT reference plane can be related by the T-parameters of the *thru* standard,

$$\begin{pmatrix} b_{D1} \\ a_{D1} \end{pmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{pmatrix} a_{D2} \\ b_{D2} \end{pmatrix}. \quad (2.8)$$

Exchanging the DUT reference plane parameters with the measured wave parameters using (2.3) and solving for k gives:

$$b_{D1,T} = (\gamma_1 a_{R1,T} + \delta_1 b_{R1,T}) = T_{11}k(a_{R2,T} + \beta_{r2}b_{R2,T}) + T_{12}k(\gamma_{r2}a_{R2,T} + \delta_{r2}b_{R2,T}) \quad (2.9)$$

$$k = \frac{\gamma_1 a_{R1,T} + \delta_1 b_{R1,T}}{T_{11}(a_{R2,T} + \beta_{r2}b_{R2,T}) + T_{12}(\gamma_{r2}a_{R2,T} + \delta_{r2}b_{R2,T})} \quad (2.10)$$

Using (2.6)-(2.7), and (2.10) gives a complete relative SOLT calibration. It is important to note that the calibration is performed defining the reference impedance as the Γ_L reference standard (making the final wave parameters pseudo-waves instead of traveling-waves), in most cases $50\ \Omega$. For a zero-length *thru*, $T_{11} = T_{22} = 1$ and $T_{12} = T_{21} = 0$:

$$k = \frac{\gamma_1 a_{R1,T} + \delta_1 b_{R1,T}}{a_{R2,T} + \beta_{r2} b_{R2,T}} \quad (2.11)$$

2.2.1B SOLR

While [63] was cited as the original incarnation of SOLR, the paper is confusing because of mixed and redundant definitions. A consistent derivation is presented here. As noted in the paper, the requirements to perform this calibration are:

- (1) The unknown *thru* is reciprocal; and
- (2) Knowledge of the unknown *thru* S_{21} phase to within 180 degrees.

The first requirement is simple to meet considering a passive network is reciprocal assuming it has no magnetic materials. Since the wave directions are not consistent for each network as shown in Fig. 2.6, the T-parameters for each defined explicitly are:

$$\begin{pmatrix} b_{R1} \\ a_{R1} \end{pmatrix} = \begin{bmatrix} E_{11}^A & E_{12}^A \\ E_{21}^A & E_{22}^A \end{bmatrix} \begin{pmatrix} b_{D1} \\ a_{D1} \end{pmatrix}, \quad (2.12)$$

$$\begin{pmatrix} b_{D1} \\ a_{D1} \end{pmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{pmatrix} a_{D2} \\ b_{D2} \end{pmatrix}, \quad (2.13)$$

$$\begin{pmatrix} a_{D2} \\ b_{D2} \end{pmatrix} = \begin{bmatrix} E_{11}^B & E_{12}^B \\ E_{21}^B & E_{22}^B \end{bmatrix} \begin{pmatrix} a_{R2} \\ b_{R2} \end{pmatrix}. \quad (2.14)$$

\mathbf{E}_A and \mathbf{E}_B are error matrices as shown in Fig. 2.6. This means that the \mathbf{E}_A error matrix (upper left of (2.3)) *cannot* be substituted in for (2.12): the inverse must be taken first and the terms diagonal each other swapped. The wave directions for (2.14) match the directions in (2.3), and cascading these results in the total measurement matrix,

$$\mathbf{T}_m = \ell \mathbf{E}_A \mathbf{T}_u \mathbf{E}_B, \quad (2.15)$$

where \mathbf{T}_u are the T-parameters of the unknown *thru* and $\ell = S_{21}^A/S_{21}^B$. The origin of ℓ can be seen by reformatting the error networks to S-parameters:

$$\mathbf{T}_m = S_{21}^A \begin{bmatrix} -\Delta^A & S_{11}^A \\ -S_{22}^A & 1 \end{bmatrix} \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \frac{1}{S_{21}^B} \begin{bmatrix} -\Delta^B & S_{11}^B \\ -S_{22}^B & 1 \end{bmatrix}, \quad (2.16)$$

where $\Delta^x = S_{11}^x S_{22}^x - S_{21}^x S_{12}^x$ and the S_{21}^A term is inverse of the S_{21}^B because of the reformatting of the wave directions needed for (2.12). The full test-set T-parameters, \mathbf{T}_m , can be calculated directly with two measurements: one with a forward wave excitation and the other with a backward wave excitation, denoted here by *fwd* and *rev* respectively:

$$b_{R1}^{fwd} = T_{11} a_{R2}^{fwd} + T_{12} b_{R2}^{fwd} + \quad (2.17)$$

$$a_{R1}^{fwd} = \quad + T_{21} a_{R2}^{fwd} + T_{22} b_{R2}^{fwd} \quad (2.18)$$

$$b_{R1}^{rev} = T_{11} a_{R2}^{rev} + T_{12} b_{R2}^{rev} + \quad (2.19)$$

$$a_{R1}^{rev} = \quad + T_{21} a_{R2}^{rev} + T_{22} b_{R2}^{rev} \quad (2.20)$$

The previous equations can be represented as a matrix and solved for the unknown T-parameters:

$$\begin{pmatrix} T_{11} \\ T_{12} \\ T_{21} \\ T_{22} \end{pmatrix} = \begin{bmatrix} a_{R2}^{fwd} & b_{R2}^{fwd} & 0 & 0 \\ a_{R2}^{rev} & b_{R2}^{rev} & 0 & 0 \\ 0 & 0 & a_{R2}^{fwd} & b_{R2}^{fwd} \\ 0 & 0 & a_{R2}^{rev} & b_{R2}^{rev} \end{bmatrix}^{-1} \begin{pmatrix} b_{R1}^{fwd} \\ b_{R1}^{rev} \\ a_{R1}^{fwd} \\ a_{R1}^{rev} \end{pmatrix} \quad (2.21)$$

In terms of the unknown *thru* matrix, \mathbf{T}_{thru} ,

$$\mathbf{T}_{thru} = \ell^{-1} \mathbf{E}_A^{-1} \mathbf{T}_m \mathbf{E}_B^{-1}. \quad (2.22)$$

The determinant of (2.16) can be taken and solved for ℓ , using requirement (1) that the network is reciprocal ($\det(\mathbf{T}_{thru}) = 1$):

$$\det(\mathbf{T}_m) = \ell^2 \det(\mathbf{E}_A) \det(\mathbf{T}_{thru}) \det(\mathbf{E}_B) \quad (2.23)$$

$$\ell = \pm \sqrt{\frac{\det(\mathbf{T}_m)}{\det(\mathbf{E}_A) \det(\mathbf{E}_B)}} \quad (2.24)$$

It is critical that the square root is computed in a geometric way.¹ There is a sign ambiguity that must be determined. Except for ℓ , most of (2.22) can be computed as

$$\mathbf{X} = \mathbf{E}_A^{-1} \mathbf{T}_m \mathbf{E}_B^{-1}. \quad (2.25)$$

Comparing the $_{22}$ parameter of (2.22) (in terms of S-parameters) and (2.25):

$$\frac{1}{S_{21}^{thru}} = \frac{X_{22}}{\ell} \quad (2.26)$$

The sign of ℓ can now be chosen such that the phase S_{21}^{thru} is closest to the expected value for the unknown *thru* standard. Now the T-parameters of the *thru* standard are known from (2.22). The full T-parameter matrix of the *thru* is used with (2.10) to find the appropriate scaling constant, k , between the upper left and lower right parts of (2.3).

2.2.1C S-PARAMETER EXTRACTION

As a side note, in a similar method to (2.21), S-parameters of a DUT can be measured. Either the raw measurements (a_{Ri}) or the de-embedded waves (a_{Di}) can be used (the same is true for (2.21)).

$$b_{D1}^{fwd} = S_{11}a_{D1}^{fwd} + S_{12}a_{D2}^{fwd} + \quad (2.27)$$

$$b_{D2}^{fwd} = \quad + S_{21}a_{D1}^{fwd} + S_{22}a_{D2}^{fwd} \quad (2.28)$$

$$b_{D1}^{rev} = S_{11}a_{D1}^{rev} + S_{12}a_{D2}^{rev} + \quad (2.29)$$

$$b_{D2}^{rev} = \quad + S_{21}a_{D1}^{rev} + S_{22}a_{D2}^{rev}, \quad (2.30)$$

which can be represented as a matrix and solved for the unknown S-parameters:

$$\begin{pmatrix} S_{11} \\ S_{12} \\ S_{21} \\ S_{22} \end{pmatrix} = \begin{bmatrix} a_{D1}^{fwd} & a_{D2}^{fwd} & 0 & 0 \\ a_{D1}^{rev} & a_{D2}^{rev} & 0 & 0 \\ 0 & 0 & a_{D1}^{fwd} & a_{D2}^{fwd} \\ 0 & 0 & a_{D1}^{rev} & a_{D2}^{rev} \end{bmatrix}^{-1} \begin{pmatrix} b_{D1}^{fwd} \\ b_{D1}^{rev} \\ b_{D2}^{fwd} \\ b_{D2}^{rev} \end{pmatrix} \quad (2.31)$$

¹ Taking the square root in standard mathematical software one might code $\text{sqrt}(x)$. This, however, is incorrect as it introduces a discontinuity for complex numbers at ± 90 degrees. The correct method is to first unwrap the phase of the complex number then consider the number in polar form: $\sqrt{x} = \sqrt{|x|}e^{j\theta_x} = \sqrt{|x|}e^{j\theta_x/2}$. This peculiarity applies to all uses of the square root for calibration.

2.2.2 LF PORT 1 CALIBRATION

To this point a relative calibration is performed to de-embed relative network parameters to the DUT reference plane on the probe station at LF. The missing parameter is the absolute calibration scaling parameter K from (2.3). Since there is no instrument (at the time of writing) that can connect to the probe tips or on wafer to measure calibrated power and phase, a secondary coaxial calibration is needed at LF port 1 reference plane. Initially, a SOL calibration is performed (and could be equally performed at the other coaxial RF port):

$$\begin{pmatrix} a_{p1} \\ b_{p1} \end{pmatrix} = L \begin{bmatrix} 1 & \lambda \\ \mu & \nu \end{bmatrix} \begin{pmatrix} a_{R1} \\ b_{R1} \end{pmatrix}. \quad (2.32)$$

Here, the scaling constant, L , represents the absolute calibration parameters of magnitude and phase that will be found in the following sections. Of critical importance are the wave directions defined in (2.32) are *reversed* as compared to (2.3). The error parameters are found in the same manner as (2.6) by assembling a matrix with measurements of the different calibration standards. The adjusted matrix accounting for the backward wave directions is:

$$\begin{bmatrix} -b_{R1,S} & a_{R1,S}\Gamma_S & b_{R1,S}\Gamma_S \\ -b_{R1,O} & a_{R1,O}\Gamma_O & b_{R1,O}\Gamma_O \\ -b_{R1,L} & a_{R1,L}\Gamma_L & b_{R1,L}\Gamma_L \end{bmatrix} \begin{pmatrix} \lambda \\ \mu \\ \nu \end{pmatrix} = \begin{pmatrix} a_{R1,S} \\ a_{R1,O} \\ a_{R1,L} \end{pmatrix}. \quad (2.33)$$

2.2.3 ABSOLUTE MAGNITUDE CALIBRATION

Absolute magnitude calibration is performed by connecting a power sensor directly to the RF port 1 as shown in Fig. 2.7. The calibrated power meter measures the absolute power at the reference plane regardless of the reflection coefficient mismatch: the power measured is the incident power $P_i = |a|^2$. In the setup, the measured power directly gives $|a_S|$. The reflection coefficient of the power meter can be found using the T-parameters solved for in (2.32), which allows the computation of the magnitude of the scaling parameter, $|L|$. Note, that the phase of L is still unknown.

From the second row of (2.32) and $b_S = b_{p1}$,

$$b_S = L(\mu a_{R1} + \nu b_{R1}). \quad (2.34)$$

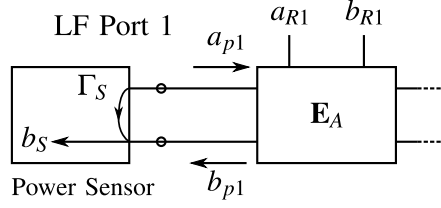


Figure 2.7: Model for power sensor. RF port 2 is excited with a CW source and a *thru* standard is on the probe station. The power is measured with a calibrated power sensor.

But only the magnitude is measured so:

$$|L| = \frac{|b_S|}{|\mu a_{R1} + \nu b_{R2}|} \quad (2.35)$$

Although, not needed for calibration, the reflection coefficient of the power meter can be found from (2.32)

as well:

$$\Gamma_S = \frac{a_{p1}}{b_{p1}} = \frac{a_{R1} + \lambda b_{R1}}{\mu a_{R1} + \nu b_{R1}}. \quad (2.36)$$

2.2.4 ABSOLUTE PHASE CALIBRATION

To calibrate the phase on a measured waveform, the relative phase between the frequency grid components must be known. This is done by measuring a known waveform with well defined phases. A known waveform can be generated by a pulse through a nonlinear device generating harmonics [61] (step-recovery-diode) or a nonlinear transmission line [68]. Or the waveform can be generated as a multisine by an arbitrary waveform generator (ARB). For this work, an ARB is used as the waveform generator. The model for the phase reference generator is shown in Fig. 2.8.

Only a_G is needed for a phase calibration. Details on determining this parameter is given in the next section (subsection 2.2.5). The equation for the measurement shown in Fig. 2.8 is

$$a_{p1} = a_G + \Gamma_G b_{p1}. \quad (2.37)$$

From (2.32),

$$L(a_{R1} + \lambda b_{R1}) = a_G + \Gamma_G L(\mu a_{R1} + \nu b_{R1}), \quad (2.38)$$

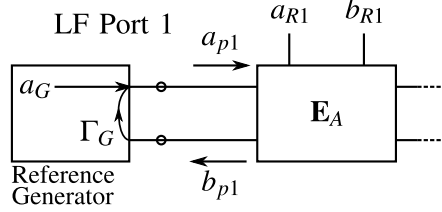


Figure 2.8: Model for reference generator. The reference generator is an ARB and is attached to RF port 1 (see Fig. 2.6). RF port 2 is terminated in a matched load and a *thru* standard is on the probe station.

which can be solved for the phase of L :

$$\angle L = \angle \left(\frac{a_G}{(1 - \Gamma_G \mu) a_{R1} + (\lambda - \Gamma_G \nu) b_{R1}} \right). \quad (2.39)$$

Note that this equation is different from that presented in [61].² The characterization of a_G is performed in a $50\ \Omega$ system (measured with the oscilloscope) and therefore when placed in the system, Γ_G is defined to be 0. The phase of L becomes

$$\angle L = \angle \left(\frac{a_G}{a_{R1} + \lambda b_{R1}} \right). \quad (2.40)$$

2.2.4A WAVEFORM GENERATION

A multisine waveform with a small tone spacing covering the entire calibration frequency range is used as the waveform for phase calibration. However a multisine waveform could have a PAR well in excess of 10 dB. To meet the maximum dynamic range limitations of the oscilloscope, the relative phases of the tones are modified so that the PAR ratio is < 3 dB. The Schroeder method is used here [69], with the smallest used frequency spacing of 10 kHz, requiring a minimum of 100 μ s oscilloscope acquisition. Larger frequency steps allow smaller acquisition times and faster measurements.

2.2.5 ARBITRARY WAVEFORM GENERATOR CHARACTERIZATION

The arbitrary waveform generator (ARB) is characterized in order to determine a_G and Γ_G in Fig. 2.8. No generator is perfect, so by measuring the reference generator parameters over frequency, any distortion of the

² Equation (5.5-33) in Verspect [61] is inconsistent with the previous equation (5.5-32) and the correct phase calibration equation is presented here. The inconsistency come from the direction of received and generated waves: $|L|$ is found by the *reception* of the wave from the error network, $\angle L$ is found by the *generation* of the wave into the error network.

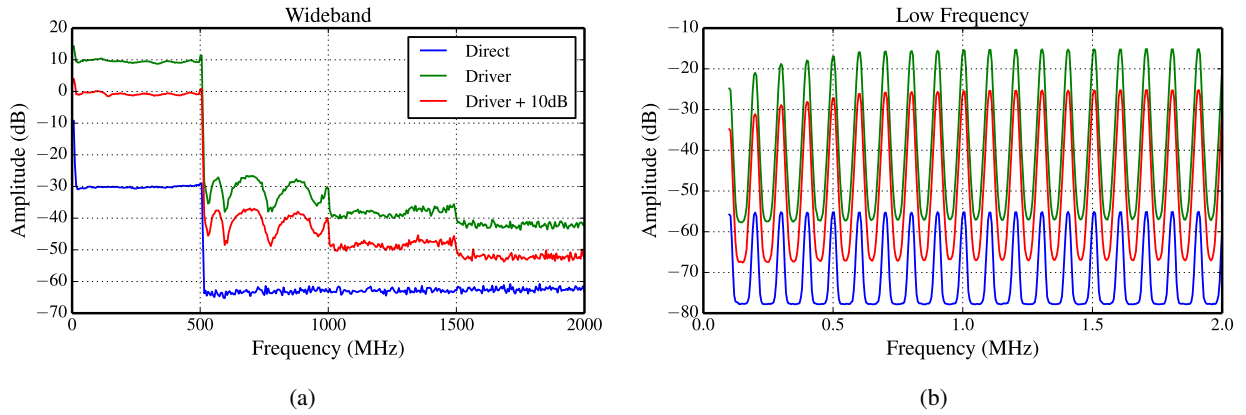


Figure 2.9: (a) Wide bandwidth and (b) narrowband spectrum of the 500 MHz bandwidth multisine. The measured power in (b) is much lower because the IF bandwidth on the spectrum analyzer is much smaller than in (a).

waveform from the generator or from optional drivers is known. As long as the distortion is time-invariant, the characterization can be used for calibration.

The reflection coefficient Γ_G would commonly be found by measuring the ARB with a standard vector network analyzer. However, in this case, the desired frequency range of 10 kHz-500 MHz is too low for a typical VNA (e.g. the Agilent E8463C minimum frequency is 10 MHz). Therefore, the LF measurement system was initially calibrated coaxially (without the probe station) and used to measure the ARB reflection coefficient. (The coaxial calibration was also performed for validation of the calibration method and is detailed in Appendix A.)

The second parameter, a_G , is found by directly measuring the waveform with an oscilloscope. The oscilloscope in the measurement is used by connecting a single channel directly to the ARB. As shown in (2.39), only the phase of a_G is needed: the magnitude calibration is performed in subsection 2.2.3. For the setup here, a 40 dB gain LF driver is used to amplify the ARB output. Fig. 2.9 shows the spectrum of the ARB and driver with a 500 MHz bandwidth multisine waveform with 100 kHz tone spacing. Fig. 2.9a demonstrates that the driver adequately amplifies the entire 500 MHz bandwidth. The low frequency end shows >30 dB of amplification down to 100 kHz even though the low end of the driver is 1 MHz. A 10 dB attenuator was added to the output of the driver to create a better match (lower Γ_G).

The direct measurement of the ARB output phase (with 10 dB attenuation and LF driver) is shown in

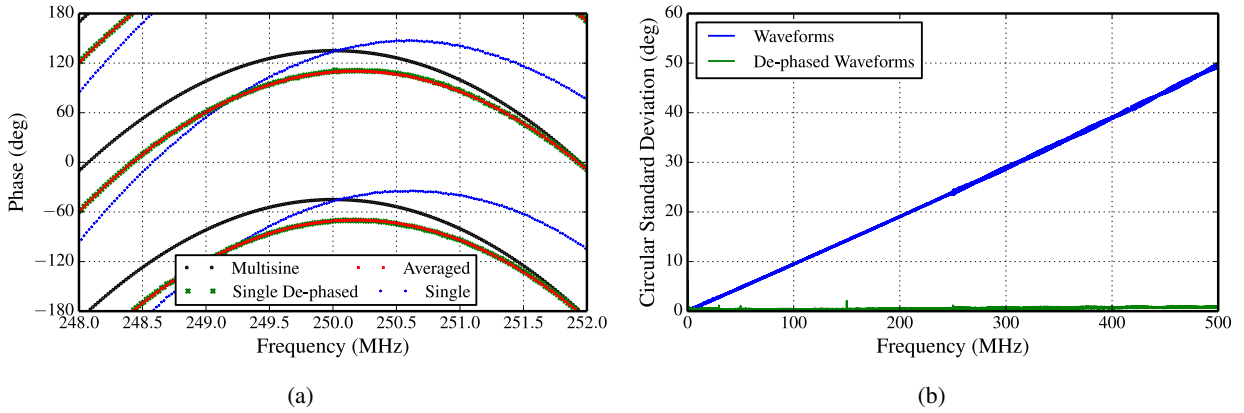


Figure 2.10: (a) Phase of the multisine waveform comparing steps for measuring the angle of a_G . (b) After de-phasing each measurement, the circular standard deviation is very low compared to the raw data.

Fig. 2.10a. The generated multisine phase from Schroeder is in black and a single measurement is shown in blue.³ While in this frequency range, the phase looks fairly close to the generated waveform, it is preferred to eliminate any linear phase shift caused by inaccurate triggering [70]. For each measured waveform, the linear phase shift (pure time delay) is optimized to give a minimum as compared to the generated multisine. For Fig. 2.10a, a single de-phased waveform is green and the average of 40 de-phased measurements of the ARB is in red. The circular standard deviation is another method to evaluate the de-phasing of the signal (Fig. 2.10b). Without the linear phase correction the circular standard deviation is very large for the high frequency range. However, after de-phasing, the standard deviation is low: under 1.5 degrees for almost the entire frequency range. The average value is a_G for use in (2.39).

The circular standard deviation is defined as:

$$S = \sqrt{-2 \ln |\bar{R}|}, \quad (2.41)$$

³ The observant reader would object to the comparison of the generated ARB waveform phase and the measured as the ARB is a *voltage* generator, not a pseudo wave generator. However, the ARB has a 50Ω output impedance and with pseudo waves having a real reference impedance, the current has phase equal to the voltage: $\angle(V) = \angle(ZI) = \angle(I)$. This makes the pseudo wave phase equal to the voltage phase. In any case, Fig. 2.10a is for illustrative purposes, and any imperfections in the source impedance are calibrated out by ARB characterization and by measuring the ARB reflection coefficient, Γ_G .

where \bar{R} is

$$\bar{R} = \frac{1}{N} \sum_{n=1}^N z_n \quad (2.42)$$

$$z_n = e^{j\theta_n} \quad (2.43)$$

and z_n is a unit vector with angle equal to the phase of the n -th frequency component. To explain (2.41) in an intuitive manner; the average of z_n (all unit vectors) will have some distance from 0 amplitude, where a value of 0 is evenly distributed around the circle, and a maximum value of 1, all z_n are at the same angle. \bar{R} is then a distance from 0 to 1 describing the distribution of a vector of angles. The minimum value for S is 0 ($\bar{R} = 1$) while the maximum is ∞ ($\bar{R} = 0$).

After de-phasing and averaging the waveform directly from the ARB, the ARB is connected (in this case with a LF driver amplifier) to the LF port 1 as shown in Fig. 2.8. The measured variable a_{R1} is used for de-phasing the coupled waves and the resulting phases over multiple measurements are averaged giving a_{R1} and b_{R1} to be used in (2.39). The angle of the scaling factor, $\angle K$, can now be computed.

2.2.6 FINDING SCALING PARAMETER K

Up to this point, two separate calibrations have been performed. Ultimately, the goal is to find all the unknowns of (2.3) to relate the measured waves to the DUT reference plane waves. This section unites the LF port calibration to find the unknown K scaling parameter in (2.3).

The previous calibrations allow one to relate the measured waves to the DUT (in a relative sense), (2.3), and to the LF port, (2.32). The equations are repeated here for convenience:

$$\begin{pmatrix} a_{D1} \\ b_{D1} \end{pmatrix} = K \begin{bmatrix} 1 & \beta_1 \\ \gamma_1 & \delta_1 \end{bmatrix} \begin{pmatrix} a_{R1} \\ b_{R1} \end{pmatrix}, \quad \begin{pmatrix} a_{p1} \\ b_{p1} \end{pmatrix} = L \begin{bmatrix} 1 & \lambda \\ \mu & \nu \end{bmatrix} \begin{pmatrix} a_{R1} \\ b_{R1} \end{pmatrix}. \quad (2.44)$$

The relationship between the RF port and the DUT reference plane can be stated in terms of T-parameters as

$$\begin{pmatrix} a_{p1} \\ b_{p1} \end{pmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{pmatrix} a_{D1} \\ b_{D1} \end{pmatrix}. \quad (2.45)$$

Since this equation relates pseudo-waves to pseudo-waves, the T-parameter matrix, \mathbf{T} is reciprocal for passive components (in this case the coupler and RF probe station tuner). The determinant of the \mathbf{T} is 1. Using

(2.44) to find the T-parameters gives,

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = L \begin{bmatrix} 1 & \lambda \\ \mu & \nu \end{bmatrix} \left(K \begin{bmatrix} 1 & \beta_1 \\ \gamma_1 & \delta_1 \end{bmatrix} \right)^{-1}. \quad (2.46)$$

Solving for K through the determinant,

$$\det[\mathbf{T}] = 1 \quad (2.47)$$

$$K = \pm\sqrt{Q} = \pm\sqrt{\frac{L^2(\lambda\mu - \nu)}{(\beta_1\gamma_1 - \delta_1)}}. \quad (2.48)$$

The scaling parameter is de-phased, subtracting a linear phase to align the frequency component phases. This leaves a plus/minus sign ambiguity which can be determined by minimizing the phase with respect to the coupler measurement port to DUT reference plane port. One must take care when taking the square root as the phase must be unwrapped first.

2.2.7 CALIBRATION SUMMARY

In summary, the steps for calibration of a 2-port probe station LF path are:

(1) Relative calibration to the probe tips:

- Measure SOL standard on port 1,
- Measure SOL standard on port 2,
- Measure *thru* standard.

(2) Absolute calibration on an RF port:

- Measure SOL standard on LF port,
- Measure absolute power on LF port,
- Attach ARB to LF port and measure multitone signal.

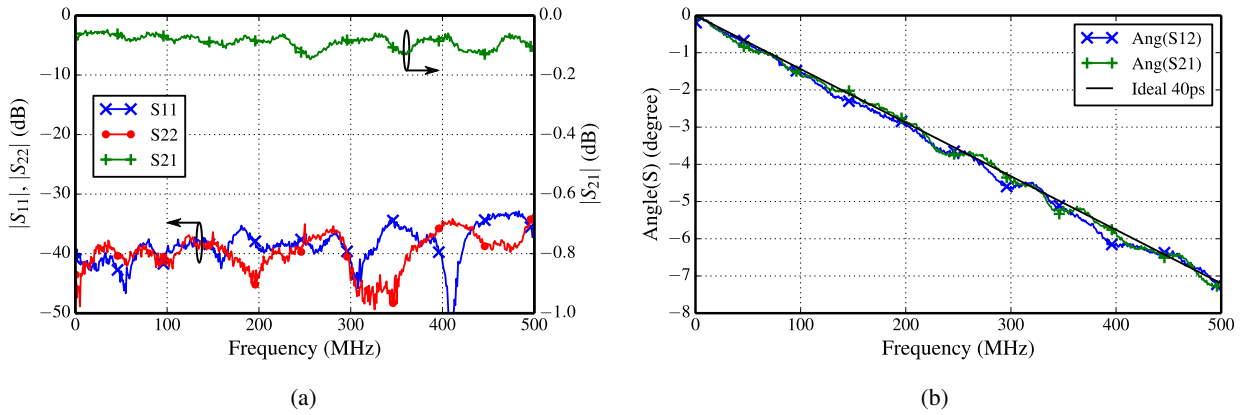


Figure 2.11: Calibration test using a 40 ps line standard. (a) Input match and loss through the line are very low as expected for a small section (5.25 mm) of CPW line. (b) Phase delay through the line compared to the ideal phase delay shows agreement within ± 0.4 degrees.

2.3 LF CALIBRATION VERIFICATION

As mentioned earlier in the chapter, there are no known instruments that can measure calibrated power or phase directly on-wafer: verification of an absolute calibration to the probe tips requires instruments that currently do not exist. Relative calibration, however, can be easily verified by measuring standards on the ISS and/or comparing to another instrument that can be calibrated in a relative manner (e.g. a commercial VNA).

2.3.0A RELATIVE CALIBRATION TESTS - 40 PS LINE

The 40 ps line on the impedance standard substrate (ISS) was used as a test network to confirm the relative calibration routine. The goal is to compare the phase delay through the line to the actual delay of 40 ps. The ideal phase of the line can be found in degrees by

$$\text{Ideal Phase} = -ft_d 360^\circ \quad (2.49)$$

where f is the frequency and t_d is the time delay, in this case 40 ps. The calibrated results are shown in Fig. 2.11. The agreement between the ideal phase delay and the measured is very close, within ± 0.4 degrees for the entire frequency range.

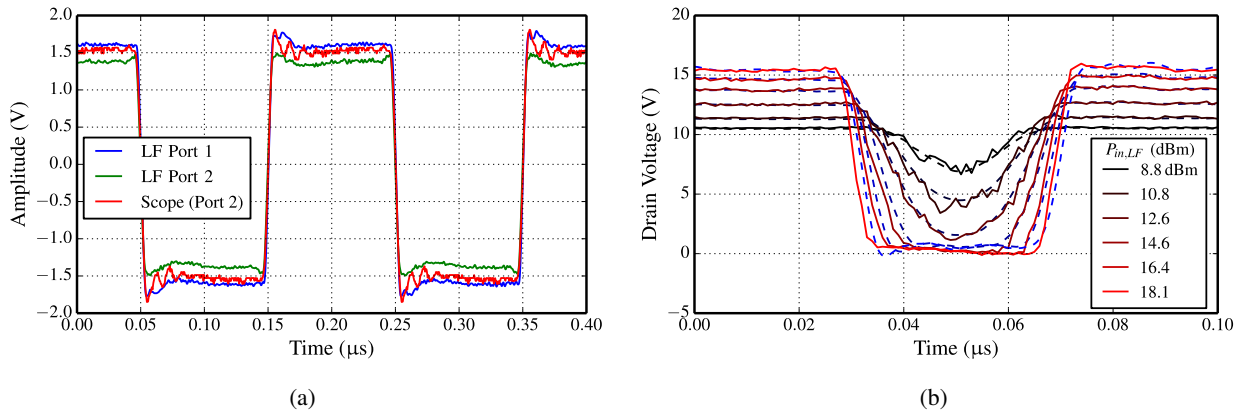


Figure 2.12: (a) 5 MHz square wave measured by LFBNA and oscilloscope. The measurement planes are *not* the same because a oscilloscope probe could not be placed on the probed *thru* line. The agreement is close although the scope shows more ringing on the front end of the square wave edges. (b) De-embedded measurements of a $10 \times 90 \mu\text{m}$ GaN FET at $V_g = -4.0 \text{ V}$ (pinched off) with the LFBNA (solid red lines) compared to an oscilloscope (dotted blue lines).

2.3.0B ABSOLUTE CALIBRATION TESTS - COMPARISON TO OSCILLOSCOPE

An oscilloscope measurement can be used to confirm the calibration procedure and was used to compare the de-embedded results of a square wave through a 40 ps line and an output waveform of a FET transistor. Since the oscilloscope probe cannot be placed on the substrate standard, the diplexer is probed on the microstrip line of the diplexer on port 2. This is the closest point to the measurement plane (for port 2). Low frequencies ($< 10 \text{ MHz}$) were used to minimize the difference between the oscilloscope and the actual measurement plane. Aside from a linear phase shift, the waveforms should be very close.

A square wave was applied to LF port 1 and the calibrated results for LF port 1 and LF port 2 shown in Fig. 2.12a. The agreement between the oscilloscope and measurement system is good with a slight overshoot at the beginning of the edges of the square wave.

The second test was with a $10 \times 90 \mu\text{m}$ FET transistor in a pinched-off state excited at 10 MHz. For large input powers the device behaves like a switch. The calibrated waveforms of an input power sweep and comparison to the oscilloscope measurement is shown in Fig. 2.12b. The overall agreement is within a few nanoseconds and $< 1 \text{ V}$ for a majority of the waveform.

The 40 ps line could be used again and de-embedded with a single 1-port excitation using (2.3) (instead

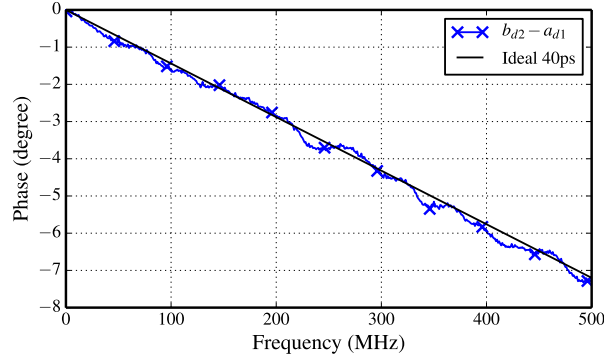


Figure 2.13: De-embedded measurement of the 40 ps line standard using a single port excitation and (2.3). The agreement is within ± 0.4 degrees.

of the necessary excitation on 2-ports for S-parameters using (2.31)) to give the relative phase between a_{D1} and b_{D2} (pseudo-wave entering the DUT at port 1 and then leaving the DUT at port 2). The phase difference should be similar to that shown in Fig. 2.11b. The results of the absolute de-embedding is shown in Fig. 2.13 which shows similar agreement to the relative de-embedding case.

2.3.1 PROBE STATION TUNER EFFECT ON LF CALIBRATION

One component that has been ignored so far is the effect of the RF probe station tuners on the LF 2-port calibration. These, so far, have been assumed to be a static, passive network. The model numbers of the tuners are Focus iTuner 5080 and 5080-2H for the source and load respectively. These are 8-50 GHz fundamental tuners while the “2H” has a second harmonic stub. Below the minimum tuner frequency of 8 GHz, any tuning performed has less and less of an effect on tuning the reflection coefficient, ultimately converging on a $50\ \Omega$ line. Reference [71] gives details on the physical operation of tuners. Fig. 2.14a shows the difference between the T-parameter computation (2.45) for two tuner positions: $50\ \Omega$ and at max gain ($\Gamma_{src} = 0.79\angle 152$ which is the maximum reflection coefficient that could be achieved at 10.7 GHz). The change in magnitude is under 0.2 dB for the entire frequency range (which could be equally attributed to repeatability error) and the phase difference is under 4 degrees. The error for the load tuner will be similar with a high Γ_{load} .

A worst case approximation for the deviation of the measurements was tested by measuring a short

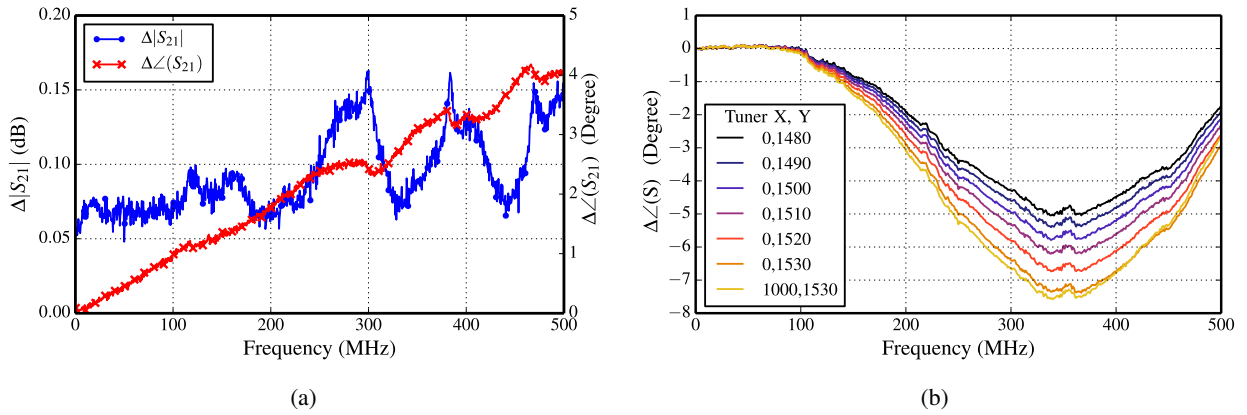


Figure 2.14: (a) Magnitude and (b) phase of the measured short standard (ISS). The magnitude has very little variation from the nominal $X=0$ and $Y=0$ while the phase is affected at most by 7.5 degrees around 400 MHz.

circuit. Fig. 2.14 shows the de-embedded phase compared to the nominal tuner position of $X=0$ and $Y=0$ (the location of the original LF calibration). The position corresponds to a movement of $3.18 \mu\text{m}$ per X and $1.5 \mu\text{m}$ per Y . At most there is approximately 7.5 degrees of error in the upper frequency range. Changing the X position has a small effect on the overall network as compared to moving the Y position of the slug because the wavelengths are large compared to the position of the slug (less than 0.2 degrees of variation for $Y=1530=2.3 \text{ mm}$). This gives the largest phase error that might be present in the LF measured parameters when modifying the RF load. In an ideal world, the tuners would be swept through all possible positions and the network measured at LF and RF. However, the amount of time required by this is large and prohibitive. Instead, after characterization of the FET with sourcepull (with 50Ω load) and then loadpull, the tuners were set to maximum gain (for source load) and maximum PAE (for the RF load). LF calibration was performed at these tuner positions to eliminate any measurement bias.

2.4 RF CALIBRATION

2.4.1 TUNER CALIBRATION

Calibration in the RF path for the probe station setup may seem complicated because of the two modifiable unknown networks (the tuners) before the desired reference plane. However, the measurement of the tuners

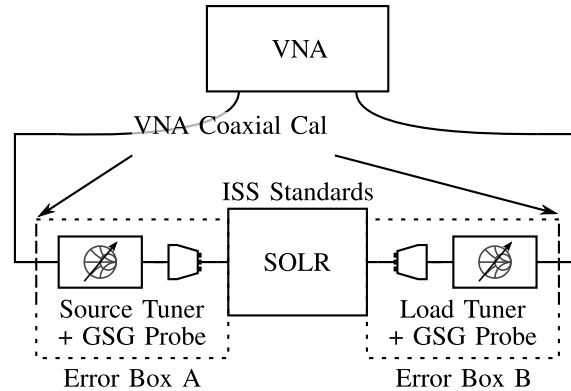


Figure 2.15: RF Tuner calibration setup. The VNA is calibrated coaxially to the end of the cables connecting to the tuners. The tuners network parameters are determined by initially performing a SOLT/SOLR calibration with the tuners at $X, Y=0, 0$.

are fairly straight forward with calibration to incremental reference planes (Fig. 2.15). Initially, the VNA is calibrated coaxially to the end of the cables that would hook up to the tuners. Subsequent measurements now only have the effect of the tuners and probe station (error boxes A,B in Fig. 2.15). To calibrate each tuner separately, an initial SOLT (or SOLR) calibration is performed to find each “error box” when the tuners are in the $50\ \Omega$ position. This allows de-embedding of a single probe station tuner when the other tuner is swept through the X, Y constellation. Each tuner is swept separately de-embedding the opposite side giving a complete tuner characterization from the coaxial port to the probe tip (the probe tip is *included* in the error box).

2.4.2 RF PATH POWER OFFSETS

The RF power offsets for the power meters are determined by measuring the S-parameters of the RF networks external to the tuners. The S-parameters of the 3-port networks (RF input, RF output, and RF coupled port) are cascaded with the tuner calibration file which contains S-parameters for all tuner positions. The cascaded network is then used to find the difference in power to the coupled port to the power input of the device (on the input network) and the power difference between the output of the device and the coupler (on the output network). Simplifications and certain requirements for the networks are detailed in [71]. Repeated here for completeness, the power offset for the input network for available input power to the DUT as measured by a

power meter on the coupled port is

$$\Theta_{in} = \frac{|S_{21}|^2}{|S_{31}|^2(1 - |S_{22}|^2)}, \quad (2.50)$$

where port 1 is the RF source, port 2 is the DUT, and port 3 is the coupled port. The output network power offset from the coupled port to the DUT is

$$\Theta_{out} = \frac{1 - |S_{11}|^2}{|S_{21}|^2}, \quad (2.51)$$

where port 1 is the DUT and port 2 is the coupled port.

2.5 CONCLUSION

A system for measurement of RF and LF performance of a device is constructed and calibrated. The calibration and components are kept separate between the LF and RF paths except for the mutual components. The diplexer needs special attention to be able to have adequate performance at LF and RF. Calibration for the LF path was covered in detail with full mathematical expressions and reasoning including pitfalls that were encountered during calibration. Finally, the RF path calibration was detailed.

CHAPTER 3

LOW FREQUENCY GAN FET MEASUREMENTS

CONTENTS

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With the multi-frequency measurement bench detailed in the previous chapter, the performance of GaN FET transistors at low frequency (1-500 MHz) and while under supply modulation can be investigated. In this chapter, a number of power regimes are considered of increasing complexity and relevance to supply modulation:

- (1) small-signal characterization with no RF/LF excitation;
- (2) small-signal characterization with RF excitation;
- (3) large-signal characterization with RF and LF.

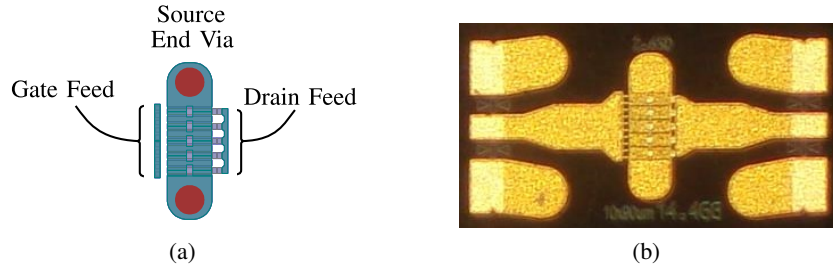


Figure 3.1: (a) Layout and (b) photograph of 10x90 μm device used for output stage of MMICs and for testing in most of this thesis.

To understand more integrated devices (e.g. power amplifiers) the primary nonlinear element, a FET transistor, is investigated first. This thesis focuses on FET transistors fabricated in the TriQuint 0.15 μm GaN process on 4 mil SiC. Two device sizes of 8x40 μm and 10x90 μm are characterized here, and are also used in the MMIC power amplifiers characterized in the following sections.

3.1 TRIQUINT GAN 0.15 μm PROCESS

The process used to the FET transistors and MMICs designed in this process were fabricated in a 0.15 μm gate length process with an AlGaIn/GaN epitaxial layer on 100 μm silicon carbide (SiC) on 100 mm diameter wafers. Typical dc characteristics of these transistors are $I_{max} = 1.15$ A/mm, conductance $g_{m,max} = 380$ mS/mm, and 3.5 V pinch-off at $V_{ds} = 10$ V. Device breakdown voltage exceeds 50 V at $I_{gd} = 1$ mA/mm. Nonlinear device models were extracted for 8x40 μm and 10x90 μm devices (number of gate fingers by gate width) at 10 GHz. To support supply modulation applications, the models were fit to S-parameter and loadpull data measured at low drain current over a wide range of drain bias voltages. Loadpull results for a PAE of 62% at 10 GHz and 20 V drain bias demonstrated 3.4 W/mm output power density with associated gain of 14 dB [72]. A photograph and layout of the 10x90 μm device is shown in Fig. 3.1. During the time frame of this thesis, TriQuint merged with RFMD and became Qorvo. The GaN 0.15 μm process was unchanged through the merger which happened in the last year of this work.

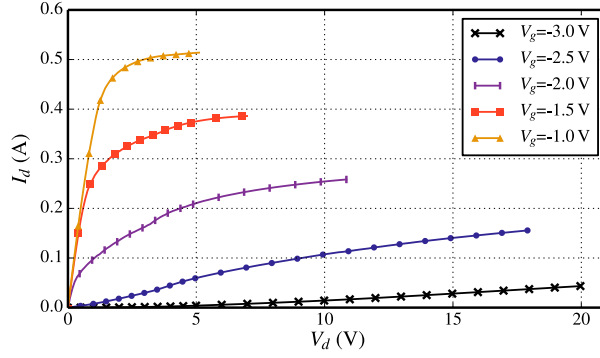


Figure 3.2: Measured I - V curves for $10 \times 90 \mu\text{m}$ device. At each point, the low frequency impedance is measured. The device is kept under 3.0 W power dissipation to avoid damage.

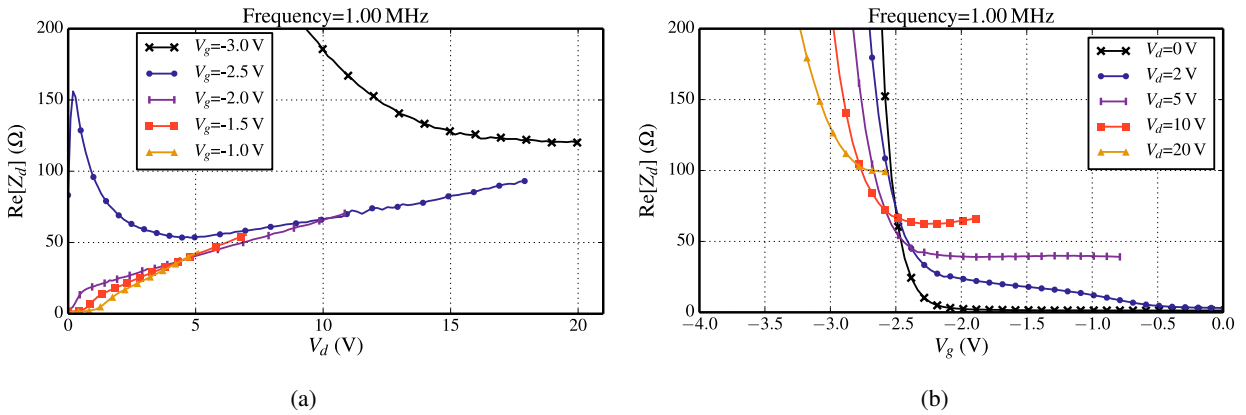


Figure 3.3: (a) Measured real part of the drain impedance at 1 MHz with no RF input. While the partial derivative of the I - V curves gives a rough approximation in trends of the drain impedance, there is a significant magnitude difference above approximately $V_d = 5 \text{ V}$. (b) The real part of the measured drain impedance plotted versus gate bias clearly shows the turn-on voltage for the device at various supply drain voltages.

3.2 STATIC DRAIN IMPEDANCE - $10 \times 90 \mu\text{m}$

The measured I - V curves of a $10 \times 90 \mu\text{m}$ device are shown in Fig. 3.2. At each bias point, the small-signal drain impedance is measured. The device is kept under 3.0 W power dissipation to avoid failure as the bench is not capable of pulsed measurements. The measured low frequency impedance at 1 MHz is shown in Fig. 3.3a. The measured impedance is not the same as the small-signal bias point resistance ($\partial V_d / \partial I_d$) because of frequency dispersive effects [33, 73, 74]. Since the measurement frequency is above the typical transition frequency for dispersion (e.g. 100 kHz in [33]), the measured impedance is closer to the S-parameters at the

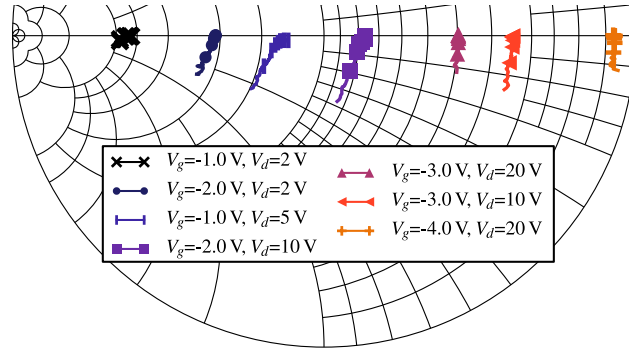


Figure 3.4: Complex impedance from 10 MHz to 500 MHz of a few bias points of the 10x90 μm transistor plotted on a 50 Ω admittance grid. The lower gate bias voltage curves can easily be fit by a parallel RC circuit. The higher gate biases (-1 and -2 V) have an inductive part in addition to the RC indicating other effects under high current.

particular bias point, compared to the dc resistance. The behavior shown in Fig. 3.3a is analogous to that of a bias dependent switch; at low V_g the device is off and presents a high impedance while, when the channel is open (high V_g) the impedance drops to the resistance of the channel itself. The current saturation of the device can be seen as the increase of resistance for higher V_d (the $V_g = -3$ V case is not saturated and so the impedance still decreases for larger V_d). Plotting the impedance versus gate voltage in Fig. 3.3b, the turn-on voltage can be clearly seen at various V_d as a large decrease in drain resistance.

The frequency variation of the static bias point can easily be fit by a parallel RC circuit. However, the higher current bias points have a distinct series inductive part that indicates other effects besides a bias dependent resistance and capacitance. This can be seen in Fig. 3.4 where the higher current bias points (-1 and -2 V) have a slant toward the left instead of following the constant admittance circles. Higher V_g is investigated further in the next section on a smaller device.

3.3 STATIC DRAIN IMPEDANCE - 8x40 μm

The I - V curves of a 8x40 μm device are shown in Fig. 3.5a. In a similar fashion to the 10x90 μm device, the impedance measured at each bias point is shown in Fig. 3.5b at 1 MHz. The trends are similar to those of the larger device. A 3D contour of the real and imaginary parts of the drain impedance are shown in Fig. 3.5c and 3.5d. The pinch off voltage can clearly be seen in the $\text{Re}[Z_d]$ as the sharp increase in impedance around

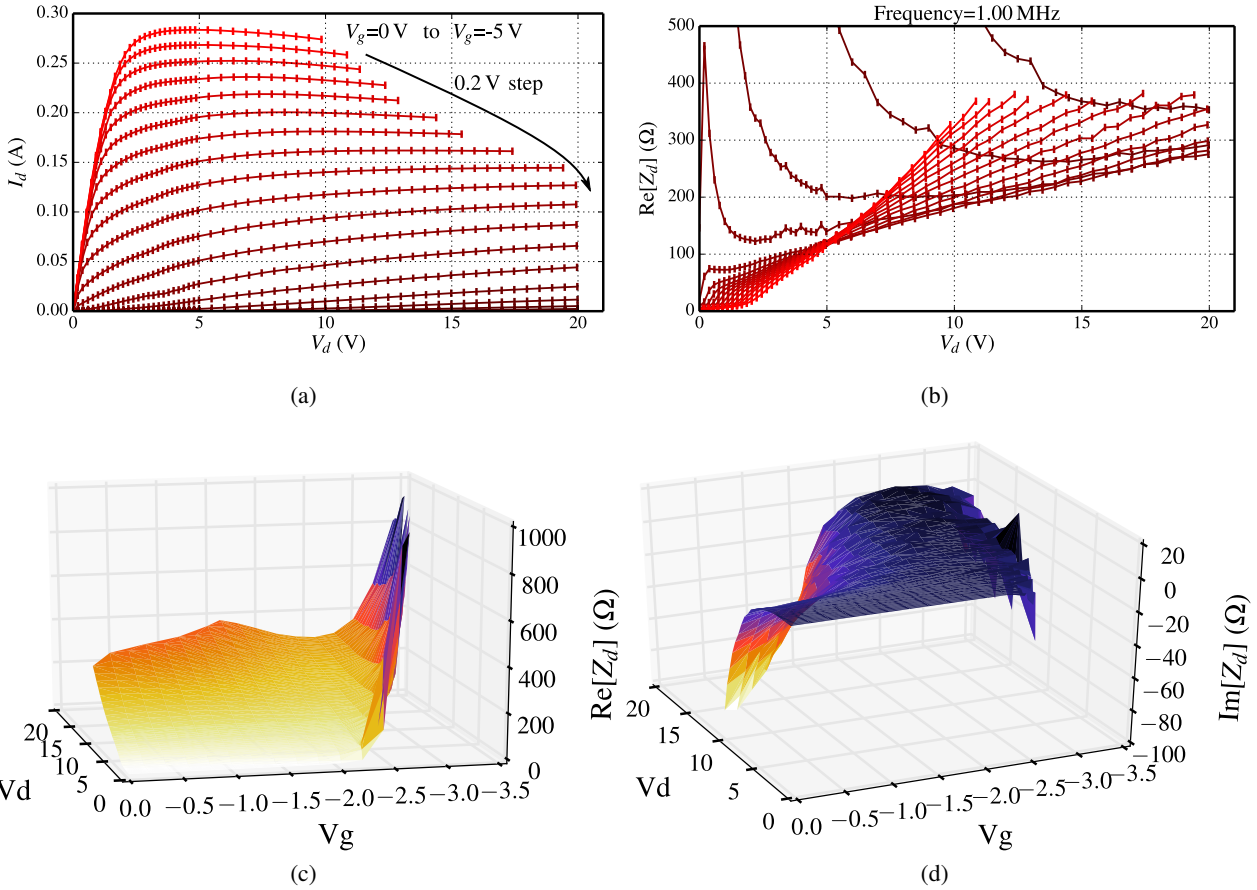


Figure 3.5: (a) Measured I - V curves for $8 \times 40 \mu\text{m}$ device. (b) At each point, the low frequency impedance is measured. The device is kept under 3.0 W power dissipation to avoid damage. (c) 3-D view of (b), the real part of the drain impedance. (d) Imaginary part of the drain impedance.

$V_g = -2.5 \text{ V}$ to -3.0 V depending on V_d . An increase in capacitance for higher currents (high V_g) and drain voltages above $V_d = 5 \text{ V}$ is clearly seen in the sharp decrease in $\text{Im}[Z_d]$. As a function of frequency, $\text{Re}[Z_d]$ is fairly constant across 1 - 500 MHz , depending primarily on the bias voltages (Fig. 3.6a). Although near pinch-off, the impedance can vary 100 's of ohms as the drain voltage increases (Fig. 3.6c). However, the imaginary portion of the impedance at high bias ($V_g = -1 \text{ V}$) suggests a large frequency dispersion effect that is not seen in the larger device. Since the device is smaller, total currents are lower so a wider range of bias voltage could be tested without worry of damaging the device due to over-heating or large currents. Although precise measurements could not be made below 500 kHz , the real and imaginary parts suggests that there is a back-gate effect on the device because of the increase in real and negative reactive impedance

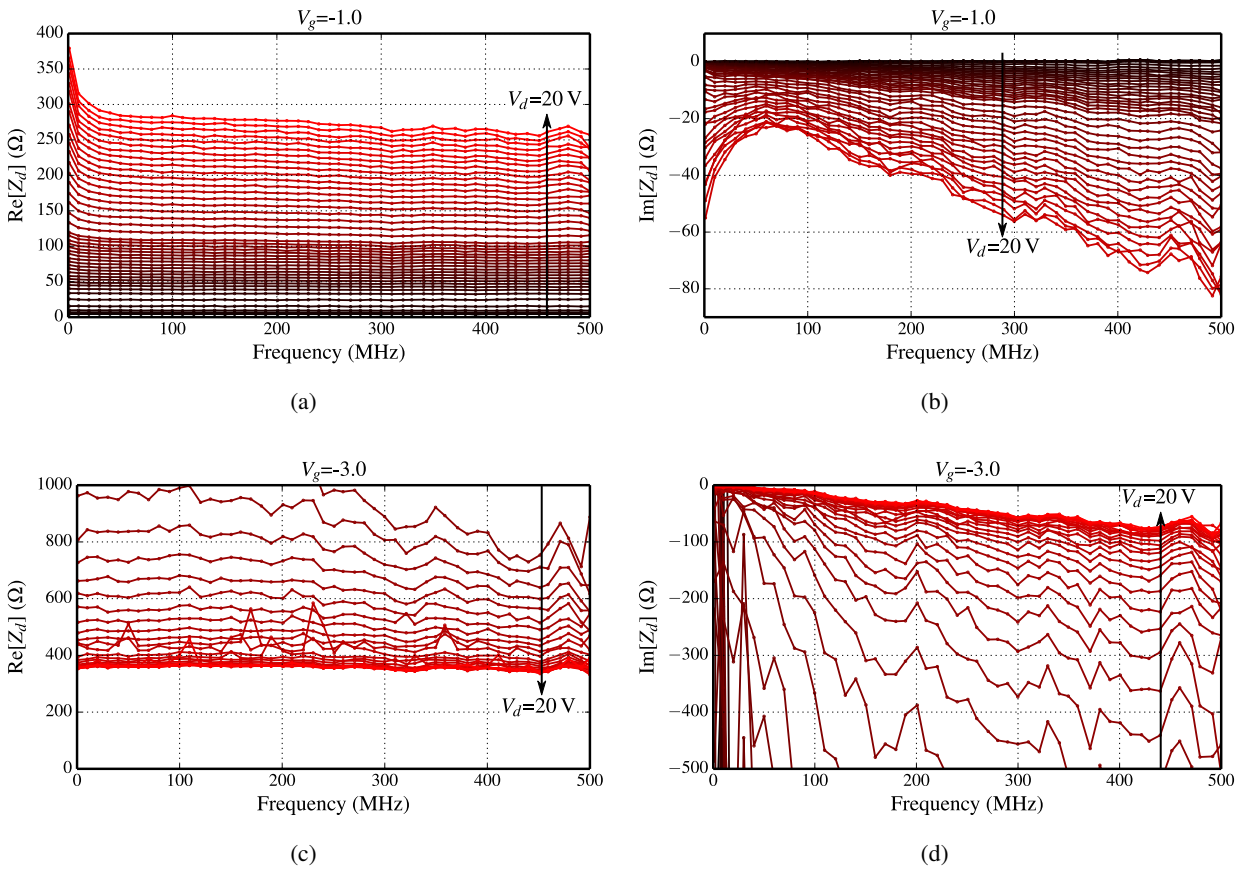


Figure 3.6: (a) Measured real part of the drain impedance for the 8x40 um GaN FET at 1 MHz with no RF input. While the partial derivative of the I - V curves gives a rough approximation in trends of the drain impedance, there is a significant magnitude difference above approximately $V_d = 5$ V. (b) The real part of the measured drain impedance plotted versus gate bias clearly shows the turn-on voltage for the device at various drain supply voltages.

at frequencies <20 MHz. The back-gate effect is shown for an Angelov model in Appendix C. Also of note is the large effect that V_d has on the impedance regardless of the gate bias.

3.4 DYNAMIC IMPEDANCE - LARGE-SIGNAL RF

While the static measurements are enlightening for certain aspects of transistor modeling, the true application of the measurement setup is for simultaneous excitation of the device with low and high frequencies, simulating supply modulation operation. There are a large number of variables that affect the LF impedance, first of which is the RF load impedance. At first glance, it may seem that load impedances presented to

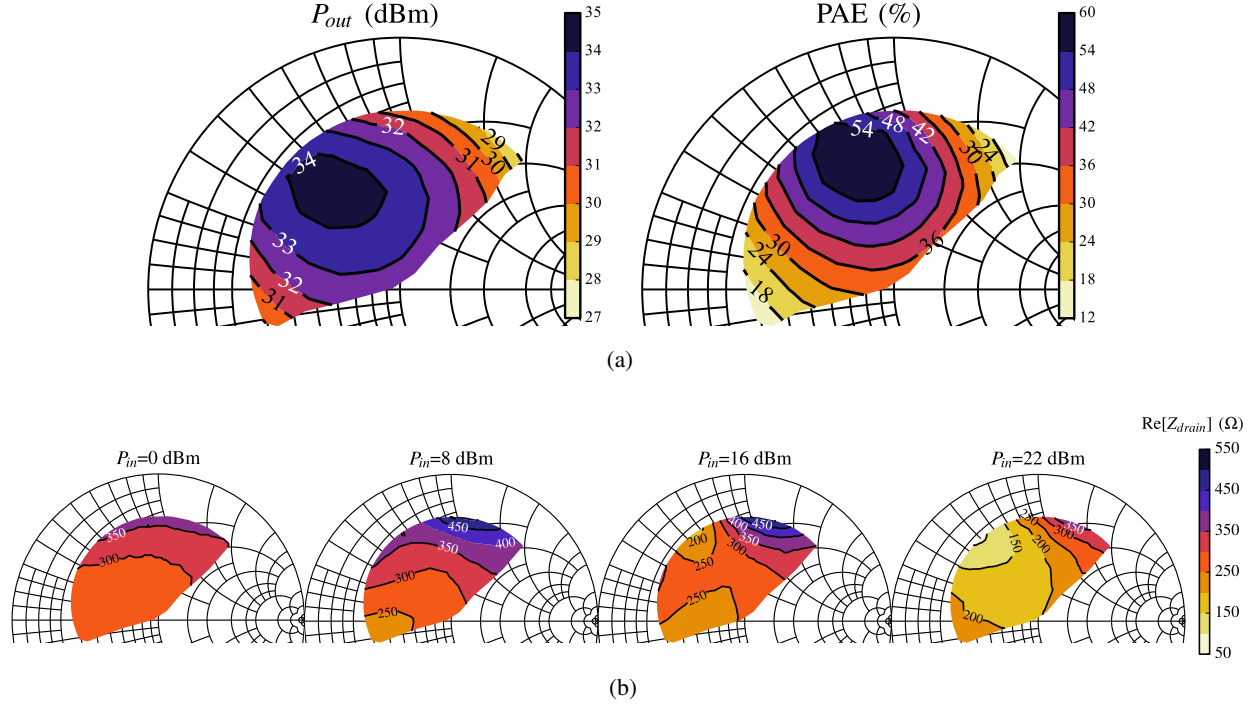


Figure 3.7: (a) Measured RF loadpull performance on $10 \times 90 \mu\text{m}$ transistor at 10 mA/mm , $V_d = 20 \text{ V}$, and RF $P_{in} = 22 \text{ dBm}$. (b) $Re[Z_d]$ at 10 MHz plotted versus RF impedance at various input powers.

the device at a particular frequency do not affect the performance or behavior at another distant frequency. However, under large-signal excitation, the RF loadline at one frequency compresses or clips the waveform which affects *any* other frequency signal passing through the device, whether it be a change in the dynamic bias point or additional RF modulation. A straightforward example of this effect is the small-signal impedance behavior during RF loadpull of the device.

Sourcepull and loadpull were performed on the $10 \times 90 \mu\text{m}$ device to find the optimum fundamental frequency RF terminations for maximum gain (source) and maximum PAE (load) at 10.7 GHz and $V_d = 20 \text{ V}$. The peak power added efficiency (PAE) occurs for an RF load of $25.0 + j34.2$. Measured output power and efficiency contours are shown in Fig. 3.7a. Over various RF input powers and at each loadpull point, the low frequency impedance is measured and shown in Fig. 3.7b. The value of the real impedance varies not only with the RF load, but with the RF input power as well, as it is expected. At low input power, Z_d is roughly constant around 300Ω with a variation toward higher impedance for higher gamma (possibly due to the impedance variation of the tuners at low frequency). As the RF input power increases, the drain impedance

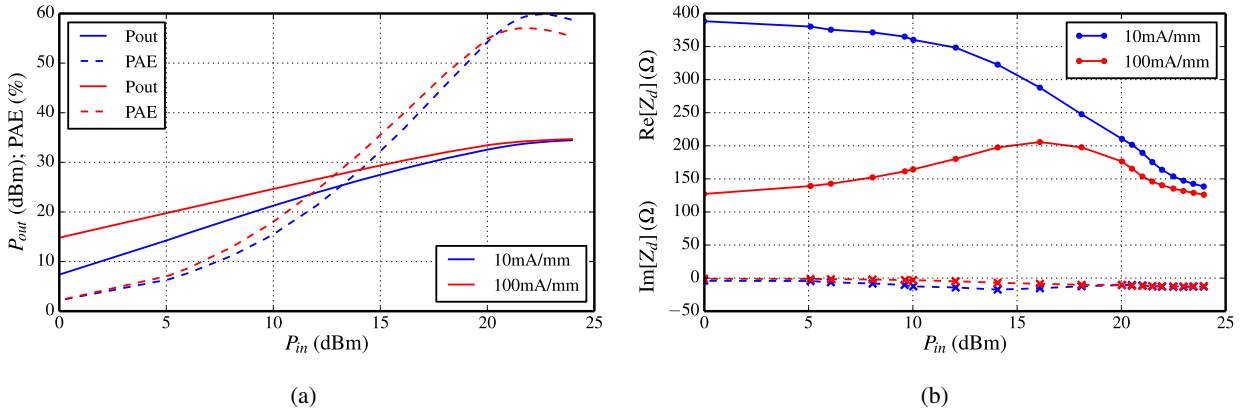


Figure 3.8: RF performance of the $10 \times 90 \mu\text{m}$ device. The RF load is set for maximum PAE. (b) Impedance of the drain versus RF input power on the gate. The class-A case (100 mA/mm) has a characteristic increase in the real part of the impedance before saturation.

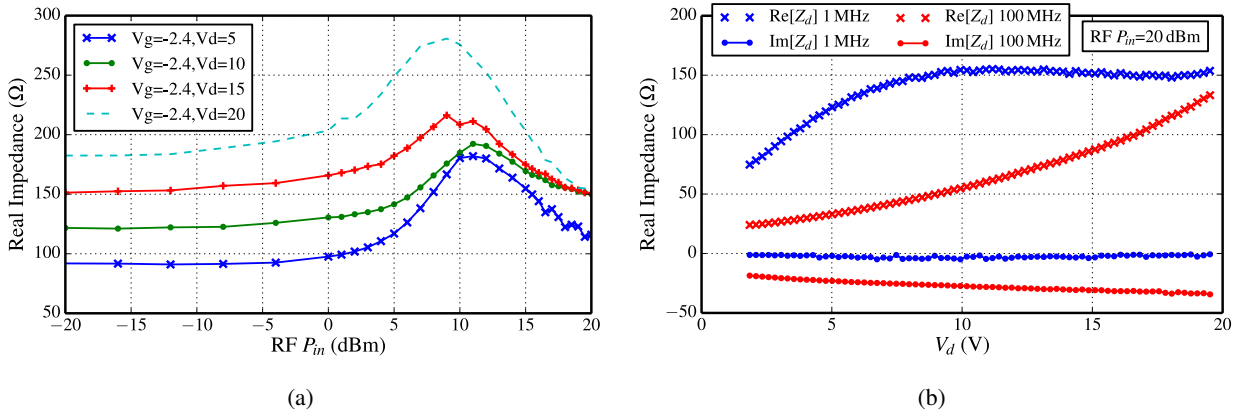


Figure 3.9: (a) Measured drain impedance at 1 MHz for the $10 \times 90 \mu\text{m}$ device versus RF input power (10.7 GHz) and drain bias voltage. (b) $Re[Z_d]$ versus drain voltage at 20 dBm input. Except for low drain voltages around the knee voltage of the device, the impedance under compression is approximately the same. The data in this plot is from a different FET device (and setup) from that used in Fig. 3.8b. $I_{dq} = 83 \text{ mA/mm}$ at $V_d = 20 \text{ V}$.

decreases to 150Ω for the RF load for peak PAE. Fig. 3.8 shows the impedance versus RF input at RF load for max PAE for two bias points; 100 mA/mm (class-A) and 10 mA/mm (class-B). As shown in the loadpull plots, even at small-signal, the LF impedance can change dramatically as a function of the RF input power to the gate of the device. The class-A case has considerably less impedance variation but has a characteristic increase *before* saturation of the device. This effect will be explored and explained in Chapter 5.

As seen with the static measurements in Section 3.2, the bias point has a large effect on the drain

impedance of a device. For the application of supply modulation, under large-signal RF drive, the drain voltage changes significantly to modify the bias point of the device in order to decrease the dissipated dc power. Fig. 3.9a shows the dependence of the drain impedance on the input power and the drain supply voltage for a high quiescent bias point of 83 mA/mm. Similar to Fig. 3.8b, there is a peaking of real impedance before compression (the device compression curve can be seen in Fig. 3.8a). In addition, increasing the drain voltage increases the real impedance, which agrees with static measurements in Fig. 3.3a. In the supply modulation case, the decrease of RF input power and drain voltage counter-act each other in terms of $\text{Re}[Z_d]$: with an RF input power of 10 dBm and $V_d = 5$ V, an impedance of 170Ω is measured versus the impedance at full bias and in compression of 150Ω . Interestingly, at V_d away from the knee voltage (for this process the knee voltage is approximately 5 V) under high compression ($P_{in} = 20$ dBm), the drain impedance is nearly the same for any V_d . This is seen in Fig. 3.9b as the flat impedance from approximately 10 V to 20 V. However, this is not necessarily true for all frequencies. Also shown is the impedance variation at 100 MHz which initially, starts at a much lower impedance and increases with drain voltage. The imaginary part of the drain impedance 1 MHz is not significant; it is nearly zero across drain voltage. However, as frequency increases, the parasitic capacitances of the device become more significant. At 100 MHz, the imaginary part decrease from $-j20 \Omega$ to approximately $-j40 \Omega$.

Figs. 3.10 and 3.11 show the very complicated behavior of a FET device over frequency and RF input power at $V_d = 5$ V and 20 V respectively. The impedance at small RF input powers (<0 dBm), is roughly constant and is similar to the results in the static case (Section 3.2); it can be modeled as a simple parallel RC. However, when approaching compression, the impedance can vary greatly in real and imaginary parts over RF input power and over frequency.

3.5 DYNAMIC IMPEDANCE - LARGE-SIGNAL LF/RF

Under supply modulation, the envelope can be considered as a frequency domain signal with some power distributed over a bandwidth. It is reasonable to expect that the impedance seen by the supply modulator will be dependent on the power that it supplies, P_{lf} . Figs. 3.12 and 3.13 show the variation in real and imaginary

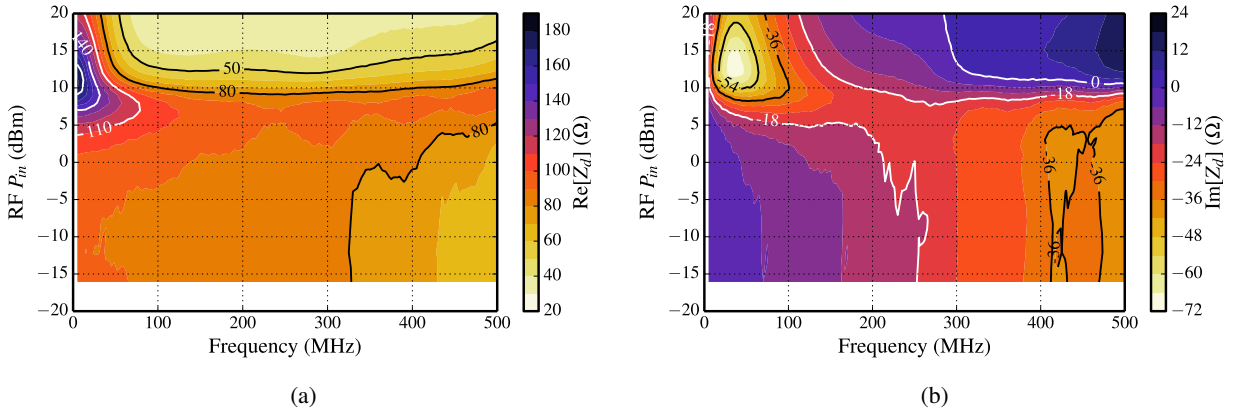


Figure 3.10: (a) Measured real and (b) imaginary part of the drain impedance of the $10 \times 90 \mu\text{m}$ device across frequency and RF input power for $V_d = 5 \text{ V}$.

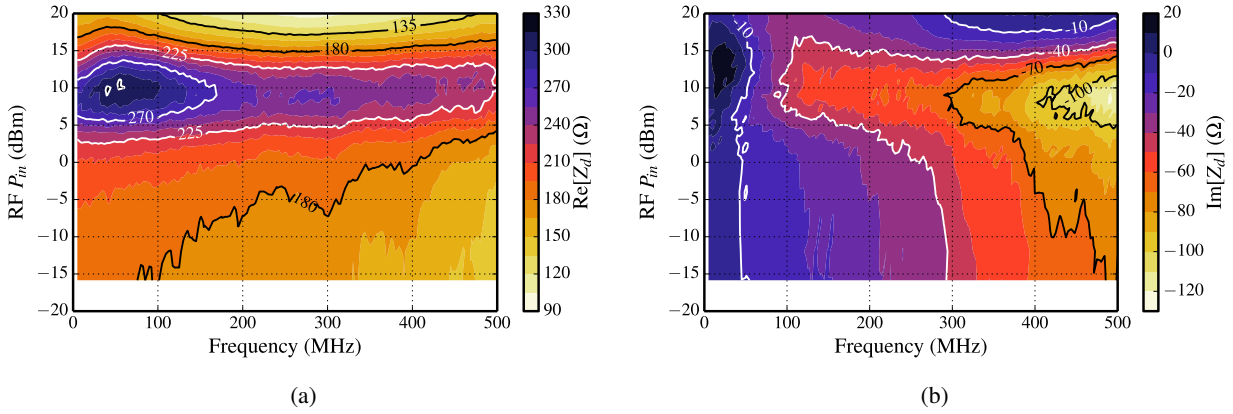


Figure 3.11: (a) Measured real and (b) imaginary part of the drain impedance of the $10 \times 90 \mu\text{m}$ device across frequency and RF input power for $V_d = 20 \text{ V}$.

parts of the drain impedance versus RF and LF baseband input power for an optimum-PAE RF load. When the transistor is biased in class-B (Fig. 3.13a), the impedance generally increases with baseband input power, P_{lf} , and decreases with RF input power, P_{rf} . At RF saturation for both 10 and 100 mA/mm, $\text{Re}[Z_d]$ is at a minimum and roughly uniform across $P_{in,lf}$ at 150Ω . However, at 100 mA/mm (Fig. 3.12a), there is a second impedance minimum for low RF and LF input power. Note that $\text{Im}[Z_d]$ also varies significantly over input powers and bias point (Fig. 3.12b, 3.13b).

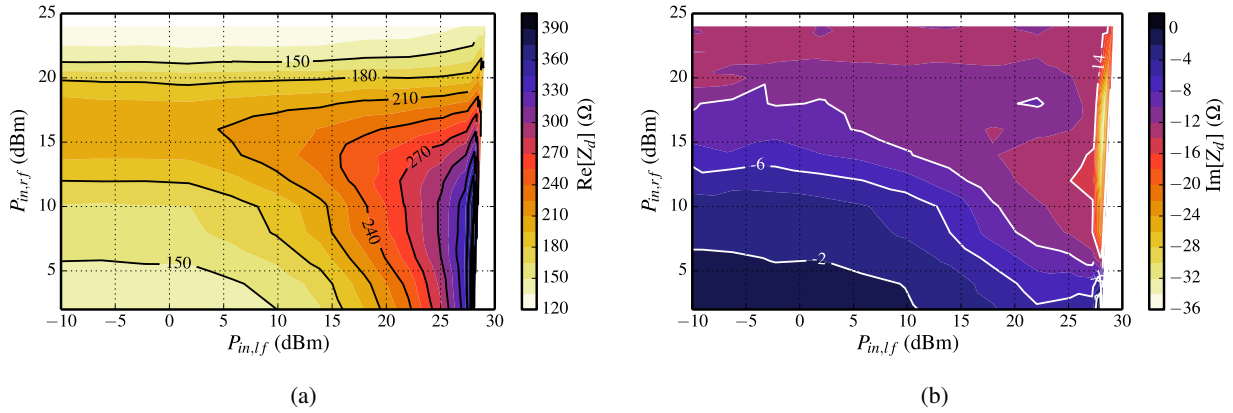


Figure 3.12: Measured real (a) and imaginary (b) drain impedance at 10 MHz and $V_d = 20$ V versus input RF and LF power at $I_{dq} = 100$ mA/mm for a 10×90 μm device.

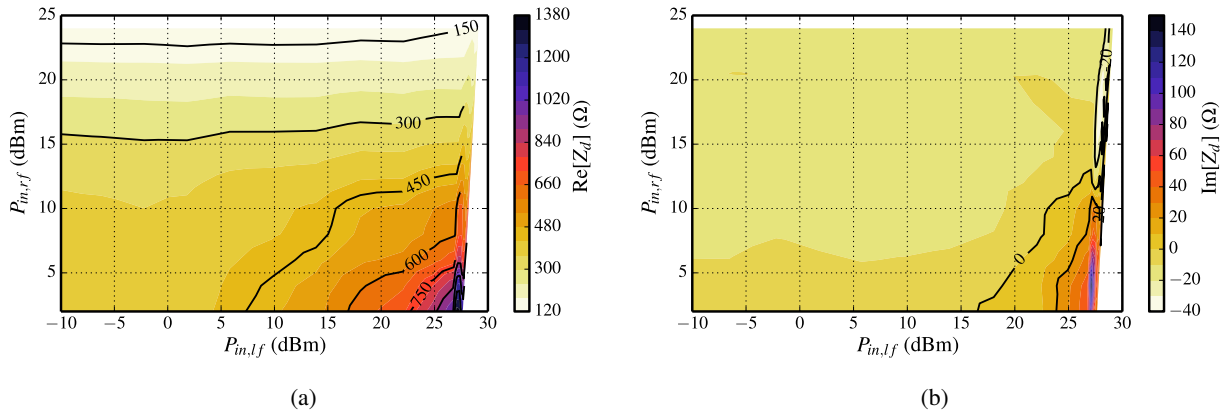


Figure 3.13: Measured real (a) and imaginary (b) drain impedance at 10 MHz and $V_d = 20$ V versus input RF and LF power at $I_{dq} = 10$ mA/mm for a 10×90 μm device.

3.6 CONCLUSION

As shown from the measurements in this chapter, the impedance variation of a GaN FET over various bias and input power can vary greatly. Table 3.1 details rough trends seen in the data. The primary control variable for the drain impedance of a FET is the gate bias voltage: it is the control knob that can pinch-off the device causing a drain impedance of 1000's Ω , or open the channel creating a short between the drain and the source. The drain supply has less of an effect compared to the bias, but still significant when the gate voltage is low and can vary the impedance by a factor of 2 when in a more pinched-off state. Additionally,

Table 3.1: Rough Trends of GaN FET Impedance. The trend is as the variable value increases.

Variable	Trend (variable value increasing)
V_g	decreases $Re[Z_d]$
V_d	Varies - Depends primarily on bias point (V_g) of device
$P_{in,rf}$	decreases $Re[Z_d]$
$P_{in,lf}$	increases $Re[Z_d]$
Frequency	Parallel RC until compression
RF Load	Varies - Changes large-signal loadline of device

the measurements can aid in creation of a compact nonlinear model tailored for supply modulation modes. Of particular note, the change in impedance behavior when varying the gate and drain bias points where the back-gate effect can be seen directly as in Figs. 3.6b and 3.6d.

CHAPTER 4

LOW FREQUENCY PA AND TRANSMITTER MEASUREMENTS

CONTENTS

4.1	GaN CLASS-B PA MEASUREMENT	52
4.2	TRANSMITTER MEASUREMENT - RESONANT MODULATOR	55
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In addition to transistor device-level measurements, the LF/RF bench can be used to characterize more integrated circuits and components. This chapter investigates MMIC power amplifiers and supply modulated transmitters with access to the node between the PA and supply modulator. It is shown that these measurements are a useful tool for evaluating a PA that will be used in conjunction with a supply modulation or in a supply modulated transmitter. To investigate the node between the supply modulator and the power amplifier only a 1-port calibration needs to be performed. In this chapter, the measurement results of a PA drain terminal are presented to evaluate the potential performance of the PA under supply modulation. Next, the PA is measured in conjunction with a resonant supply modulator to investigate PA/SM interaction.

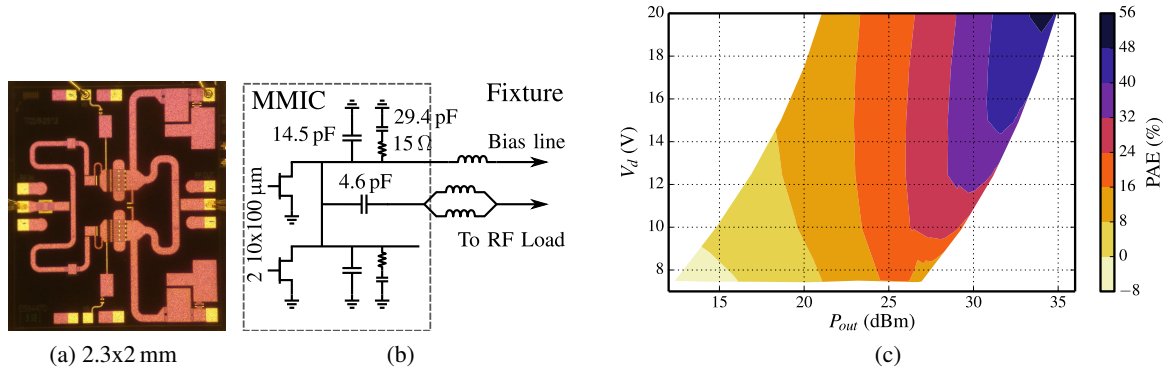


Figure 4.1: (a) Layout of X-band GaN MMIC power amplifier characterized for use in a supply modulated transmitter. Two $10 \times 100 \mu\text{m}$ devices are combined as a single stage amplifier. (b) Low frequency equivalent lumped element schematic. The shunt RC of 29.4 pF and 15Ω is for low frequency stability of the MMIC. The effective shunt capacitance on the MMIC is 87.8 pF . (c) Measured PAE of the amplifier shown in Fig. 4.1a versus output power and drain voltage.

4.1 GAN CLASS-B PA MEASUREMENT

A single-stage class-B power amplifier on $0.15 \mu\text{m}$ GaN was designed for to be used in a supply modulated transmitter and is detailed in [72]. The power amplifier combines 2 $10 \times 100 \mu\text{m}$ devices at the output for 2 mm of output stage gate periphery and 4 W of output power at saturation. A photograph is shown in Fig. 4.1a. The MMIC was mounted as in [72] with the off-chip drain capacitances removed. The measurement setup for a PA is simpler than the transistor setup as a bias network is already integrated on the MMIC and the designed diplexer (Fig. 2.5) is not needed. In addition to finding the impedance that the PA will present to the modulator, the purpose of the measurements here is to quantify how wide of a low frequency modulation bandwidth injected through the drain bias line is achievable with an existing power amplifier. For this particular MMIC, the bias network was not specially designed to diplex the LF and RF frequencies.

The low frequency equivalent circuit in Fig. 4.1b shows integrated capacitors and resistors on the MMIC and the interconnection to the measurement setup. The power amplifier was designed to work near pinch-off in class-B operation with 5 mA of quiescent current. The PAE measured at 10.1 GHz shown in Fig. 4.1c is highest at the nominal drain voltage bias of 20 V and high compression. Simultaneously, the impedance de-embedded to the off-chip end of the bondwire connected to the MMIC dc bias pad was measured across

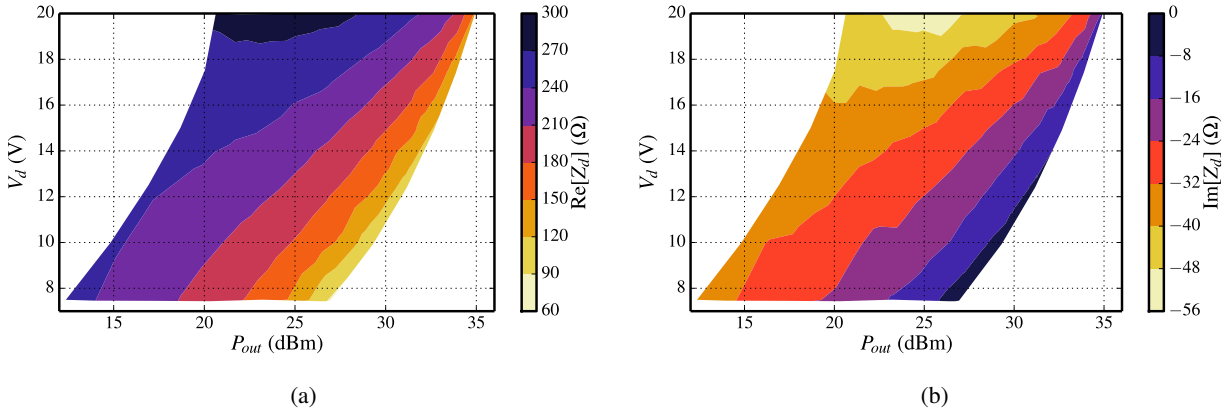


Figure 4.2: (a) Real and (b) imaginary part of the power amplifier bias line impedance at 1 MHz. At low input power, the PA is pinched off and presents a large impedance to the drain modulator. As the RF drive power increases, the real impedance decreases below $100\ \Omega$.

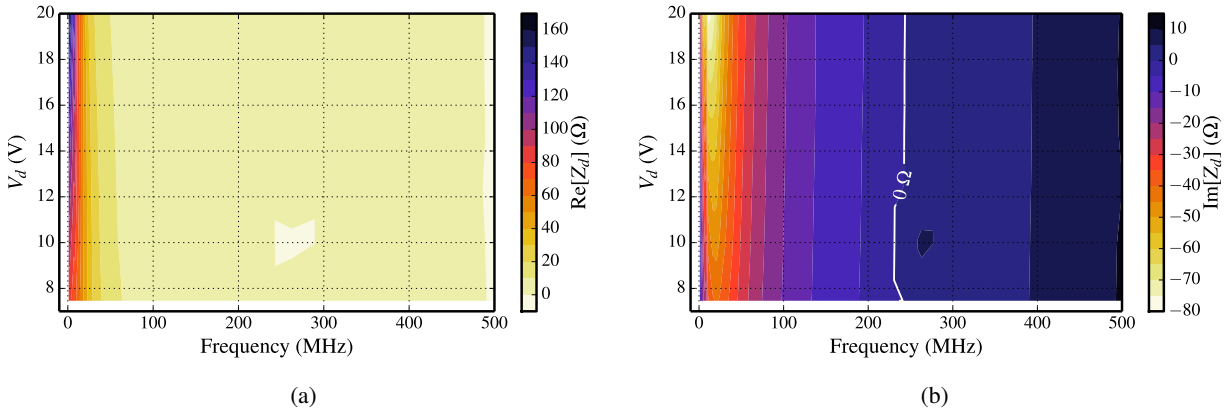


Figure 4.3: (a) Real and (b) imaginary impedance of the power amplifier bias line across frequency and drain voltage at 26 dBm input RF power. Because of the large bias line capacitance on-chip, the impedance above 80 MHz is nearly zero. The area at 250 MHz at 10 V had a measured negative real impedance indicating possible bias line instabilities.

the baseband frequency. Fig. 4.2a shows the impedance at 1 MHz. At this frequency the real part of the impedance decreases and the reactance increases with RF input power.

Fig. 4.3a and 4.3b show the impedance across frequency when the amplifier is compressed (approximately 34.5 dBm output power with $V_d = 20\ \text{V}$). The high bias line capacitance of 87.8 pF causes the impedance to be very low and roughly constant above 80 MHz. At a particular drain voltage, the impedance variation looks like a parallel RC for low frequencies. At higher baseband frequencies, the impedance looking into the

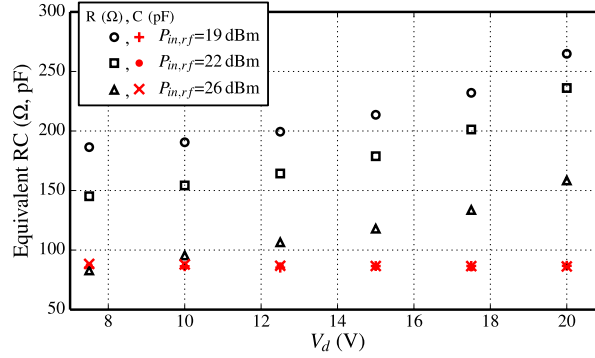


Figure 4.4: Extracted resistance and capacitance of the PA over drain voltage and at various input powers. The bias network capacitance overwhelms the small reactance of the transistors giving nearly constant equivalent capacitance over input power and drain voltage. The real part of the impedance, however, increases with V_d and decreases with $P_{in,rf}$ agreeing with the transistor measurements (Figs. 3.3a, 3.7).

bias line becomes inductive, as seen in Fig. 4.3b, caused by the wirebond to the die. The equivalent parallel RC of the PA (for frequencies under 100 MHz) is shown in Fig. 4.4. Over input power and drain voltage, the equivalent capacitance is very close to 88 pF; the bias line capacitance is the dominating factor for the reactive impedance. The resistive part of the impedance, however, depends on the drain voltage and input power, generally increasing with V_d and decreasing with $P_{in,rf}$.

Some of the conclusions that can be drawn from the measured data are:

- From Fig. 4.2a, it is seen that the real part of the drain impedance for a supply modulated PA varies substantially over drain voltage and output power. The imaginary part also varies significantly at the nominal drain voltage of 20 V. Therefore, the design of the signal-split from Fig. 1.7 will have a large impact on not only the PAE, but on the supply modulator efficiency which varies with loading.
- From Fig. 4.3, most of the frequency variation of the drain impedance is below 100 MHz. This is due to the on-chip capacitance. If this PA is used in as a supply modulated PA, the supply modulator's bandwidth and efficiency could be compromised because of the large impedance variation.
- Even when there are no off-chip drain bias capacitors, there is a large frequency variation in the impedance. With a more conventional power amplifier design with a bank of RF shorting capacitors, the bandwidth would be even more limited and stability a possible issue.

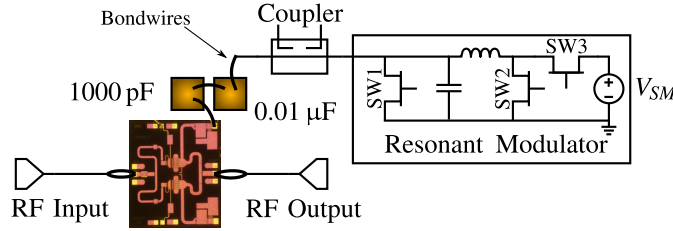


Figure 4.5: Block diagram of transmitter with MMIC power amplifier and resonant modulator. There are two bias line capacitors on the MMIC fixture totaling $0.011 \mu\text{F}$. The switches are controlled by an FPGA and are timed as shown in Fig. 4.6.

These measurements are representative of only one PA design and will be different for other designs. However, class-B was focused on here because it has the same bias point as other high-efficiency modes of operation (class-E, F, F^{-1}). Class-A power amplifiers will have less impedance variation as shown in the transistor measurements (Fig. 3.12a). However, under supply modulation, class-A PAs are limited to an efficiency of 50%. High-efficiency mode power amplifiers designed for supply modulation must take the bias network and transistor drain impedance variation into account.

4.2 TRANSMITTER MEASUREMENT - RESONANT MODULATOR

The measurement setup described here can also monitor performance of and interaction between a PA and supply modulator. The PA from the previous section is next connected to a supply modulator and the system measured with the low frequency coupler placed between the RFPA and modulator. The modulator in this case is not a standard dc-dc converter assisted with a linear amplifier commonly used for communication signals (e.g. [22]), but rather a resonant modulator for AM radar pulses. Radar supply modulation has been explored by other authors and the primary benefit includes reduced radiated spectral emissions. The resonant modulator is a simple design based on a damped LC resonant circuit and has been shown to reach efficiencies $>90\%$ [9, 11]. A simplified diagram of the resonant modulator designed for a resistive load of $\approx 50 \Omega$ is shown in Fig. 4.5. The inductance and capacitance are switched (using switches SW1, SW2, and SW3) into the circuit to charge and discharge, giving an approximate Gaussian output waveform shape. The switches are controlled by an FPGA and are timed as shown in Fig. 4.6 along with the simulated output waveforms.

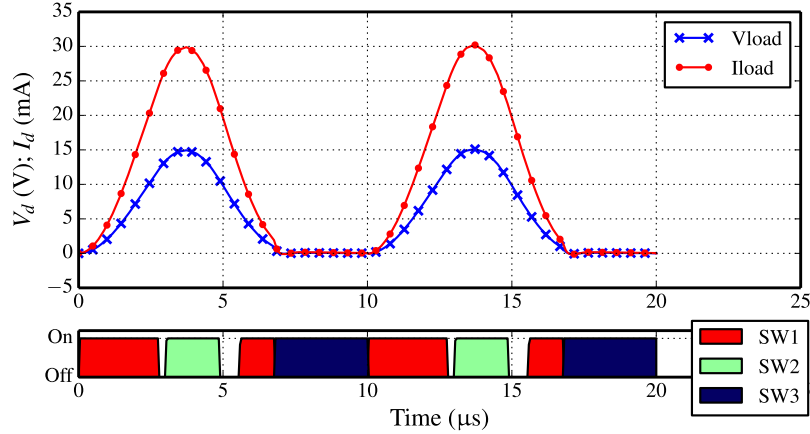


Figure 4.6: Simulated output voltage and current waveform with switching transitions for the resonant modulator with a $220\ \Omega$ resistive load. The switches control the current and voltage at the load by charging and discharging the capacitance and inductance in a controlled way to create an approximate Gaussian waveform shape.

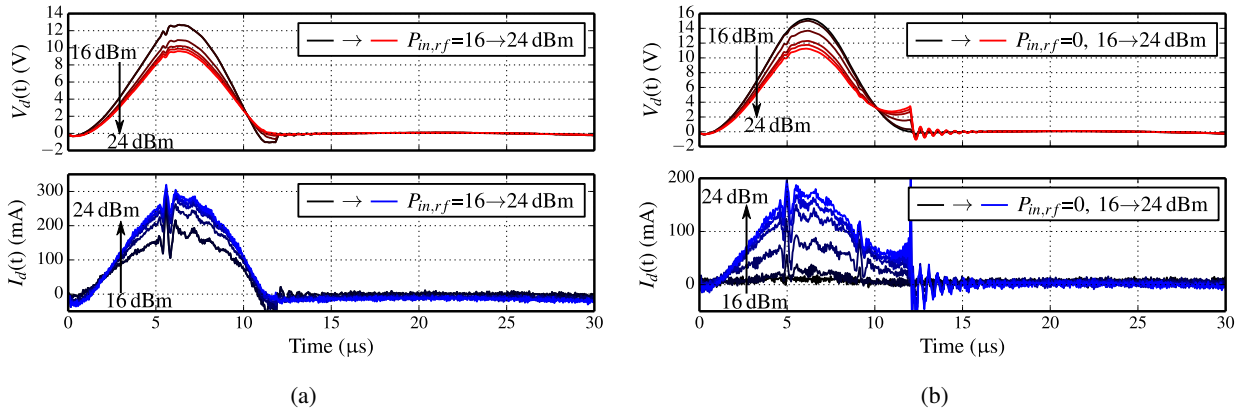


Figure 4.7: Time domain drain voltage and current measured at RFPA bias pad. The RFPA is biased at (a) $V_g = -3.0\ \text{V}$ and (b) $V_g = -4.5\ \text{V}$ while the modulator supply voltage is $V_{SM} = 8\ \text{V}$ for both plots (peak voltage will nominally occur at $2V_{SM} = 16\ \text{V}$).

Since the waveform of interest is no longer a continuous wave as the previous sections of the paper have been, it is more useful to consider the performance and PA/SM interaction in the time domain. Calibration and de-embedding are still performed in the frequency domain. The transmitter example in this paper uses a resonant modulator because it has a smooth and slow envelope that is well known and has a large voltage variation, going from $0\ \text{V}$ to the nominal voltage of the amplifier. In addition, the PA/SM combination is complete and is used as it would be in a system.

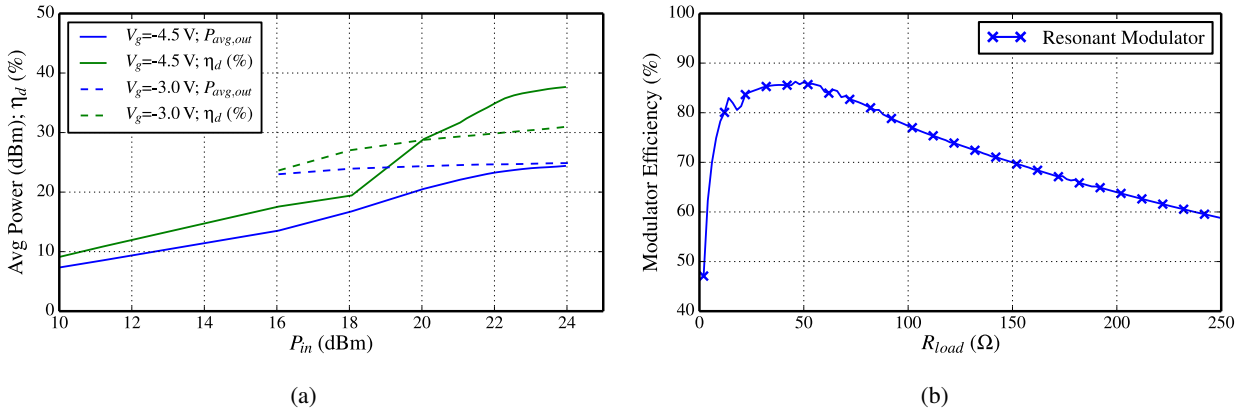


Figure 4.8: (a) RF average output power and drain efficiency over a pulse. By lowering the RFPA gate voltage, the efficiency can be increased with approximately the same output power. (b) Simulated efficiency of the resonant modulator and example buck converter versus a static resistive load.

The de-embedded voltage and current at the MMIC bias pad (off-chip capacitances were de-embedded) are shown in Fig. 4.7 for two different gate bias voltages. In the first case (Fig. 4.7a), the modulator switching times were adjusted for an optimum Gaussian shape for an input power of 24 dBm (red line). As the input power decreases from 24 dBm down to 16 dBm, the load that the modulator sees increases, giving a higher peak voltage and increasing the optimum discharging time for the capacitor causing a negative voltage at the end of the Gaussian pulse. The current follows the same Gaussian shape as the voltage, but there is current ringing at the peak of the pulse caused by SW1 turning off in the modulator.

In the second case (Fig. 4.7b), the modulator switching times were adjusted for an optimum Gaussian shape in the voltage for an input power of 0 dBm (black line) at a bias of $V_g = -4.5$ V. The voltage has a Gaussian shape, however the modulator is supplying very little power to the PA as the current is very low. As the RF input power increases, the modulator sees a decreasing load, decreasing the peak voltage of the modulator. Additionally, the optimum charging time for the capacitor is decreased giving the upswing in the voltage at the end of the Gaussian pulse for high RF input powers. However, it is evident the modulator is not designed for such a high load as there is no current into the PA even at the optimum input power of 0 dBm: there would be no efficiency improvement of the transmitter using a supply modulator because of the very low power that the resonant modulator supplies. This means that the resonant modulator would need to be redesigned if an input power of 0 dBm is desired with a very pinched off PA.

The average RF output power and drain efficiency of the RFPA is shown in Fig. 4.8a. With a more adequate load for the resonant modulator ($V_g = -3.0$ V), the RFPA only reaches 31% drain efficiency. The efficiency can be increased to 38% by pinching the device off, however, large distortions are apparent in the current waveforms from the modulator. There is a clear trade-off between RFPA efficiency and modulator distortion, which translates to distortion of the RF output pulse. Moreover, the resonant modulator works best for a particular load, in this case about 50Ω as shown in Fig. 4.8b. Under pinch-off, the resonant modulator is far from the optimum load impedance as the transistor has a very high impedance.

4.3 CONCLUSION

The low frequency measurement setup is used as a diagnostic tool for investigating and optimizing the performance of power amplifiers and modulators when connected to the RFPA. Measuring the drain bias node under large-signal operation characterizes the potential supply modulation bandwidth that the PA can handle. The limiting factor is due to the on-chip (or off-chip) capacitance. If these capacitances are eliminated to provide wider baseband bandwidths or flatter impedance variation within the bandwidth, stability of the PA may be a potential issue.

By observing the voltage and the current at the RFPA bias line, distortion and SM/RFPA interactions can easily be seen. Fig. 4.8 illustrate a trade-off between RFPA efficiency and linearity performance of the modulator. In this case to keep a Gaussian shape for different loads, the modulator switching times can be adjusted for the load variation of the RFPA by a simple look-up table. The more optimum solution for output power control is by adjusting the resonant modulator supply voltage directly decreasing the amplitude of the Gaussian pulse. The RF output power versus supply voltage is shown in Fig. 4.9. As shown in previous sections, the impedance variation over drain voltage is smaller than the impedance variation over RF input power.

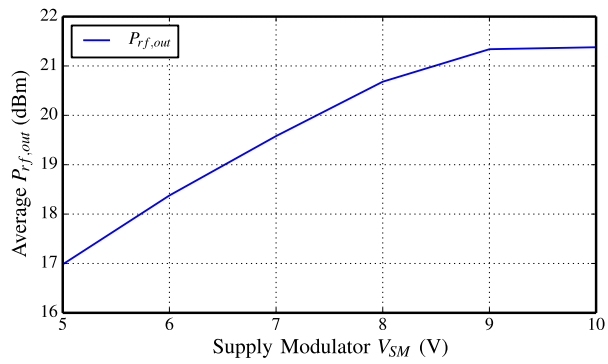


Figure 4.9: RF output power versus supply modulator voltage, V_{SM} . The supply voltage affect the average output power which may have less drain impedance variation than changing the RF input power.

CHAPTER 5

NONLINEAR MULTI-TONE ANALYSIS USING DESCRIBING FUNCTIONS

CONTENTS

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Previous efforts in characterizing nonlinear elements have focused on Volterra series [75–80]. Volterra series can accurately describe nonlinear circuits that are only mildly nonlinear (requiring low orders of mixing products) and, depending on the extraction method of the Volterra kernels, gives the effect of the nonlinearities as dependent sources in the circuit [78,81]. However, for the analysis in this thesis, it is desired to have a large-signal analysis method. A description of the effects of a large-signal supply variation on the transistor, especially under RF saturation, is needed to predict performance under supply modulation. To

be able to model the complicated $I_{ds}(V_{gs}, V_{ds})$ dependency of transistors, describing functions (DF) will be used [82]. The describing function method uses quasi-linearization and has an advantage over Volterra series in that the extracted functions are *dependent* on the amplitude of input signals, and in extension, can be shown to have “no limit in the range of signal magnitudes” [82]. This property is incredibly useful in that it can explain small-signal and large-signal phenomena in a single compact formula. However, describing functions rely on knowing the input waveform and the ability to integrate the nonlinear element equation. These issues as well as methods for addressing them, will be discussed later in this chapter.

A short introduction to a basic Volterra series formulation (as presented in [78]) is first presented detailing the foundation of the series and an extraction method for describing nonlinear circuits. Some issues are highlighted, which motivate the application of DF theory. A shunt diode is used as an example for DF to illustrate benefits and pitfalls of this method.

5.1 BASIC VOLTERRA SERIES

The Volterra series is a generalization of the Taylor series expansion of a function that includes memory (past output values influence current output values). If the nonlinear function (or system) is time-invariant, the input-output relationship can be given as a sum of operators that act on the input signal:

$$y(t) = \mathbf{H}_1[x(t)] + \mathbf{H}_2[x(t)] + \mathbf{H}_3[x(t)] + \dots + \mathbf{H}_n[x(t)] \quad (5.1)$$

A block diagram representation of (5.1) is shown in Fig. 5.1. Each operator, $\mathbf{H}_n[x(t)]$, is known as the n -th order Volterra operator:

$$\mathbf{H}_n[x(t)] = \int_{-\infty}^{\infty} d\tau_1 \dots \int_{-\infty}^{\infty} d\tau_n h_n(\tau_1, \dots, \tau_n) x(t - \tau_1) \dots x(t - \tau_n). \quad (5.2)$$

The function, $h_n(\tau_1, \dots, \tau_n)$, is the n -th order Volterra kernel. For example, a first-order system $y(t) = \mathbf{H}_1$ with a step function input, $u(t)$, is the unit impulse response of the system, $h_1(t)$:

$$\mathbf{H}_1[u(t)] = \lim_{\delta \rightarrow 0} h_1(t, \delta) = h_1(t), \quad (5.3)$$

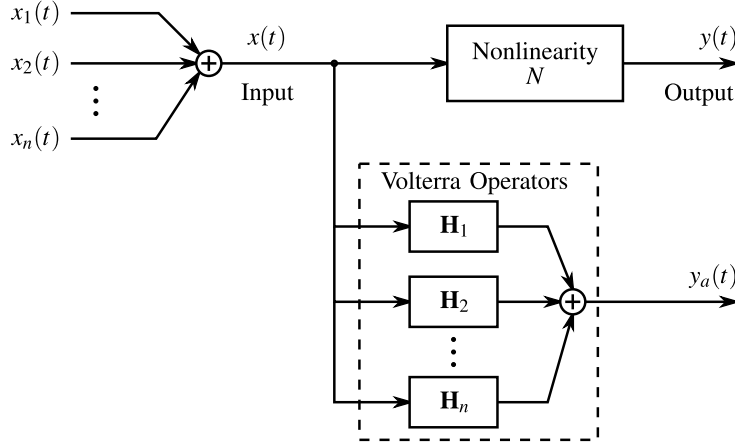


Figure 5.1: Block diagram for the sum of the operators of the n -th order Volterra series. Each input $x_n(t)$ is an input that is independent of all the other inputs.

and with (5.2), the system output becomes

$$y(t) = \int_{-\infty}^{\infty} d\tau h_1(\tau)x(t - \tau). \quad (5.4)$$

For simplification, and since we are interested almost solely in sinusoidal input and responses, (5.2) can be transformed into the frequency domain by multidimensional Fourier transforms. Equation (5.2) can be thought of as the n -th nonlinear transfer function and written as:

$$\mathbf{H}_n[\omega_{q1}, \omega_{q2}, \dots, \omega_{qn}] = \int_{-\infty}^{\infty} d\tau_1 \dots \int_{-\infty}^{\infty} d\tau_n h_n(\tau_1, \dots, \tau_n) \exp[-j(\omega_{q1}\tau_1 + \dots + \omega_{qn}\tau_n)] \quad (5.5)$$

and subsequently, the output

$$y(t) = \sum_{n=1}^N \frac{1}{2^n} \sum_{q_1=-Q}^Q \dots \sum_{q_n=-Q}^Q A_{q1} \dots A_{qn} \mathbf{H}_n(\omega_{q1}, \omega_{q2}, \dots, \omega_{qn}) \exp[-j(\omega_{q1} + \dots + \omega_{qn})t], \quad (5.6)$$

where A_{qn} are the amplitudes of the q_n -th input sinusoid. A first-order system in the frequency domain becomes:

$$\begin{aligned} y(t) &= \int_{-\infty}^{\infty} d\tau h_1(\tau)e^{j\omega(t-\tau)} \\ &= \mathbf{H}_1(j\omega)e^{j\omega t}. \end{aligned} \quad (5.7)$$

Now the question becomes, how are the Volterra operators found? There have been a number of publications that detail three main methods for extracting the operators; formulation of a differential equation and

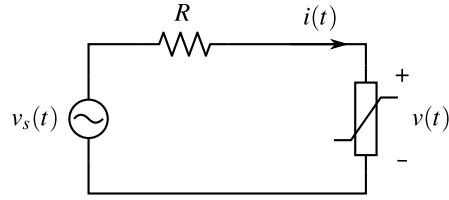


Figure 5.2: Circuit for analysis of a generic nonlinear current that is a function of the voltage, $v(t)$.

solving assuming a Volterra series input [76], harmonic-input method [78, 83], and the method of nonlinear currents [78, 81]. The more common methods of harmonic-input and nonlinear currents solve the circuit in an iterative fashion, requiring computation of the lower order responses (operators) before higher orders can be computed. Volterra series are used for analysis of weakly nonlinear circuits or systems and as such are useful for describing intermodulation [78].

5.2 BASIC VOLTERRA SERIES - SHUNT DIODE EXAMPLE

An example will be used to explore the application of Volterra series to nonlinear elements. The nonlinear transfer functions, \mathbf{H}_n , will be found by the method of nonlinear currents: to find the n -th order response the circuit is assumed to have a n -th order sinusoidal input (sum of positive-frequency phasors) and the voltage and currents are algebraically solved with the circuit equations [78]. This is an iterative process because the n -th order response necessarily is a function of the voltage and currents of orders lower than the n -th order.

5.2.1 GENERAL NONLINEAR ELEMENT

Fig. 5.2 shows a circuit diagram of a generic nonlinear element that will be analyzed with Volterra series. In this case, the nonlinear element equation is real and single-valued making a power series analysis equally valid. The voltage source, $v_s(t)$, is an arbitrary input. However, for ease in analysis and determining the Volterra series coefficients, it will be assumed to be a multi-tone source with non-commensurate frequencies. This means that the excitation frequencies are not harmonics of each other. The nonlinear element characteristic function can be represented by a Taylor series about some dc bias point. In this case, the characteristic

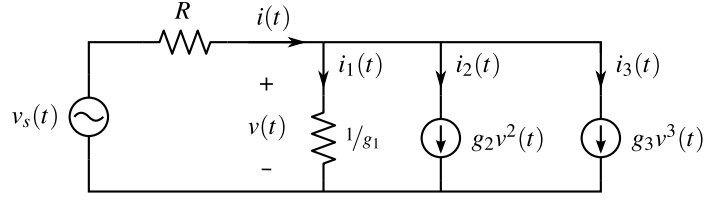


Figure 5.3: The nonlinear element is decomposed into higher-order voltages and currents. By superposition, each order term (for example, second order in Fig. 5.4) can be solved independently in a linear fashion.

function will be controlled by the voltage across the element and specify the current through it:

$$i(t) = g_1 v(t) + g_2 v^2(t) + g_3 v^3(t) + \dots, \quad (5.8)$$

where g_n are coefficients for the higher order nonlinear effects of the element. For this example, the nonlinearity will be restricted to 3rd order in the analysis even though the nonlinear element may have an infinite Taylor series. Since the input frequencies are non-commensurate, the higher-order voltages ($v^2(t)$ and $v^3(t)$) *must* be created by the nonlinear element. Keeping this in mind, the total voltage can be written as a sum of the higher-order mixing products, $v_n(t)$, and the higher-order voltages can be written in terms of the mixing products:

$$v(t) = v_1(t) + v_2(t) + v_3(t) \quad (5.9)$$

$$v^2(t) = v_1^2(t) \quad (5.10)$$

$$v^3(t) = v_1^3(t) + 2v_1(t)v_2(t). \quad (5.11)$$

Since the voltages can be separated out in higher-order components, it is beneficial to do the same to the higher-order currents:

$$i(t) = i_1(t) + i_2(t) + i_3(t) \quad (5.12)$$

$$i_1(t) = g_1(v_1(t) + v_2(t) + v_3(t)) \quad (5.13)$$

$$i_2(t) = g_2 v_1^2(t) \quad (5.14)$$

$$i_3(t) = 2g_2 v_1(t)v_2(t) + g_3 v_1^3(t) \quad (5.15)$$

The nonlinear element Fig. 5.2 can now be decomposed into multiple current sources that denote higher order terms as shown in Fig. 5.3.

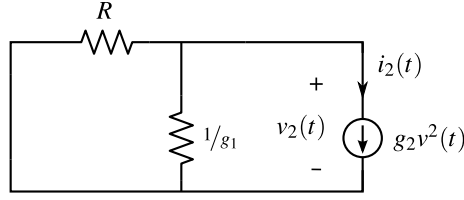


Figure 5.4: Second order voltages and currents from Fig. 5.3.

The input source, $v_s(t)$, has Q tones at $\pm\omega_q$

$$v_s(t) = \frac{1}{2} \sum_{q=-Q}^Q V_{s,q} \exp(j\omega_q t) \quad Q \neq 0 \quad (5.16)$$

The positive and negative frequency components are needed to generate the correct mixing terms. The first order voltage, $v_1(t)$, can be solved by setting all the higher-order current sources to zero.

$$v_1(t) = \frac{1/g_1}{1/g_1 + R} v_s(t) = \frac{1}{g_1 R + 1} \left[\frac{1}{2} \sum_{q=-Q}^Q V_{s,q} \exp(j\omega_q t) \right] \quad (5.17)$$

Now the second order current can be calculated from (5.14).

$$i_2(t) = g_2 v_1^2(t) = g_2 \left(\frac{1}{g_1 R + 1} \right)^2 \left[\frac{1}{4} \sum_{q_1=-Q}^Q \sum_{q_2=-Q}^Q V_{s,q_1} V_{s,q_2} \exp[j(\omega_{q_1} + \omega_{q_2})t] \right] \quad (5.18)$$

The second order voltage is found by setting all current and voltage sources that do not have a second-order component to zero as shown in Fig. 5.4. The voltage source is now a short because there is no frequency component that coincides with the second order frequency terms. The only source is the current generated from the nonlinear element.

$$v_2(t) = \frac{-1}{g_1 R + 1} R g_2 i_2(t) = \frac{-1}{g_1 R + 1} R g_2 \left(\frac{1}{g_1 R + 1} \right)^2 \left[\frac{1}{4} \sum_{q_1=-Q}^Q \sum_{q_2=-Q}^Q V_{s,q_1} V_{s,q_2} \exp[j(\omega_{q_1} + \omega_{q_2})t] \right] \quad (5.19)$$

Now the third-order current can be calculated from the lower order voltages (5.17) and (5.19). The two components that contribute to the current in (5.15) are split apart for better visualization on paper:

$$i_3(t) = 2g_2 v_1(t)v_2(t) + g_3 v_1^3(t) = i_{3a}(t) + i_{3b}(t) \quad (5.20)$$

$$i_{3a}(t) = 2g_2^2 R \frac{-1}{g_1 R + 1} \left(\frac{1}{g_1 R + 1} \right)^3 \left[\frac{1}{8} \sum_{q_1=-Q}^Q \sum_{q_2=-Q}^Q \sum_{q_3=-Q}^Q V_{s,q_1} V_{s,q_2} V_{s,q_3} \exp[j(\omega_{q_1} + \omega_{q_2} + \omega_{q_3})t] \right] \quad (5.21)$$

and

$$i_{3b}(t) = g_3 \left(\frac{1}{g_1 R + 1} \right)^3 \left[\frac{1}{8} \sum_{q_1=-Q}^Q \sum_{q_2=-Q}^Q \sum_{q_3=-Q}^Q V_{s,q_1} V_{s,q_2} V_{s,q_3} \exp[j(\omega_{q_1} + \omega_{q_2} + \omega_{q_3})t] \right]. \quad (5.22)$$

Finally, the 3rd order voltage can be found as

$$v_3(t) = R \frac{-1}{g_1 R + 1} i_3(t). \quad (5.23)$$

5.2.2 DIODE TWO-TONE EXCITATION

The previous derivation was for a general nonlinear element in which the nonlinearity can be expanded in a Taylor series. The coefficients of the nonlinearity are denoted by the g_n variables. Now a specific diode nonlinearity is considered:

$$i_{diode}(v) = I_0 \left(\exp \left(\frac{qv}{\eta kT} \right) - 1 \right), \quad (5.24)$$

where q is the charge of an electron, k is Boltzmann's constant, T is the temperature of the device in Kelvin, η is the ideality factor, and I_0 is the saturation current of the diode. The exponential constant terms will be denoted as

$$\alpha = \frac{q}{\eta kT} \quad (5.25)$$

Since the characteristic equation of the element contains an exponential, the Taylor series is infinite and must be truncated to a limited number of terms. In this example, 3rd order is sufficient for demonstration purposes. The Taylor expansion of the diode with a bias point of V_{dc} is

$$\begin{aligned} i_{diode}(v) \simeq & I_0(e^{\alpha V_{dc}} - 1) + I_0 \alpha e^{\alpha V_{dc}} (V - V_{dc}) + \frac{I_0 \alpha^2}{2} e^{\alpha V_{dc}} (V - V_{dc})^2 \\ & + \frac{I_0 \alpha^3}{6} e^{\alpha V_{dc}} (V - V_{dc})^3 + \mathcal{O}[V - V_{dc}]^4, \end{aligned} \quad (5.26)$$

where $\mathcal{O}[V - V_{dc}]^4$ are the remaining terms in the Taylor series higher than 3rd order. However, solving for the dc bias point requires solving the transcendental equation

$$v = v_s - I_0 (\exp(\alpha v) - 1) R. \quad (5.27)$$

The voltage and current (with a series $R = 10 \Omega$) are shown in Fig. 5.5. A few different bias points will be used and are shown in Fig. 5.5 and coefficients detailed in Table 5.1. The constants used for (5.24) are listed in Table 5.2.

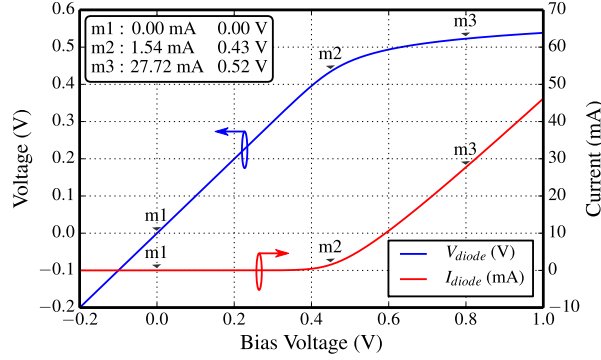


Figure 5.5: I - V characteristic curve of the diode. Three dc bias points are marked: (m1) off, (m2) knee, (m3) saturation.

For a two-tone input, the source, $v_s(t)$, is now restricted to $Q = 2$. Since the I - V characteristic curve is a real function and contains no frequency dependent parameters, the fundamental frequencies can be anything without the results changing. Additionally, the positive and negative frequency component coefficients will be equal: $\omega_{-2} = \omega_2$, $\omega_{-1} = \omega_1$, $V_{s,-1} = V_{s,1}$, $V_{s,-2} = V_{s,2}$. For comparison, a harmonic balance simulator was used to compare the results of the Volterra series. For the HB simulation, 1 GHz and 1.01 GHz were used as the two fundamental tones. Two mixing products are compared versus equal (in amplitude and phase) voltage input tones, v_s : the 1 GHz fundamental voltage and lower intermodulation mixing product at 0.99 GHz. Expanding (5.9) with (5.17), (5.19), and (5.23) and picking out only the $e^{j\omega_1 t}$ terms gives:

$$v_{1\text{GHz}} = \frac{V_1}{(g_1 R + 1)} + \frac{2g_2^2 R^2 V_1^3}{(g_1 R + 1)^5} - \frac{g_3 R V_1^3}{(g_1 R + 1)^4}. \quad (5.28)$$

This is a cubic function of amplitude (V_1) only in 1st and 3rd order. This will not accurately model the

Table 5.1: Taylor series diode coefficients

V_s (V)	V_{dc} (V)	I_{dc} (mA)	g_1	g_2	g_3
0.0	0	0	$3.28 \cdot 10^{-8}$	$5.37 \cdot 10^{-7}$	$5.87 \cdot 10^{-6}$
0.45	0.435	1.54	0.05046	0.82711	9.03786
0.8	0.523	27.72	0.90872	14.8944	162.752

Table 5.2: Diode parameter constants

I_0 (mA)	η	T (K)	R (Ω)
$1 \cdot 10^{-6}$	1.2	295	10

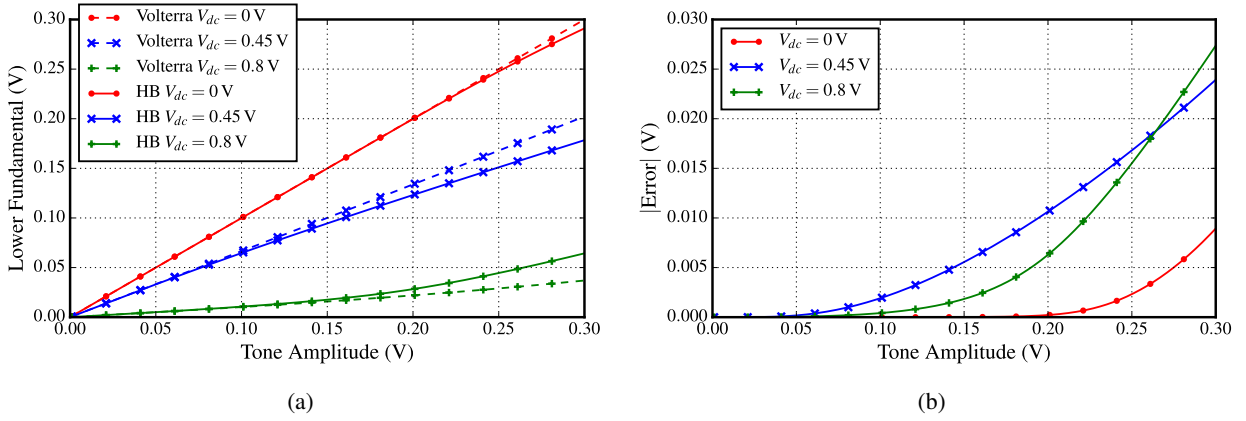


Figure 5.6: (a) Lower fundamental voltage (1 GHz) across the diode for three different bias voltages and (b) error as compared to harmonic balance simulation.

fundamental tone for large input tone powers since the nonlinear characteristic function is exponential which requires infinite terms for convergence. Computing higher order terms, however, increases computation and complexity significantly as the mixing terms increase exponentially. Additionally, the lower intermodulation mixing product at 0.99 GHz can be computed in a similar manner picking only the terms with $e^{j(2\omega_1+\omega_2)t}$:

$$v_{0.99 \text{ GHz}} = -\frac{3RV_1^2V_2(g_1g_3R - 2g_2^2R + g_3)}{(g_1R + 1)^5}. \quad (5.29)$$

Similar to (5.28), the lower IM3 product is a cubic limiting the convergence over input voltages.

Fig. 5.6 shows the results of the Volterra and HB simulation for the fundamental voltage across the diode. At lower tone amplitudes ($V_{s,1}$ and $V_{s,2}$) the Volterra series matches very well with the HB simulation as expected. However, since the Volterra series is a linearization of the circuit, at higher input tone powers, the Volterra result diverges significantly from the HB result. The bias points chosen accentuate some the properties of the Volterra series convergence. The lowest error (for the largest range of input voltages) is at a bias point of $V_{dc} = 0$ V. Comparing to Fig.5.5, this bias point has the largest range where the input voltage will not intersect either the knee or saturation region of the diode (m2 or m3). However, the largest error voltages (for low input voltage) is with the bias point directly on the knee of the diode at $V_{dc} = 0.45$ V: the convergence of the Volterra series is very poor for nonlinear elements that have quickly varying characteristic functions with respect to the control variables (in this case the voltage across the diode). The largest error is at the $V_{dc} = 0.8$ V in the saturation region: the large nonlinearity from the exponential function creates

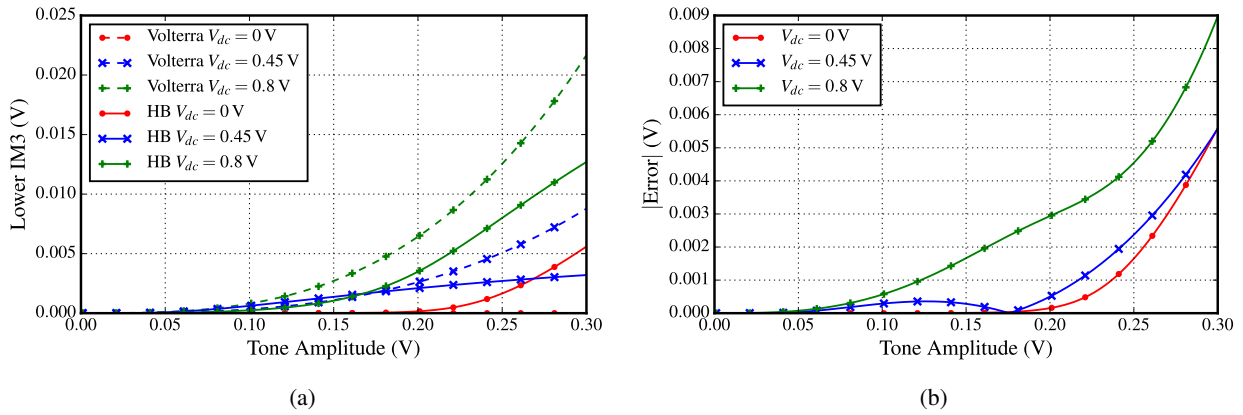


Figure 5.7: (a) Lower intermodulation product (0.99 GHz) voltage across the diode for three different bias voltages and (b) error as compared to harmonic balance simulation.

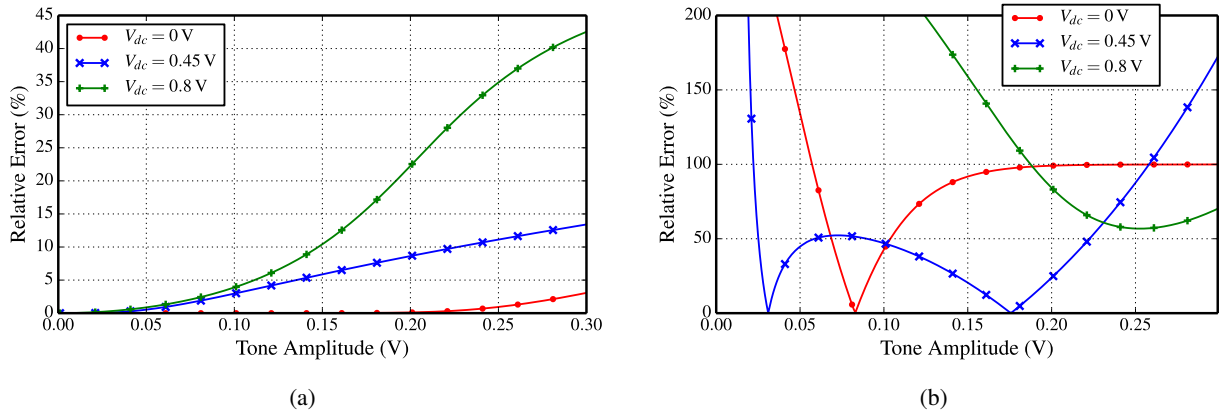


Figure 5.8: (a) Relative error to the harmonic balance simulation for the lower fundamental voltage (1 GHz) across the diode and (b) lower intermodulation product (0.99 GHz) voltage across the diode for three different bias voltages.

large mixing products that the Volterra series does not model well at high input voltage amplitudes.

Looking at the lower IM3 product shown in Fig. 5.7, results are similar for the lowest bias point of $V_{dc} = 0$ V. However, the Volterra series has larger error modeling the 3rd order mixing at the higher bias point of $V_{dc} = 0.8$ V as compared to the bias point at the knee of the diode.

The relative error for both frequency components and all bias points are shown in Fig. 5.8. The exceedingly high relative errors for the lower intermodulation product (Fig. 5.8b) is due to the low voltages generated at low input amplitudes: a small numerical error divided by a much smaller number gives a large error even though the absolute error is small (Fig. 5.7b).

All told, the Volterra series, even with very small orders, models a nonlinear well with small input amplitudes, in this case > 0.05 V for both RF tones. For larger input voltages, the Volterra series diverges significantly, depending on the bias point and mixing product desired.

5.2.3 LIMITATIONS OF VOLTERRA SERIES

Extraction of the Volterra series requires that the nonlinearity be a power series or a Taylor series (for non-polynomial function) about a bias point. The fitting of the power series to the nonlinearity restricts that applicability for Volterra series to small-signal and weakly nonlinear circuits as can be seen by the previous example. Convergence for complicated nonlinearities or input signals of moderate magnitude is questionable and highly dependent on the type of nonlinearity. In addition, the Volterra operators are *independent* of amplitude meaning that the solution obtained is linearized about a single static operating point. However, the methods outlined in [78] allow for the complete solution of a general circuit without restrictions to the type of elements (aside from the type of nonlinearity). No assumptions are made about the input to the nonlinear element.

5.3 DESCRIBING FUNCTIONS

Describing functions (DF) are an alternative analysis method for nonlinear systems and differential equations. DF have certain assumptions compared to Volterra series that greatly simplify the analysis of nonlinear systems. The DF method is a quasi-linearization of a system which means that the approximated output is a linear operation that depends on the input of a signal of finite size. This, however, leads to the necessary knowledge of the type (and amplitude) of the input signal, as independent signals will *not* have independent outputs. When considering microwave circuits, the type of input and output signal is generally a sum of sinusoids. This brings up an additional requirement that any feedback from the nonlinear output back to the input must be adequately filtered so the original input form still holds. A major benefit of using DF (compared to Volterra series) is the ability to solve systems with hysteresis and with large input signals. The DF method is dependent on the input and is suitable for analysis of nonlinear elements at all input amplitudes.

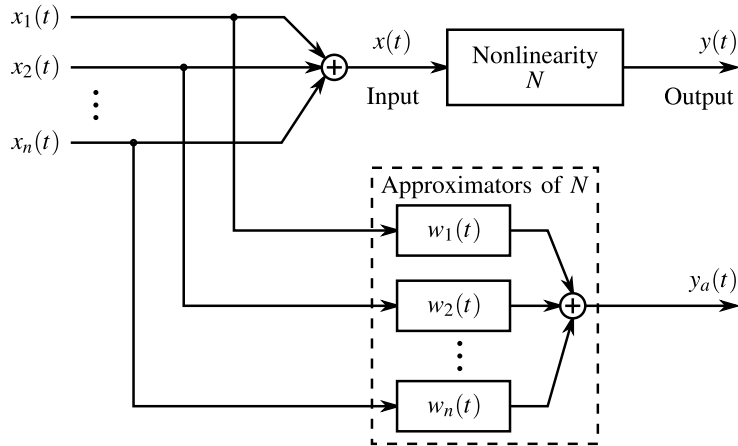


Figure 5.9: Generalized block diagram for the DF method. Each “approximator” is an optimum function that describes the nonlinearity N . Each input $x_n(t)$ has a separate form (for example sinusoidal input or a constant bias input) and a separate optimum function, $w_n(t)$, that operates on that particular input form.

In addition, analyzing outputs at higher frequency orders are straightforward as they do not take any more effort to compute than the first order output case.

There are many describing functions and the choice of DF is dependent on the form of the input signal to the nonlinearity (albeit the DF for a particular form is the same for all nonlinearities). Here, basic theory for describing functions is covered and a sinusoidal input DF is derived. The full derivation is detailed in [82], however, relevant details for background theory and of sinusoidal describing functions are repeated here for completeness. In particular, the derivation is generalized for signals in phasor form instead of the typical sinusoidal derivation form. After the DF is found, extensions are made to two- and multi-sinusoid inputs. The DF approach for multiple dependent variable nonlinear functions is discussed. Finally, implementation issues and methods to overcome them are considered.

5.3.1 DF DERIVATION

The DF based analysis is formulated as a sum of quasi-linear input-dependent approximators to a nonlinear element as shown in Fig. 5.9. In Fig. 5.9, each input, $x_i(t)$, is a separate type of input, for example a sinusoidal or Gaussian noise input. A particular type of input, $x_1(t)$, is operated on by the optimal approximator for that input type, $w_1(t)$. The sum of all the optimal functions gives the approximate output $y_a(t)$. The question is,

how is the approximator found or computed? The minimum mean squared error is used as the criterion for the derivation of a describing function [82, 84, 85]. The error in the approximation as given in Fig. 5.9 is

$$e(t) = y_a(t) - y(t) \quad (5.30)$$

and the mean-squared error of the approximation is

$$\overline{e(t)^2} = \overline{y_a(t)^2} - 2\overline{y_a(t)y(t)} + \overline{y(t)^2}, \quad (5.31)$$

where the overline denotes the expected value of the function. The convolution of the i -th approximator and the input to the i -th approximator is taken to give the approximated output:

$$y_a(t) = \sum_{i=1}^n \int_0^{\infty} d\tau w_i(\tau) x_i(t - \tau). \quad (5.32)$$

Other terms in (5.31) are

$$\overline{y_a(t)^2} = \sum_{i=1}^n \sum_{j=1}^n \int_0^{\infty} d\tau_1 \int_0^{\infty} d\tau_2 w_i(\tau_1) w_j(\tau_2) \phi_{ij}(\tau_1 - \tau_2), \quad (5.33)$$

$$\overline{y_a(t)y(t)} = \sum_{i=1}^n \int_0^{\infty} d\tau w_i(\tau) \overline{y(t)x_i(t - \tau)}, \quad (5.34)$$

where

$$\phi_{ij}(\tau_1 - \tau_2) = \overline{x_i(t)x_j(t + \tau)}. \quad (5.35)$$

The goal is to show that $\overline{e(t)^2}$ is stationary with respect to small variations in $w_i(t)$. Small perturbations ($\delta w_i(t)$) are added

$$w_i(t) = w_i(t) + \delta w_i(t). \quad (5.36)$$

The first-degree $\delta w_i(t)$ terms in $\overline{e(t)^2}$ must vanish for the error to be stationary and the second-degree term must be positive to give a minimum error. The first-degree term with respect to the perturbation in the approximator is

$$\delta \overline{e(t)^2} = 2 \sum_{i=1}^n \int_0^{\infty} d\tau_1 \delta w_i(\tau_1) \left[\sum_{j=1}^n \int_0^{\infty} d\tau_2 w_j(\tau_2) \phi_{ij}(\tau_1 - \tau_2) - \overline{y(t)x_i(t - \tau_1)} \right], \quad (5.37)$$

and the second-degree term is

$$\delta^2 \overline{e(t)^2} = \sum_{i=1}^n \sum_{j=1}^n \int_0^{\infty} d\tau_1 \int_0^{\infty} d\tau_2 \delta w_i(\tau_1) \delta w_j(\tau_2) \phi_{ij}(\tau_1 - \tau_2). \quad (5.38)$$

The second-degree term has the same form as the mean-squared output of the linear approximator, $\overline{y_a(t)^2}$, in (5.33). The previous equation can be considered as the mean-squared value for weighting functions of $\delta w_i(\tau_1)$ applied to inputs $x_i(t)$. This must be positive because of the nature of the convolution, giving the mean squared error a minimum value. However, the first-degree term must also be zero for a minimum in the error. This requires

$$\sum_{j=1}^n \int_0^{\infty} d\tau_2 w_j(\tau_2) \phi_{ij}(\tau_1 - \tau_2) = \overline{y(t)x_i(t - \tau_1)} \quad (5.39)$$

for positive τ_1 , $i = 1, \dots, n$. The interpretation of (5.39) is that the cross-correlation between the input and approximate output must equal the cross-correlation between the input and the actual output of the nonlinear element:

$$\overline{x_i(t)y_a(t + \tau_1)} = \overline{x_i(t)y(t + \tau_1)} \quad i = 1, \dots, n \quad (5.40)$$

This must be true for *each* component of the input. The cross-correlation equivalence is also required for all optimum linear filter theories based on mean-squared-error such as the Wiener filter [82].

5.3.2 DF FOR SINUSOIDAL INPUT

For a sinusoidal input, $x(t) = V \cos(\omega t + \theta)$, the optimal approximator (in a least squares sense) is

$$N_1 = n_p + jn_q \quad (5.41)$$

$$n_p = \overline{2y(0) \cos \phi},$$

$$n_q = \overline{2y(0) \sin \phi},$$

where $\phi = \omega t$. Using (5.41) for analysis is straightforward as it is simply the integration the nonlinear equation over all the possible phases of the input:

$$n_p = \frac{2}{2\pi} \int_0^{2\pi} d\phi y[x(t)] \cos \phi, \quad (5.42)$$

$$n_q = \frac{2}{2\pi} \int_0^{2\pi} d\phi y[x(t)] \sin \phi. \quad (5.43)$$

The previous two equations can be combined with (5.41) in phasor form as

$$N_1 = \frac{2}{2\pi} \int_0^{2\pi} d\phi y[x(t)]e^{j\phi},$$

$$N_1(V, \theta) = \frac{2}{2\pi} \int_0^{2\pi} d\phi y[V \cos(\phi + \theta)]e^{j\phi}. \quad (5.44)$$

Integration is carried out over $\phi = \omega t$. Since there is no dependence on time, the phase, θ , is irrelevant but kept in the formula for continuity when additional sinusoids are added. The factor of 2 in the numerator is emphasized because there are two equal components at positive and negative frequency because $y(t)$ is implicitly assumed to be a real valued function. Equation (5.44) is mathematically simple and can easily be compared to Fourier series; the fundamental tone is being “picked” out of the signal $y[x(t)]$ and the result becomes a *function* of the input amplitude and phase. It is important to use cosine as the input because it contains the positive and negative frequency components; without the negative frequency components, there would be missing mixing products generated from the nonlinearity. A optimum approximator (or transfer function) can also be found in a similar way starting from (5.39) for a dc or bias component into the nonlinearity. In fact, since a bias and sinusoidal components are independent of each other, finding the dc output of the nonlinearity is merely a special case of (5.44):

$$N_1(V, \theta) = \frac{1}{2\pi} \int_0^{2\pi} d\phi y[V \cos(\phi + \theta)]. \quad (5.45)$$

Additionally, the n -th harmonic component at the output can be found easily

$$N_n(V, \theta) = \frac{2}{2\pi} \int_0^{2\pi} d\phi y[V \cos(\phi + \theta)]e^{jn\phi}. \quad (5.46)$$

5.3.3 DF FOR MULTI-TONE AND MULTI-DIMENSIONAL INPUTS

Now an additional sinusoid is added to the input. To perform the cross-correlation in (5.35), the sinusoids are considered as uncorrelated and independent by restricting the frequency to be non-commensurate. This essentially makes the phases of the two sinusoids random variables and decouples (5.35) into a auto-correlation. Equation can then be solved (5.39) and has the exact same form as (5.44) except with the input

as two sinusoids:

$$x(t) = V_1 \cos(\phi_1 + \theta_1) + V_2 \cos(\phi_2 + \theta_2) \quad (5.47)$$

$$N_{nm}(V_1, V_2, \theta_1, \theta_2) = \frac{2}{(2\pi)^2} \int_0^{2\pi} d\phi_1 \int_0^{2\pi} d\phi_2 y \left[V_1 \cos(\phi_1 + \theta_1) + V_2 \cos(\phi_2 + \theta_2) \right] e^{j(n\phi_1 + m\phi_2)} \quad (5.48)$$

Note that the integer numbers n and m in the exponential allow picking out any of the mixing products at the output between the two sinusoids. Since the frequencies are non-commensurate, the selected output frequencies will not overlap. Using sinusoidal inputs that are not correlated is not particularly useful in describing electrical circuits because the generated output harmonics inevitably will feedback to the nonlinear inputs. In fact, for most nonlinear transistor models, the drain node is one of the nonlinear control inputs (I_{ds} is a function of V_{ds}), meaning that there will always be harmonics on the “input” of the nonlinear element. If frequencies are used that are harmonics of one another, (5.39) becomes a set of coupled integral equations and (5.48) is no longer the optimum DF. This is easily seen as the harmonics at the input of a nonlinear element can mix in different ways to the same output frequency. For example, if the one of the input tones has frequency of ω and the other is 2ω , the fundamental DF can be computed as $N_{1,0}$ or $N_{-1,1}$ ($1 \cdot \omega + 0 \cdot 2\omega$ for the first and $-1 \cdot \omega + 1 \cdot 2\omega$ for the second). Both have the *same* output frequency of ω . This means that *one* DF equation is no longer enough; the sum of all the mixing terms that land on a particular frequency is needed to get the total nonlinear response to the input tones.

From here, it is easy to extrapolate (5.48) to K input sinusoids.

$$N_{\vec{k}}(\vec{V}, \vec{\theta}) = \frac{2}{(2\pi)^K} \int_0^{2\pi} d\phi_1 \cdots \int_0^{2\pi} d\phi_K y \left[V_0 + \sum_{i=1}^K V_i \cos(\phi_i + \theta_i) \right] \exp \left[j \left(\sum_{i=1}^K k_i \phi_i \right) \right] \quad (5.49)$$

K is the total number of input sinusoids, \vec{V} and $\vec{\theta}$ are vectors of the input sinusoid amplitudes and phases respectively, and \vec{k} is a vector denoting the order of the describing function (for example, $N_{1,0}$ would have a \vec{k} of $[1, 0]$). Equation (5.49) also adds in the dc bias of V_0 to the input of the nonlinear element. Even though (5.49) becomes a K dimensional integral, the interpretation is still very simple, the full frequency spectrum is fed to the nonlinear function ($y[x(t)]$) and the \vec{k} -th order output is selected with the exponential ($\exp(\dots)$). The equation can be further extended to multidimensional nonlinearities. For example most

nonlinear transistor models depend on the node voltages of V_{gs} and V_{ds} :

$$I_{ds}(t) = I_{ds}[V_{gs}(t), V_{ds}(t)], \quad (5.50)$$

where both $V_{gs}(t)$ and $V_{ds}(t)$ can be a sum of bias and sinusoids. Using the same form as (5.49), a multidimensional DF can be computed as

$$N_{\vec{k}}(\vec{V}_a, \vec{V}_b, \vec{\theta}_a, \vec{\theta}_b) = \frac{2}{(2\pi)^K} \int_0^{2\pi} d\phi_1 \cdots \int_0^{2\pi} d\phi_K y \left[V_{a0} + \sum_{i=1}^K V_{ai} \cos(\phi_{ai} + \theta_{ai}), \right. \\ \left. V_{b0} + \sum_{i=1}^K V_{bi} \cos(\phi_{bi} + \theta_{bi}) \right] \times \exp \left[j \left(\sum_{i=1}^K k_i \phi_i \right) \right] \quad (5.51)$$

Here there is an assumption that the frequency content at one input has the same frequencies as the other input (if there is no tone at a particular input, the corresponding V_i amplitude is set to zero). Again, to get the total response of a harmonic at the output of the nonlinearity, all the DF that sum to that particular frequency must be summed together. The benefit of analyzing a nonlinear method with (5.51) as opposed to harmonic balance, is that the all mixing products that land at the same frequency can be computed, giving information about how the nonlinearity combines input tones to give the total harmonic response at a frequency. In contrast, harmonic balance gives *only the total* harmonic response (there are ways to get around this in simulators by connecting K voltage sources with the correct phase and amplitude directly to the nonlinear element).

5.3.4 LIMITATIONS OF DESCRIBING FUNCTIONS

First, as mentioned before, the input form of the signal to the nonlinearity must be known in advance. The ability to know the input for use of DF either requires a suitable filtering network between the output and input of the nonlinearity or a very general input form that allows for a large number of input signals. Secondly, there is no adequate evaluation of the accuracy of the DF method [82]. Thirdly, as presented, no elements or components are modeled outside of nonlinear element. For Volterra series method of nonlinear circuit analysis, the entire circuit is modeled including reactances and load impedances. This gives information on how the nonlinear element interacts with the world; for example how load impedances can change the performance of the nonlinear element. With the simplified describing function analysis implemented here,

only information regarding the outputs of the nonlinearity from certain inputs can be inspected. How those inputs relate to the larger world are lost with this analysis. However, extensions of the basic theory outlined here to larger circuits, either by including the elements within the nonlinear equation or by nodal, analysis are possible. Finally, considering the form of the signal at the input must be known, a quote from [82] is particularly poignant:

... the analysis answers only the specific questions asked of it. If the designer does not ask about all important aspects of the behavior of a nonlinear system, describing function analysis will not disclose this behavior to him. [82]

The quote drives home the point that there may be multiple solutions to a particular formulation of a problem.

Since HB is used to find the inputs for DF analysis, the question arises: Are the variations of the output of the nonlinear element due to the inputs changing, or from the outputs of the nonlinear element? Harmonic balance is a simulator that gives the *steady state* of a circuit; a particular voltage does not *cause* a current (and vice versa) as all voltages and currents interact with each other. This means it is difficult, if not, impossible to determine primary causes because all voltages and currents are at an equilibrium state. However, the method of nonlinear currents from Volterra analysis or the basic iteration procedure of HB gives some insight. First, the top level harmonic balance simulation has excitation at a maximum of two frequencies, RF and LF. This means that any harmonics or mixing products are caused *by the nonlinear current source* (neglecting the nonlinear capacitors) and are manifested by the current output of the nonlinear element. These higher order currents cause higher order voltages which then feed back into the input of the nonlinear element. For DF, there is no requirement that higher order terms must be smaller than the fundamental terms but for the most part, this is true for nonlinear current sources:

- Feedback to the gate is restricted by a small C_{gd} capacitance and the source impedance is small enough that it can be neglected.
- The V_{ds} “gain” through the nonlinear current source is small and any feedback becomes smaller.
- A nonlinear current source with increasing feedback terms is unstable and may be unusable in a physical implementation.

- In addition to the above, Volterra series also requires that the magnitude of each successive term is smaller than the previous [78].

Since, as the mixing order increases the amplitude of the effects decrease, the primary cause of the nonlinear effects come from the lowest mixing order terms. Additionally, using DF one can separate out the effect of various mixing terms and determine that adding certain higher order terms increases the accuracy of the DF approximation with respect to the HB solution. All told, the variations of the output current are primarily due to the mixing effects of the nonlinear element rather than the voltage feedback to the input of the nonlinear element.

5.3.5 HISTORICAL PERSPECTIVE

It is interesting to note differences between DF and Volterra series not only from a mathematical point of view, but also from a historical perspective. The ground work for describing functions started with Van der Pol [86] with the first derivation of the DF by Krylov and Bogoliubov [87]. Major efforts in nonlinear analysis first started in the late 1930's and were focused on mechanical vibrations, acoustics, and electrical oscillators. The primary purpose of DF were as a tool for analysis of nonlinear feedback and control [88]. Of particular importance was the ability of DF to model systems with hysteresis, which Volterra and Wiener series cannot do. With the advent of World War 2, the application of nonlinear analysis focused on control systems for servomechanisms for accurate fire-control systems. Issues such as friction, backlash, and saturation in amplifiers were the focus of nonlinear control in the US and UK while controls for guided weapons were the area of focus in Germany [89]. After the war, there was still great interest mechanical systems and further independent derivations continued in Russia, England, France, Germany, and the United States [82].

At the same time Weiner had many works on time and frequency-response descriptions of a stochastic processes including analysis of nonlinear circuits [88,90]. Of particular interest is a quote from MacFarlane in a historical perspective of the decade before World War 2:

Two distinctive approaches to dynamical systems now began to develop which were associated with different ways of thinking about such systems and which, in view of their historical evolution, can be conveniently called the “mechanical engineers’ viewpoint” and the “communication engineers’

viewpoint,” respectively. A mechanical engineer using a differential equations approach modeled his system in terms of some real or abstract “mechanism” and wrote his system-describing equations down from a detailed study of the relevant physical mechanism. The communication engineer’s viewpoint, however, was quite different. It was natural for him to regard his various bits of apparatus in terms of “boxes” into which certain signals were injected and out of which emerged appropriate responses. [88]

DF was primarily used as a tool for mechanical system designs while Volterra series became the tool of choice for nonlinear electrical systems. A brief history of nonlinear control is covered in [89] and with a focus on German advances in [91]. MacFarlane gives a more detailed historical perspective of frequency response control analysis with a plethora of references [88]. An extensive list of citations covering origins of Volterra and Wiener series is in [76].

Mathematically, however, there may be additional incentive for pre- and post-war designers to use Weiner or the Volterra series instead of describing functions in the field of electrical engineering. First, is the assumption of filtering between the output of the nonlinear function and the input. It is reasonable to expect the use of DF were limited in the electrical realm considering the feedback often does not filter harmonics or mixing products. Leading to the second; the expanded inputs (harmonics + mixing products) at the input of the nonlinear element would require accurate multidimensional numerical integration for anything more complicated than a polynomial or exponential based nonlinearity. Conversely, Volterra and Weiner series can compute higher order effects from nonlinearities by series expansion and is useful even for very complicated circuits/nonlinearities. Atherton noted that:

In problems involving dual input describing function methods it was often found that the accuracy of the approach was not as good as that for the single input case due to the increased distortion components present at the nonlinearity input caused by cross modulation products. [89]

The increased complexity, either through numerical means or analytic means, most likely eliminated DF as a tool for electrical circuits early in the history of nonlinear control theory. Even as late as 1985, Schetzen stated that

... the describing function method normally is not useful in general nonlinear network analysis, [81]

without any further explanation or reference.

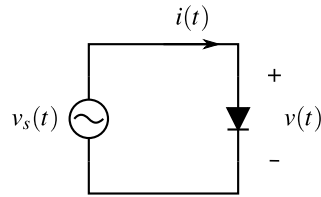


Figure 5.10: Circuit of a direct excitation shunt diode with a voltage source.

There is a single instance that the author is aware of that DF were used in recent literature in a electrical context. In the paper and in follow up papers using the same method, DF were used to accurately describe IMD behavior for a 2-tone input in power amplifiers [92].

5.4 DESCRIBING FUNCTIONS - SHUNT DIODE EXAMPLE

The same example as in Section 5.2 will be treated again using describing functions instead of the Volterra series. Two different methods are used to find the nonlinear total voltage and current through the diode. The first method uses direct excitation of the diode with a voltage source so the input voltages are known exactly (Fig. 5.10). The second method includes a $10\ \Omega$ resistor between the source and diode as in the Volterra example (Fig. 5.2). For the second case, the DF method cannot be used in the exact same way as the Volterra series in that it does not solve a nonlinear circuit directly. However, DF can still be used as a tool for analysis of a nonlinear element.

5.4.1 DIRECT EXCITATION

The voltage source shown in Fig. 5.10 is a two-tone voltage,

$$v_s(t) = V_0 + V_1 \cos(\omega_1 t) + V_2 \cos(\omega_2 t). \quad (5.52)$$

This is the total voltage excitation across the nonlinear element as all the other voltage components are shorted by the voltage source. Using (5.49) for $K = 2$:

$$i_{k_1, k_2}(V_0, V_1, V_2, \theta_1, \theta_2) = \frac{2}{(2\pi)^2} \int_0^{2\pi} d\phi_1 \int_0^{2\pi} d\phi_2 y[v_s(t)] \exp[j(k_1\phi_1 + k_2\phi_2)], \quad \text{for } \sum k_i \omega_i \neq 0 \quad (5.53)$$

$$i_{k_1, k_2}(V_0, V_1, V_2, \theta_1, \theta_2) = \frac{2}{(2\pi)^2} \int_0^{2\pi} d\phi_1 \int_0^{2\pi} d\phi_2 I_0(\exp[\alpha(V_0 + V_1 \cos(\phi_1 + \theta_1) + V_2 \cos(\phi_2 + \theta_2))] - 1) \\ \times \exp[j(k_1\phi_1 + k_2\phi_2)], \quad (5.54)$$

where $y[t]$ is the diode characteristic equation (5.24). The k_i terms represent the first tone and second tone mixing products. For example, the output current for the lower fundamental input tone would be $i_{1,0}$. The dc response is

$$i_{0,0}(V_0, V_1, V_2, \theta_1, \theta_2) = \frac{1}{(2\pi)^2} \int_0^{2\pi} d\phi_1 \int_0^{2\pi} d\phi_2 I_0(\exp[\alpha(V_0 + V_1 \cos(\phi_1 + \theta_1) + V_2 \cos(\phi_2 + \theta_2))] - 1), \quad (5.55)$$

because (5.54) is for the positive and negative frequencies (hence the factor of 2). Expanding the exponentials in (5.54) into trigonometric functions gives

$$i_{k_1, k_2}(V_0, V_1, V_2, \theta_1, \theta_2) = \frac{2}{(2\pi)^2} \int_0^{2\pi} d\phi_1 \int_0^{2\pi} d\phi_2 \left[-I_0 \cos[k_1\phi_1 + k_2\phi_2] \right. \\ - jI_0 \sin[k_1\phi_1 + k_2\phi_2] \\ + I_0 \exp(\alpha(V_0 + V_1 \cos(\phi_1 + \theta_1) + V_2 \cos(\phi_2 + \theta_2))) \cos[k_1\phi_1 + k_2\phi_2] \\ \left. + jI_0 \exp(\alpha(V_0 + V_1 \cos(\phi_1 + \theta_1) + V_2 \cos(\phi_2 + \theta_2))) \sin[k_1\phi_1 + k_2\phi_2] \right]. \quad (5.56)$$

With all k_i as integers, the first term becomes zero. The second term is zero because of the integration over an odd function. The third and fourth terms, however, are in the form of a modified Bessel function of the first kind:

$$I_n(z) = B_n(z) = \frac{1}{\pi} \int_0^\pi d\theta e^{z \cos \theta} \cos(n\theta). \quad (5.57)$$

Since I_n conflicts with the symbol for current, B_n is used for the denotation of the modified Bessel function.

The sum of angles in the cosines and sines in the exponent can be split apart to a product of the angles. The

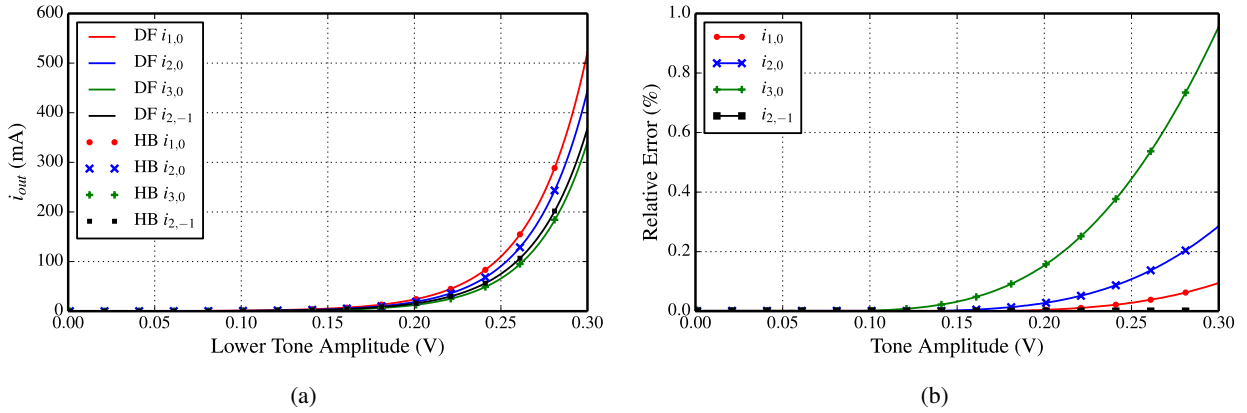


Figure 5.11: (a) Comparison between HB and DF for various harmonic components, i_{k_1, k_2} . A dc voltage of $V_{dc} = 0.3 V$ is used. (b) Error as compared to harmonic balance simulation.

final result of the integration of (5.54) is

$$i_{k_1, k_2}(V_0, V_1, V_2, \theta_1, \theta_2) = 2I_0 e^{\alpha V_0} e^{-j(k_1 \theta_1 + k_2 \theta_2)} B_{k_1}(\alpha V_1) B_{k_2}(\alpha V_2), \quad (5.58)$$

and the dc term is

$$i_{0,0}(V_0, V_1, V_2, \theta_1, \theta_2) = I_0 (e^{\alpha V_0} B_0(\alpha V_1) B_0(\alpha V_2) - 1). \quad (5.59)$$

The dc term is equivalent to the characteristic equation for the diode if the sinusoidal tones, V_1 and V_2 , are equal to zero. Equations (5.58) and (5.59) are startlingly simple equations considering that they can compute the current for *any* mixing product generated by the nonlinear element with an arbitrary amplitude and phase of the two voltage source tones. A harmonic balance simulation was performed on the circuit of Fig. 5.10 with a dc voltage of $V_{dc} = 0.3 V$ and the current of various harmonic components measured (all voltage components except the fundamental tones are shorted by the voltage source). The harmonic current result of the HB and DF from (5.58) are shown in Fig. 5.11a. The improvement from the Volterra series in Figs. 5.6b and 5.7b is drastic, the total error being under 1% for the DF case as compared to >40% for the Volterra series. The error for the lower intermodulation mixing product, $i_{2,-1}$, is nearly zero for the entire swept voltage range.

Although the results are nearly exact for known input voltage components, it is instructive to return to the original example as in Fig. 5.2 with the resistor in series with the diode and determine how using DF for inputs that may not be exact will affect the accuracy.

5.4.2 INDIRECT EXCITATION

5.4.2A 1 TONE EXCITATION

Initially, a single tone excitation will be used for the source. In contrast to the previous section, the higher order voltages across the diode will not longer be shorted as there is a resistor in series with the nonlinear element (Fig. 5.2). This complicates the assumption that there are only 2 tones into the nonlinearity; there will be harmonics in addition to the fundamental. The number of input tones now equals the number of mixing products created by the nonlinearity, which is infinite. However, for practical purposes, after a certain number of harmonics (or order mixing product), the amplitude will have a negligible effect on the total voltage or current at the diode.

Expanding (5.58) for more than two frequency components across the nonlinearity happens to be very simple; adding an additional tone only multiplies by another modified Bessel function. For an arbitrary number of K tones for $v_s(t)$, (5.58) can be rewritten as

$$i_{\vec{k}}(\vec{v}, \vec{\theta}) = 2I_0 e^{\alpha v_0} \prod_{i=1}^K B_{k_i}(\alpha v_i) e^{-j k_i \theta_i}. \quad (5.60)$$

The vectors denote the properties for each tone: \vec{k} is the order of the tone, \vec{V} is the amplitude of each tone at the nonlinearity input, and $\vec{\theta}$ is the phase of each tone. Initially, K will be limited to 2 for the fundamental and first harmonic tone which will be denoted by v_1 and v_2 respectively and the frequencies are given by $k_i \omega_i = [1, 2]$ GHz. From the circuit diagram, the voltage across the diode at dc, the fundamental, and first harmonic can be written as

$$\begin{aligned} v_0 &= V_{s,dc} - R i_{0,0} = V_{s,dc} - R \left(I_0 (e^{\alpha v_0} B_0(\alpha v_1) B_0(\alpha v_2) - 1) \right), \\ v_1 &= V_{s,1} - R i_{1,0} = V_{s,1} - R \left(2I_0 e^{\alpha v_0} e^{-j\theta_1} B_1(\alpha v_1) B_0(\alpha v_2) \right), \\ v_2 &= V_{s,2} - R i_{0,1} = V_{s,2} - R \left(2I_0 e^{\alpha v_0} e^{-j\theta_2} B_0(\alpha v_1) B_1(\alpha v_2) \right), \end{aligned} \quad (5.61)$$

which represents a system of equations of three variables. This set of equations is very difficult to solve because of the modified Bessel functions. Additionally, each voltage at a particular frequency depends on the voltage amplitudes at all the other frequencies; there is no easy variable to solve for first. Instead of solving

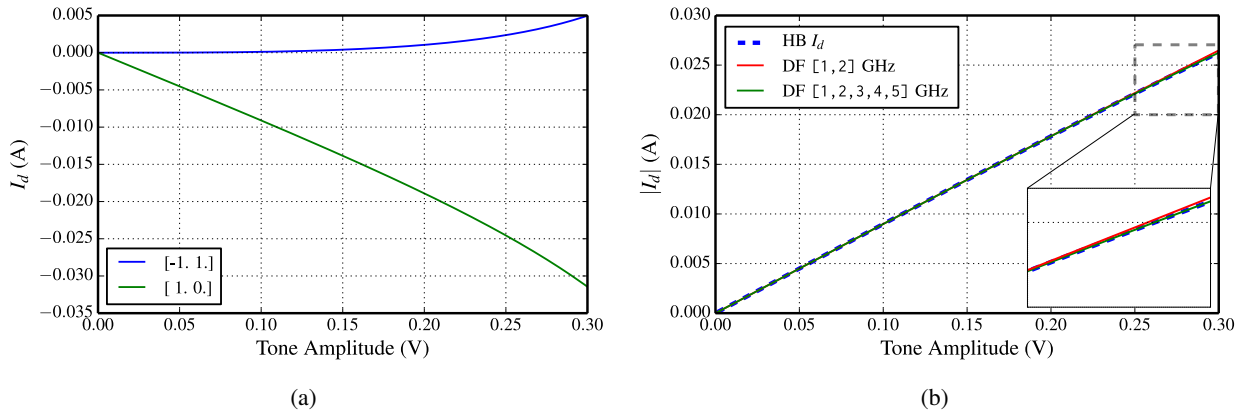


Figure 5.12: (a) Complex current mixing product components of DF with tones $[1, 2]$ GHz. (b) Comparison between HB and total DF response for a single tone excitation at 1 GHz of a shunt diode and series resistor. A dc voltage of $V_{dc} = 0.8$ V is used.

(5.61) directly for the voltages at the nonlinearity (extremely complicated), a harmonic balance simulation result is used to find the input voltages. This may seem like cheating. However, DF just as Volterra series, is not meant as a replacement for HB; DF is a nonlinear analysis tool to gain insight to the mixing effects of the nonlinearity. The disadvantage is that any loading effects on the diode cannot be solved for directly with this formulation. The numerical voltages for the fundamental and harmonic components are exported from a commercial HB solver and used as the amplitudes and phases for \vec{v} and $\vec{\theta}$ respectively.

The use of (5.60) is slightly different from (5.58) in that a mixing product landing on the desired frequency can be achieved multiple ways with \vec{k} . For the fundamental tone, \vec{k} can be either $[1, 0]$ (fundamental only) or $[-1, 1]$ (negative frequency component of fundamental and 2nd harmonic mixing, $\sum k_i \omega_i = -1 \cdot 1 + 1 \cdot 2 = 2$ GHz). All mixing components need to be summed to give the total nonlinear response. Code to find the mixing orders for a particular frequency is in Listing E.3.

The diode is simulated with the $V_{dc} = 0.8$ V bias point, putting the diode in a highly nonlinear regime. Fig. 5.12a shows the individual current components for each of the tones. The mixing tone, $[-1, 1]$, has an opposite effect on the fundamental only tone which decreases the total current as the amplitude increases. The total current of the DF computation in Fig. 5.12b is very close to the HB result even with only using 2 tones from the original HB simulation. With 5 tones (fundamental plus 4 harmonics), the agreement is nearly perfect.

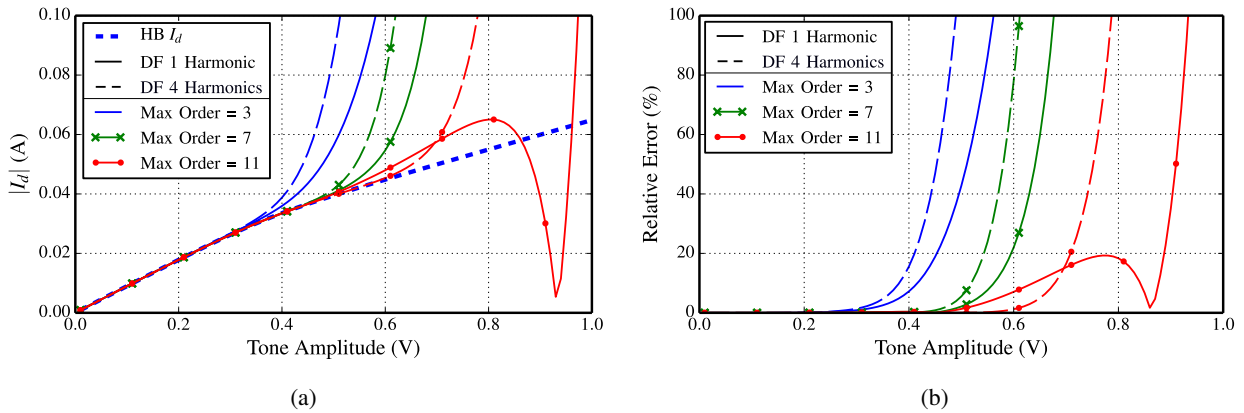


Figure 5.13: (a) HB and total DF response for various number of tones and mixing order across a shunt diode and series resistor. (b) Relative error between HB simulation and DF method.

While the DF method is a quasi-linearization and fits nonlinearities better, increasing the source tone amplitude shows limitations for very high nonlinearities. Fig. 5.13a shows the current compared to the HB simulation and how it converges with increasing number of harmonic tones and increasing maximum mixing orders. For the same number of input tones (solid lines), a higher maximum mixing order models the nonlinearity better. Conversely, a higher number of input tones (dashed lines) does not necessarily model nonlinearity better compared to a lower number of input tones unless the maximum order is allowed to increase as well. The relative error is shown in Fig. 5.13b. This highlights the dependence of the DF method on the knowledge of the type and number of inputs to the nonlinearity. Increasing the accuracy of the modeling increases the complexity of the integration (unless it can be solved analytically as the diode nonlinearity can); the number of tones has the largest effect on the time of integration for DF. Note that the relative error for the Volterra series for a 1-tone excitation is 11% at 0.3 V input amplitude compared to the <2% for the worst case DF result.

5.4.2B 2 TONE EXCITATION

Taking the method and lessons from the previous section, describing functions are used for 2-tone analysis with the shunt diode. Again, HB is used to give the inputs for the DF method. With 2-tones, there are numerous input tones to the nonlinearity. To give good accuracy for the DF method the HB simulation

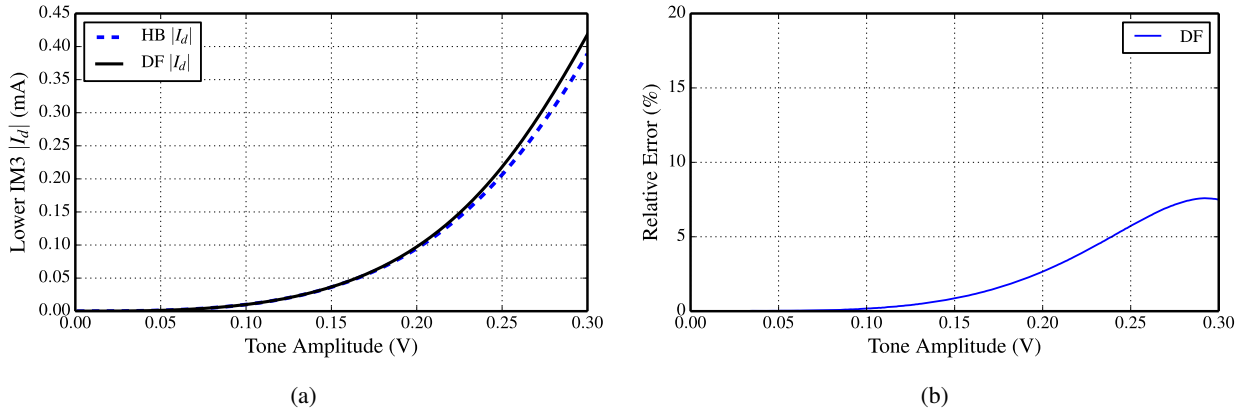


Figure 5.14: (a) HB and total DF response for a 2-tone excitation at 1 GHz of a shunt diode. A dc voltage of $V_{dc} = 0.8$ V is used. (b) Relative error between HB and DF.

was performed with 5 harmonics for each tone (1 GHz and 1.01 GHz) and a maximum mixing order of 11. Additionally, the frequency components at the nonlinearity was filtered in HB to reduce the number of relevant tones. The cutoff frequency was 1.5 GHz for the filter. For the DF analysis only a mixing order of 7 was used with tones:

$$\vec{f} = [0.01, 0.02, 0.04, 0.97, 0.99, 1, 1.01, 1.02, 1.04] \text{ GHz.} \quad (5.62)$$

These tones were chosen based on the highest harmonic magnitude for an input tone case of $V_s = 0.275$ V. Fig. 5.14 shows the total current and relative error as compared to the HB simulation for the lower 3rd order intermodulation product (IM3) at 0.99 GHz. With a maximum mixing order of 7, there are 1278 total mixing products to create 0.99 GHz from the tones in (5.62) resulting in 1278 evaluations of (5.60). While numerically intensive, the result has significantly less error of 8% than in the Volterra case of >70% at an input tone voltage amplitude of 0.3 V.

This diode example is a worst case example for DF use because the control (voltage) and output (current) are at the same node causing any nonlinear output to feed directly back into the input greatly increasing the number of tones at the input and maximum mixing order proper analysis. Even for a stressing case for the DF method, the accuracy under large-signal is considerably better than the Volterra series' accuracy. Additionally, individual mixing tones can be separated out and investigated for how important it is relative to the total result.

5.5 DF ANALYSIS OF ANGELOV FET MODEL

Now that we have a tool for the analysis of a nonlinear element, the next step is to look at the interaction of how a low frequency (LF) and RF signal interact in a nonlinear FET model. Some features of the LF impedance response can be easily explained through the mixing products of the nonlinear element. Practical DF implementation details need to be covered first however.

The first issue that arises from calculating (5.51) is that the input voltage vector (amplitude and phase for all spectral components) is unknown. The Angelov compact model, discussed in detail in Appendix C and shown in Fig. C.1, contains resistive, reactive, and nonlinear elements. This means that the solution of the circuit involves coupled, nonlinear, and frequency dependent equations. Harmonic balance (HB) is much more suited to analysis of large scale nonlinear circuits. The describing functions developed here are not meant to replace HB; it is meant to be used as a tool for analyzing how a nonlinear element behaves under certain operating conditions. In this light, a commercial HB simulator is used to simulate the FET model and the control node voltages are exported and used as inputs for the DF method. By this method, not only can the nonlinearity effects be calculated, but the total component results can be compared to the HB total component result. Parameter sweeps can also be easily performed in the HB simulator and the nonlinearity effect over an independent parameter calculated.

Fig. 5.15a and 5.15b show a sample integration surface for the Angelov current source (equation (C.1) in Appendix C) over two parameters (input sinusoids) with frequencies $\vec{f} = [0.01, 10]$ GHz and an order of $\vec{k} = [-1, 1]$. The surface is the integrand of (5.51), which in this case, is a function of the three controlling voltages, V_{gii} , V_{dsi} , and V_{bg} :

$$A(\dots) = I_{ds}(\vec{V}_{gii}, \vec{V}_{dsi}, \vec{V}_{bg}) \exp [j(-\phi_1 + \phi_2)] \quad (5.63)$$

where

$$\vec{V}_{gii} = V_{gii,0} + V_{gii,1} \cos(\phi_1 + \theta_{gii,1}) + V_{gii,2} \cos(\phi_2 + \theta_{gii,2}), \quad (5.64)$$

$$\vec{V}_{dsi} = V_{dsi,0} + V_{dsi,1} \cos(\phi_1 + \theta_{dsi,1}) + V_{dsi,2} \cos(\phi_2 + \theta_{dsi,2}),$$

$$\vec{V}_{bg} = V_{bg,0} + V_{bg,1} \cos(\phi_1 + \theta_{bg,1}) + V_{bg,2} \cos(\phi_2 + \theta_{bg,2}).$$

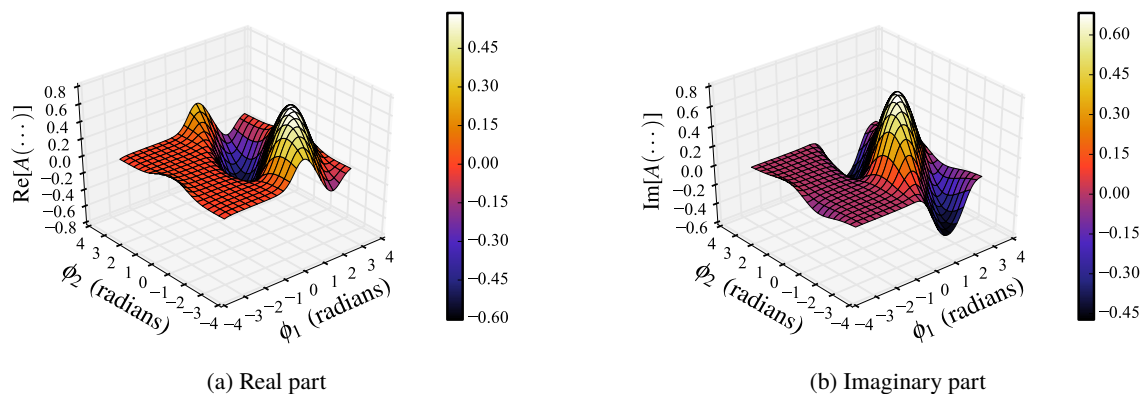


Figure 5.15: Evaluation of the integrand in (5.51) where the function $y[t]$ is the Angelov current source equation (C.1) and $\vec{x}(t)$ is three input waveforms for V_{gs} , V_{ds} , and V_{bg} each with bias and two sinusoids which include positive and negative frequencies. Each frequency phase, ϕ_i , is integrated over all possible values: $-\pi$ to π (equivalent from going 0 to 2π).

Table 5.3: Angelov control voltage coefficients from an HB simulation for an input power of 26 dBm.

	$V_{-,0}$	$V_{-,1}$	$\theta_{-,1}$	$V_{-,2}$	$\theta_{-,2}$
$V_{gii,i}$	-2.501	2.314	-1.434	0.332	0.208
$V_{dsi,i}$	20	14.373	1.580	0.932	-0.048
$V_{bgi,i}$	0	0.586	1.581	0.038	-0.048

The coefficients were extracted for an input power of 26 dBm and listed in Table 5.3. The surface is smooth and finite. However, there can be many zero crossings at higher orders and higher input amplitudes and other portions are nearly flat which may significantly increase time for numerical integration over the surface. The next step would be to integrate over the surface to find the amplitude to the particular mixing product (for $\vec{f} = [0.01, 10]$ GHz and an order of $\vec{k} = [-1, 1]$ the output frequency would be 9.99 GHz):

$$N_{-1,1}(\dots) = \frac{2}{(2\pi)^2} \int_{-\pi}^{\pi} d\phi_1 \int_{-\pi}^{\pi} d\phi_2 A(\dots). \quad (5.65)$$

Python code was implemented to find the results of the describing functions, $N_{\vec{k}}(\dots)$. Integration was performed with, `Cubature`, a multi-dimensional integration library.¹ The algorithms in the library originally come from [93,94]. Adding additional dimensions (more input sinusoids) increases computation time considerably.

¹ C code for the library is at <http://ab-initio.mit.edu/wiki/index.php/Cubature>. A Python wrapper can be found at <https://github.com/saullocaastro/cubature>.

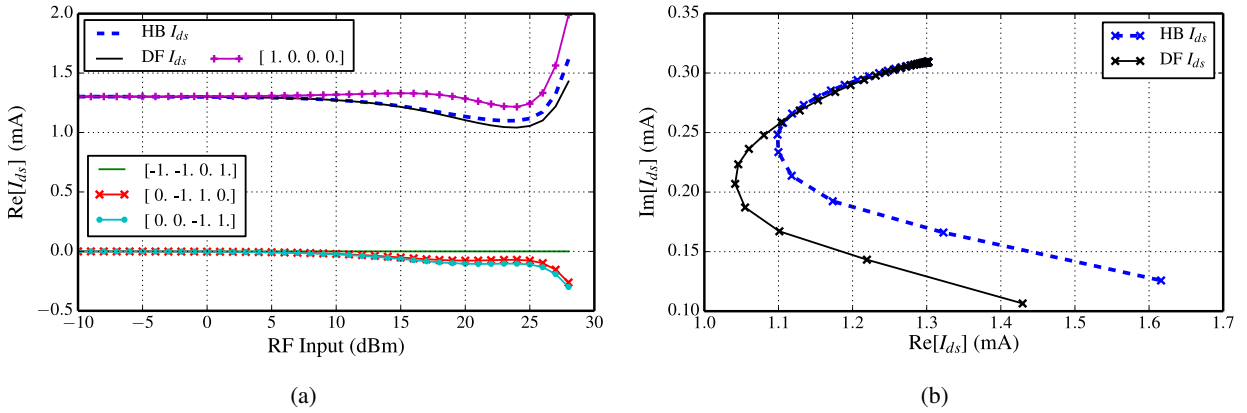


Figure 5.16: (a) Describing function result for Angelov FET with 10 GHz input on gate, and 10 MHz input on drain. The total DF result (sum of the individual mixing products) tracks very closely to the HB result (dotted blue line). (b) Polar plot of the total DF and HB result.

5.5.1 DF DRAIN IMPEDANCE OVER SWEPT RF POWER

One particular feature of the LF variation in impedance is over RF input power. Fig. 3.9b shows this variation for different V_d . The characteristic bump in impedance can be shown to exist in a standard harmonic balance simulator, however, an intuitive description would be useful to see if this behavior could be modified. The simulation was performed with an RF input source on the gate of the nonlinear model and a low frequency source on the drain of the model. Five harmonics plus mixing products (up to order 5) of each tone were simulated in ADS. The gate, drain, and back-gate voltages were exported and used with the describing function code. To shorten the time for integration of the DF, a small selection of tones were used (pick based on relevance to the total solution): $[0, 10e6, 9.99e9, 10e9, 10.01e9]$ Hz. The drain impedance is calculated as:

$$Z_d = \frac{V_d}{I_d}. \quad (5.66)$$

Fig. 5.16a shows the results of the DF output for the various mixing products for the drain current at 10 MHz compared to the total current as found by HB (dotted line). The numbers in the brackets correspond to the frequency mixing products as given by the vector of frequencies in the previous paragraph. For example, the primary (and majority of the current) component comes from the 10 MHz signal injected at the drain (legend key $[1, 0, 0, 0]$). The second order mixing products which involve 10 GHz and one of the IM3 side

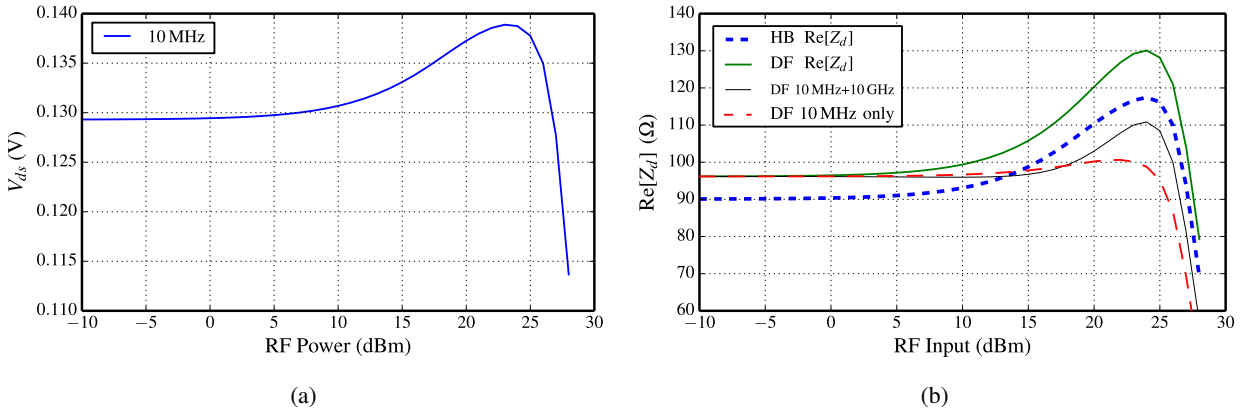


Figure 5.17: (a) HB voltage used to calculate the (b) drain impedance at 10 MHz. The comparison between HB and (total) DF Z_d is close both having very similar trends. If only the primary LF tone is used, the impedance does not have the large characteristic bump in impedance.

tones, have a smaller effect but are increasingly significant at higher RF input powers. The sum of the DF gives the black line in the plot which tracks closely to the HB result. Fig. 5.16b shows the total I_{ds} current in the complex plane. At lower RF input powers DF are almost identical to the HB result. The voltage from HB (used for calculating the LF impedance for both the DF and HB) is shown in Fig. 5.17a. However, if one just uses the primary 10 MHz tone to calculate Z_d , the result is very flat and does not exhibit the peaking characteristic as shown by the red dashed line in Fig. 5.17b. Adding the RF tone in addition to the 10 MHz tone (black line) gives a self-biasing effect when the transistor starts to compress, but the impedance bump is less than the HB result. Whereas, the full DF result tracks closely to the HB result. The results are not identical because of a small numerical offset of the DF compared to the HB result (in Fig. 5.16a the current between the results are almost identical, however, with the very small voltage, the impedance difference becomes $\approx 6 \Omega$).

The resulting conclusion that can be drawn is that the RF IMD products mixing back down to LF provide a non-trivial decrease in current at the onset of saturation, thereby, increasing the drain node impedance. This effect can be tested by modifying one of the RF adjacent tones and finding how it affects the LF impedance.

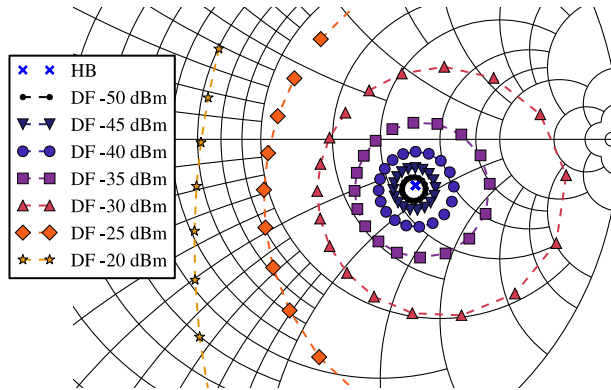


Figure 5.18: LF impedance (Z_d) of a FET when excited with 10 GHz and a 9.99 GHz tone is modified to have a set power (symbols) and phase (dotted line connecting symbols of certain type).

5.5.2 DF DRAIN IMPEDANCE WITH 2ND RF TONE

The same exported node voltages are used for the input power of 24 dBm, only modifying the 9.99 GHz tone at the gate node to have a set power and phase. The results are shown in Fig. 5.18. The HB result, denoted by the 'x', is the nominal impedance without modifying the 9.99 GHz tone. By modifying this tone to have a given peak-to-peak voltage and swept phase, the impedance of the FET at 10 MHz can be modified to be any impedance desired. As the power of the secondary tone increases, the gamma of the drain node may move outside the Smith chart meaning that the device is *generating* power at LF. Consequently, if a device has a wideband RF input signal, the drain node will generate a similar signal at baseband depending on the phase of the RF signal and the bias point of the device. Harmonic balance simulations give very similar results.

5.5.3 MEASURED DRAIN IMPEDANCE WITH 2ND RF TONE

While DF and HB indicate an ability to modify the drain impedance at a particular frequency with a secondary RF tone, it is straight forward to test this phenomena. The measurement bench in Chapter 2 was used with an additional RF source and analog phase shifter to generate the second RF tone at 10.68 GHz with desired phase. The primary RF source at 10.7 GHz was set for an input power of 15 dBm. The low frequency impedance was measured at 20 MHz. Results of the measurement are shown in Fig. 5.19. The impedance with no power on the second RF tone is approximately 300 Ω . As the secondary tone power is increased and the phase swept, the same impedance modification effect is seen as in the simulated case: as the LF

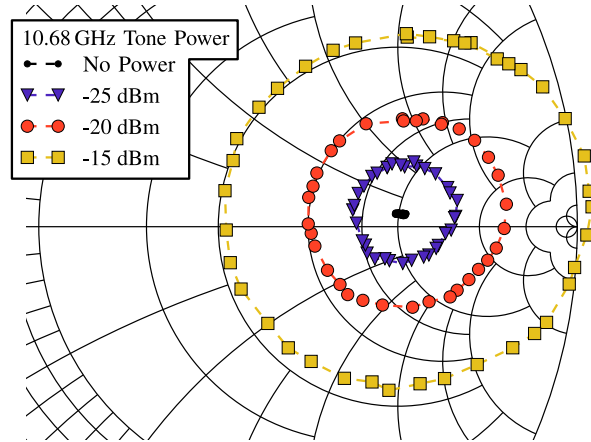


Figure 5.19: Measured Z_d with a RF source of 10.7 GHz and a secondary RF source at 10.68 GHz with power given in the legend. The same LF impedance modification effect is seen as in DF and HB simulations.

impedance is centered around the 0 W input power case with angle given by the phase and radius by the power of the RF tone. Note that the input powers for the secondary tone cannot be compared between the simulated and measured case: the simulated case sets the power at the internal gate control node assuming voltage across a 50Ω load while the measured case is the available power at the input of the FET.

One may note that the computed impedance over swept phase as shown by DF do not have the same shape as the measurement: co-centric circles centered on the initial impedance point. This is because the HB control voltages for 24 dBm were used, only modifying the 9.99 GHz tone, instead of re-simulating in HB for each gate input power: all the remaining elements of the Angelov model were ignored when directly modifying the 9.99 GHz tone. If the control voltages for HB were used for each input power and phase, the shape would be almost identical to the measured case. However, this example provides demonstration of the utility of DF as an analysis tool for nonlinear elements.

This “active” impedance impedance modification can be used directly with the measured LF impedance to predict the LF output waveform for wideband RF signals. Unfortunately, with the current setup, the relative phase of the RF sources could not be measured which would be required to give the full picture of RF \rightarrow LF mixing.

5.6 CONCLUSION

The simplicity of the DF method is apparent when compared to Volterra series for describing the mixing product interactions between input tones. In addition, DF can describe large-signal phenomena without any additional complexity in the formulation or formula itself. This chapter detailed a basic Volterra series formulation of a diode nonlinearity, with results compared to harmonic balance. Describing functions were introduced and adapted to nonlinear electrical elements. Extensions to phasor form and multiple inputs into a multidimensional nonlinearity were also detailed. DF were used to investigate the mixing components of a current source in an Angelov nonlinear FET model. In particular, the LF drain impedance behavior as a function of RF input power was analyzed. Second order mixing products mixing down the the LF tone were be shown to have a non-negligible effect on the low frequency drain impedance. Finally, modification of the LF drain impedance was demonstrated with DF by modifying the lower intermodulation mixing product showing that the LF impedance could be “loadpulled” to any impedance desired. A measurement was performed to confirm the “loadpulling” effect with two RF input tones to the gate of the device.

CHAPTER 6

CONCLUSION AND FUTURE WORK

CONTENTS

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6.1 SUMMARY AND CONTRIBUTIONS

This thesis was focused on the characterization of FET transistors and amplifiers under supply modulation. It is a step toward a cohesive model for design and simulation of supply modulated transmitters.

- A measurement bench was developed for simultaneous measurement of RF and low frequency performance of a FET or power amplifier. The device under test was operated in large-signal in X-band to characterize the static and dynamic supply port impedances from 1 to 500MHz. The setup is versatile and measurement data on bare die transistors for modeling and design, power amplifiers for co-design with a supply modulator, and transmitters to inspect interactions between the PA and SM was presented. Calibration was covered for the most complex case for absolute voltage and current and

simpler bench setups involve only parts of what was presented here. Addition of a vector measurement component (samplers or NVNA/LSNA) at RF is preferable in the future for modeling of the RF→LF and LF→RF mixing transfer functions. This part of the thesis is covered in Chapter 2 and published in [95,96].

- Measurements of FET devices and power amplifiers were presented to corroborate the DF theory analysis and provide meaningful results for modifying current nonlinear models. The measurements could also be used as a debugging tool for improving transmitter performance because of misaligned switching times and/or correcting PA impedances that a supply modulator might not be designed to handle. This is covered in Chapters 3 and 4 and published in [95,96]
- Design of MMIC power amplifiers specifically for supply modulation. There are a number of aspects related to the bias network that should be considered for wide bandwidth supply modulation. This is covered later in the conclusion in Section 6.3 and published in [72].
- Describing functions (DF) for multiple-input and multi-dimensional nonlinear elements were developed as an analysis tool to explore the interaction between the LF and RF regimes of a transistor current source. The 2nd order mixing product from RF→LF was shown to be exploitable to modify the low frequency impedance seen by a supply modulator. Additionally, the 2nd order mixing product could be used as a basis for a simple model usable in a harmonic balance (HB) simulator. The DF approach is not only a tool for supply modulation but is a general theory that can be used for any nonlinear element or system. This part of the thesis is covered in Chapter 5 and a paper is submitted to IMS 2016 with the title “Multi-Frequency Large-Signal Analysis Using Describing Functions”.

6.2 DISCUSSION

6.2.1 MEASUREMENT BENCH AND FET MEASUREMENTS

The multi-frequency measurement bench from Chapter 2 with large-signal capability at low frequency (LF) allows the measurement of individual GaN FET transistors. These measurements would be very useful

for creating a model for supply modulation. Some initial efforts for a comprehensive model are detailed in [34, 48]. The low frequency ability of the measurement setup can be applied directly to modeling low frequency phenomena including trapping effects in the small-signal regime [31], and the nonlinear regime [34, 37, 38, 97]. The goal was to quantify the dynamic supply-terminal impedance towards the understanding of the interaction of a PA with a wide bandwidth (>10 MHz) supply modulator. If one considers the impedance contours in Fig. 3.13, the impedance seen by a supply modulator is roughly constant when the transistor is under RF compression. If a transmitter is operated in this region, the output power dynamic range must come entirely from the variation of voltage on the drain (also known as EER) and allows high-efficiency PA operating modes (class-E, F, F^{-1}). If a transmitter trajectory includes a combination of RF and LF input power (partial drive modulation), the impedance variation can be minimized by operating the RF transistor in class-A. However, the impedance becomes widely variable over frequency and drain bias under saturation as shown in Fig. 3.11 and 3.10. For the device in this paper, a $50\ \Omega$ variation is observed for a 100 mA/mm bias point compared to $>200\ \Omega$ for partial drive modulation. However, partial drive modulation limits the maximum efficiency of the PA to 50% and system to $<50\%$ depending on the efficiency of the supply modulator.

6.2.1A NONLINEAR MODEL IMPROVEMENTS FOR SUPPLY MODULATION

Traditionally, nonlinear models are fit using I - V curves and S-parameters [98–104] and more recently authors have been using time domain waveforms for fitting [34, 97, 105, 106]. However, very few authors have investigated modeling for nonlinear devices under multiple excitations [37, 97]. Current nonlinear models have not focused on modeling the simultaneous excitation at high and low frequencies necessary for supply modulation.

Most nonlinear device models are only measured and extracted at RF frequencies. Because of this, directly comparing simulation results to measurements is not constructive as the comparison would purely be on a case-by-case basis depending on how it was extracted for RF frequencies. Instead general trends will be commented on for areas of improvement.

Fig. 6.1 shows a comparison between measurement and simulation of the complex impedance of the

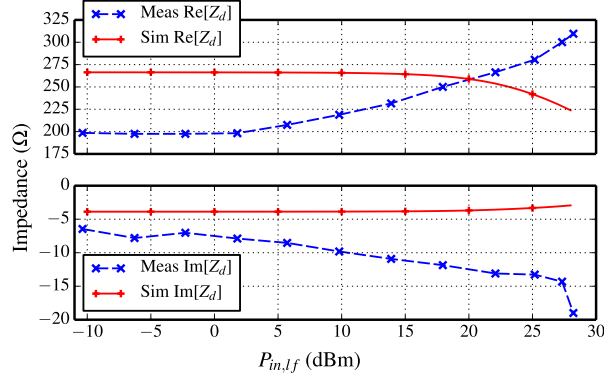


Figure 6.1: The nonlinear device model is not valid under dynamic operation at low-frequencies as expected. Comparison between simulated and measured low frequency impedance at 10 MHz for the $10 \times 90 \mu\text{m}$ device at $V_d = 20 \text{ V}$ and $I_{dq} = 100 \text{ mA/mm}$.

drain port over swept baseband input power (or low frequency input power, P_{lf}) at 10 MHz. The model is Angelov-based and was extracted with 10 GHz loadpull (original application frequency) at multiple drain voltages with a bias points of 10 mA/mm and 100 mA/mm. The device was measured at 100 mA/mm with a 20 V drain with 14 dBm input RF power. The simulation was performed under the same parameters as the measurement. The simulation result has roughly the same impedance at low input powers, but as the low frequency input power increases, the trend is opposite of measurement: the low frequency real part of the impedance decreases by only about 50Ω starting at 15 dBm input while the measurement starts an increasing at 2 dBm input with a total increase of 110Ω . Another example is shown in Fig. 6 of [96], simulation for one of the MMICs shows non-physical behavior near compression, although RF simulations with the same model accurately predict carrier-frequency behavior. These examples highlight the need to characterized the device for supply modulation purposes under high multi-frequency drive.

6.2.2 PA/MODULATOR MEASUREMENTS

For the resonant pulse transmitter example in Section 4.2, it is clear the modulator cannot handle the load variation of the PA caused by RF input power changes with a variable amplitude Gaussian pulse. Instead, the drain supply voltage on the modulator must be changed to minimize the load variation and give variable output powers. This complicates the system implementation of such a modulator requiring another variable voltage supply, albeit one that can be considerably slower than the resonant pulse modulator. In short, for

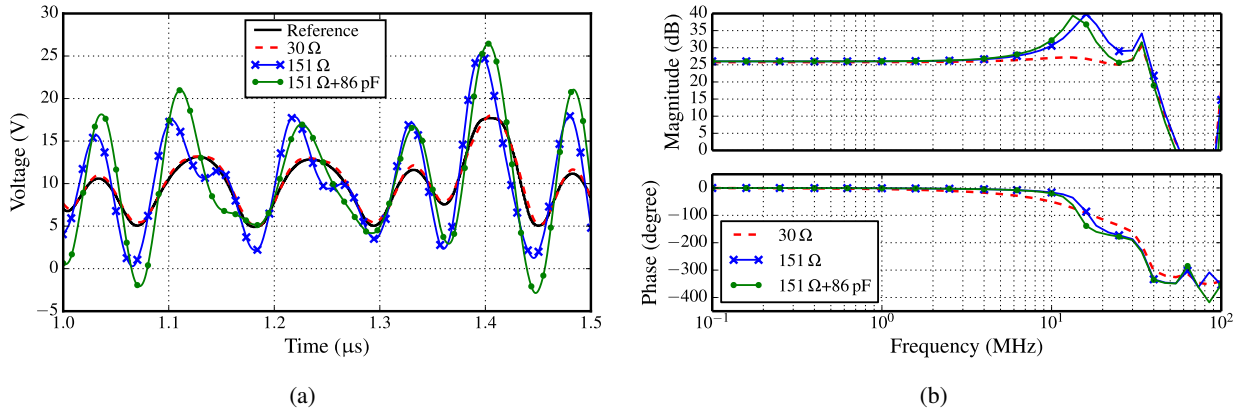


Figure 6.2: (a) Waveform and (b) Bode plot simulation of Buck converter with 4th-order output filter designed for a $30\ \Omega$ purely real load. The converter tracks the envelope of a 20 MHz LTE waveform. The envelope is accurately tracked for the designed load of $30\ \Omega$. However, with the measured load of the PA in Section 4.1 (at $V_d = 15\ \text{V}$ and 23.8 dBm RF input power), the higher resistance and capacitance cause distortion and significant drain voltage overshoot.

this example, the modulator should be designed to supply power under a higher resistive load or the power amplifier design should be changed to provide a more uniform impedance over RF/LF input powers.

Communication transmitters commonly use a switching dc-dc converter assisted with a linear amplifier [22]. A switching dc-dc converter creates a large amount of switching noise at baseband and needs a low-pass LC filter to block switching noise from the modulator [107] and some authors have expanded the modulator output reactances to higher order filters [108]. However, even with a filter, the modulator load is determined by the transistor dynamic impedance. As an example, a Buck converter was simulated in Simulink by MathWorks[©] with a 4th-order output filter optimized for a $30\ \Omega$ load [29]. The output voltage waveform for a 20 MHz LTE envelope is shown in Fig. 6.2a. There is good tracking with the static $30\ \Omega$ load. However, with a baseband load extracted from Section 4.1 ($R = 151\ \Omega$ and $C = 86\ \text{pF}$ from Fig. 4.3) at a static V_d and RF input power, the waveform becomes greatly distorted with large voltage swings which may cause damage to the amplifier. The large resistance change causes the bulk of the distortion. Fig. 6.2b shows the frequency transfer function for the converter with various loads. The amplitude shows the need for linearization because of the peaking within the supply modulation bandwidth. This simulation does not include the variation in baseband impedance due to drain voltage which would create even more distortion. With the potential variation in baseband impedance, the buck converter would no longer be at an optimal load

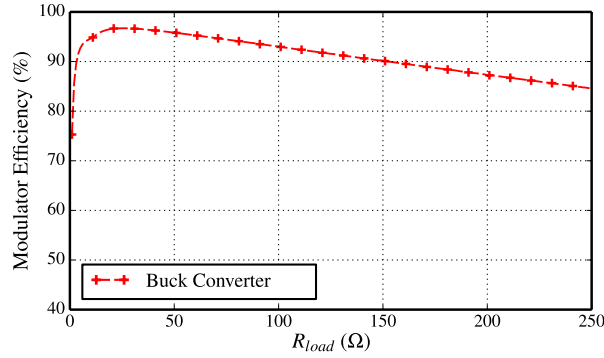


Figure 6.3: Simulated efficiency of the buck converter versus a static resistive load.

(Fig. 6.3), decreasing the efficiency of the transmitter system. This further highlights the need to consider the variation in baseband impedance of a transistor or power amplifier for different RF input powers and bias points.

The measurements presented in this thesis highlight the need to understand the RF transistor impedances at baseband over all operating conditions for optimal design of the supply modulator. The baseband impedance can vary dramatically over input powers and bias conditions. Other work has been performed that indicate other solutions to the switcher filter including, reduction of the bandwidth of the switcher which relaxes requirements on the filter [109] or a different supply modulation technique by way of discrete level modulation [30].

6.3 MMIC PA DESIGN FOR SUPPLY MODULATION

As opposed to taking an off-the-shelf PA to characterize for supply modulation a number of monolithic microwave integrated chip (MMIC) designs were fabricated over a 4 year period specifically for drain supply modulation under the Microscale Power Conversion (MPC) DARPA (Defense Advanced Research Projects Agency) project. A number of MMICs are detailed in [72]. The goals of the DARPA project were 10 W of power at 10 GHz with 500 MHz of instantaneous RF bandwidth at 6 dB PAR and a total average composite efficiency (CPAE) of 75%. To achieve the very high efficiency with the 6 dB PAR requirement, the supply modulation transmitter architecture was used to increase the efficiency at backed-off powers. The CPAE is

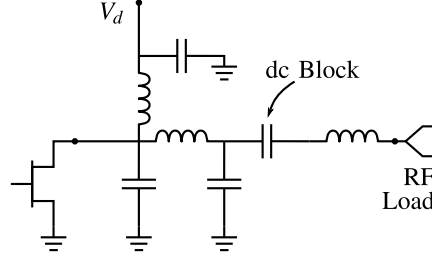


Figure 6.4: Lumped element equivalent circuit for an output matching network. The dc blocking capacitor is nominally large to provide low loss at RF frequencies.

defined as

$$CPAE = \frac{\int_{V_{min}}^{V_{max}} dV PDF(V)[P_{RF,out}(V) - P_{RF,in}(V)]}{\int_{V_{min}}^{V_{max}} dV PDF(V)[P_{dc,PA}(V) + P_{dc,mod}(V)]}. \quad (6.1)$$

A large portion of previous literature in supply modulation focuses on communication standards that are limited to 3-20 MHz of RF bandwidth [110–114]. With an RF bandwidth of 500 MHz (which may necessitate 500 MHz of supply modulation bandwidth), special considerations need to be implemented the bias network on-chip. Common stability capacitors in the supply dc circuit have to be eliminated because the supply has high-bandwidth signal content [10, 44]. A wide passband need to allow low frequency content from the bias pad to the transistors while still isolated at RF frequencies. In addition, some aspects of layout and fabrication will be discussed. Finally, measurements on the device are presented.

6.3.1 DRAIN MATCHING NETWORK

For PA design, the output (drain) matching network requires a dc blocking capacitor to block the dc current from escaping to the RF load. However, for drain supply modulation the dc blocking capacitor cannot be too large as the envelope frequency modulated signal will pass through to the RF load instead of the transistors as desired. A generic PA output matching network is shown in Fig. 6.4. Usually for MMIC design (and hybrid design), the dc blocking capacitor is large in value compared to the other lumped equivalent elements for low RF loss. Also if the capacitor is large, it can be placed anywhere in the matching circuit (and can be integrated with many other components) because it is an RF short. However, for supply modulation applications, a large dc blocking capacitor is detrimental for wide bandwidth supply modulated signals.

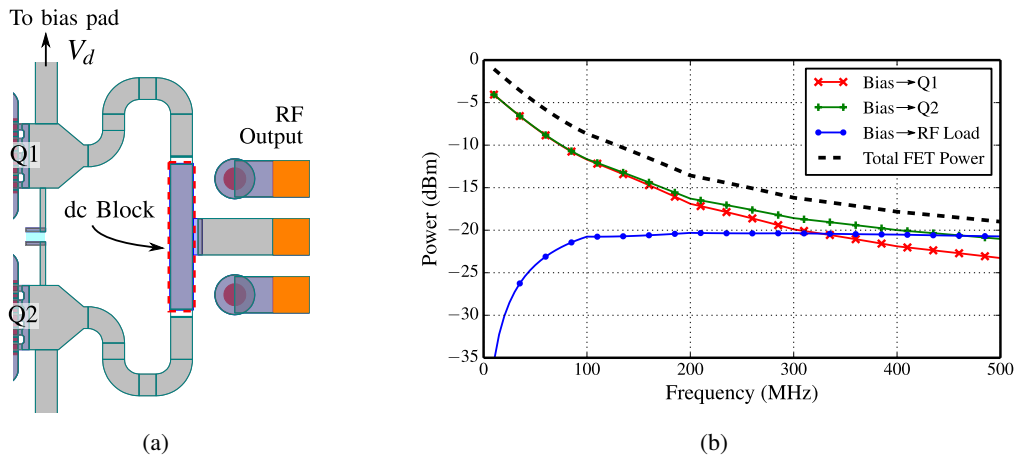


Figure 6.5: (a) Output matching network for EG0447D. The dc blocking capacitor is outlined in a dotted red line. The value of the capacitance is 5.75 pF. (b) Power through the network normalized to 0 dBm. The FET devices were set to 160Ω which is the small-signal drain impedance for the devices used.

As an example, the first designed MMIC's (EG0447D) output matching network is shown in Fig. 6.5a. The capacitance of the dc block is 5.75 pF. The power through the matching network is simulated and the thru power from the bias pad to the transistor device and from the bias pad to the RF load is shown in Fig. 6.5b. Around 300 MHz, the power that reaches the RF load is *higher* than the power that reaches the RF devices. (The relatively low power that reaches the FET at low frequency is due to the large RF shunting capacitance on the bias line and is addressed in the next section.) Larger capacitances only exacerbate the problem allowing more modulated power out through the RF load. Additionally, the power that reaches the near device (Q1) versus the far device (Q2) from the bias pad is different; upwards of 2 dB at 500 MHz. Another hazard of having a large dc blocking capacitor is that the RF load is not necessarily 50Ω : there may be filters or other highly reflective loads (like an antenna) at low frequency that reflect the modulation back to the amplifier causing additional distortion.

Instead, a small dc blocking capacitor must be used to block the low frequency envelope modulation, and must be part of the RF matching. The output network used for the fourth designed MMIC (EG0666B) is shown in Fig. 6.6a. This network uses two series capacitors: the first and larger one is used as an RF short to block the dc; the second and smaller is used to block the low frequency (LF) envelope modulation. The separation of the capacitor functionality reduces the peak voltage that may be across the capacitor (only LF+RF versus dc+LF+RF voltages) which decreases the possibility for dielectric failure. The resulting

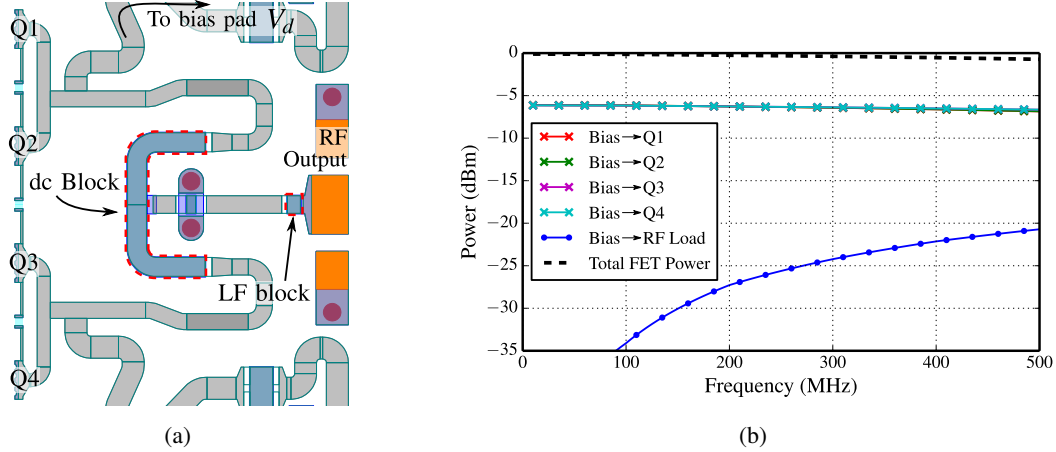


Figure 6.6: (a) Output matching network for EG0666B. The dc blocking capacitor is the large dotted outlined capacitor. The smaller outlined capacitor is the low frequency block. (b) Power through the network normalized to 0 dBm. The FET devices were set to 150Ω which is the small-signal drain impedance for the devices used.

power that reaches all the devices (Q1-Q4) are nearly identical and the total power is close to the ideal of 0 dBm. Finally, the low frequency power that reaches the RF load for EG0666B is 20 dB lower than the power that reaches the devices.

6.3.2 NOVEL BIAS LINE DESIGN

In order to design the bias network for supply modulation, there are a few desirable qualities:

- (1) Small size
- (2) $|S_{21}^{LF}| = 0$ dB; low insertion loss at low frequency.
- (3) $|\Gamma_1^{RF}| = 1$; carrier frequency block (high isolation).

The superscripts RF and LF denote the carrier frequency and low frequency regimes respectively and the subscripts 1 and 2 are the ports looking into the network from the transistor and the power supply respectively. A traditional bias network uses a RF short, or a large shunt capacitor, to provide items 1 and 3. However, item 2 implies that the impedance variation of the network over the low frequency range is small (insertion loss is defined for 50Ω systems). Having even a moderate sized capacitor (for example 15 pF) for the RF short will introduce a large impedance variation, approaching a short circuit at 500 MHz. This means that

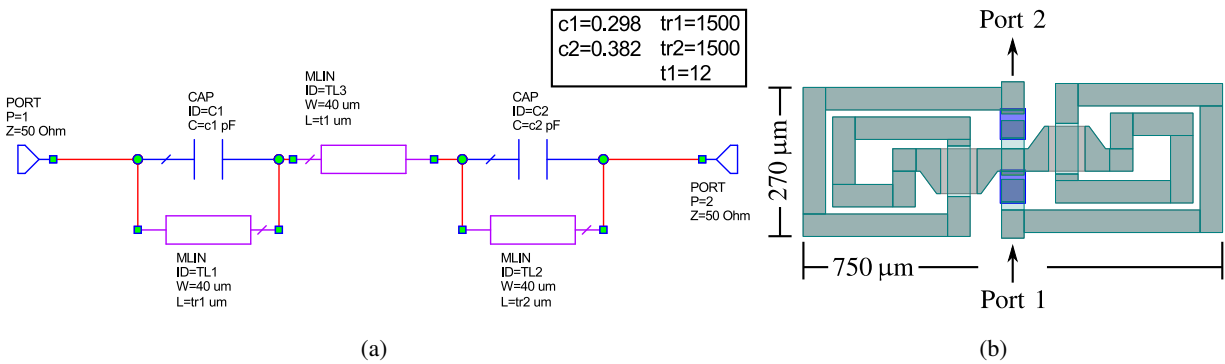


Figure 6.7: Series parallel RF resonator at 10 GHz. (a) Equivalent circuit and (b) EM simulation layout.

the effective capacitance must be reduced as much as possible for the bias network for items 1-3 to be met. Item 3 does not strictly require a phase for the network, however, the phase determines how the network is implemented in the MMIC.

- $1 \angle 0^\circ$; open circuit to allow network placement anywhere.
- $1 \angle 180^\circ$; short circuit (or any other phase), must be correctly phased and used as a matching element.

The carrier RF frequency is 10 GHz with 1 GHz of bandwidth and the low frequency regime is 0-500 MHz. DC must pass through the network, which requires the network to be some form of a parallel resonator. Two cases were considered: a series parallel and a shunt parallel resonator.

6.3.2A SERIES PARALLEL LC RESONATOR

A series parallel resonator was initially considered which presents an open circuit at the resonant frequency (10 GHz) which allows the network to be placed anywhere in the output matching network. The equivalent circuit for the series resonator bias network is shown in Fig. 6.7a. Two series resonators are cascaded together with slightly different resonant frequencies to give the desired 1 GHz of bandwidth. Since the goal is high reflectivity, a high Q is needed limiting the bandwidth of a single resonator. Bandwidth could be increased by increasing the inductance, however, this greatly increases the size of the resonator which is undesired.

The layout shown in Fig. 6.7b was simulated in AXIEM, a method of moments 2.5D simulator for planar circuits. The stackup used is the TriQuint 0.15 μm GaN process and all capacitors are 240 pF/mm² (CT9).

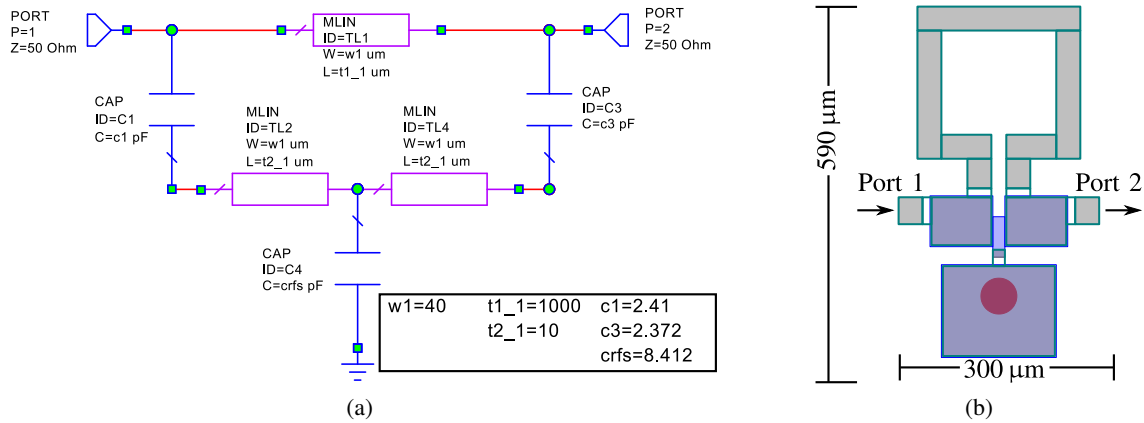


Figure 6.8: Shunt parallel RF resonator at 10 GHz. (a) Equivalent circuit and (b) EM simulation layout. The smaller series capacitors block low frequency content while allowing the RF to pass through to the large RF shunt shorting capacitor.

Performance of the resonator has about 1 GHz of bandwidth and 20 dB of isolation (Fig. 6.9a). The LF performance is good with 0.1 dB of loss at 1 GHz. Better isolation comes at expense of larger line lengths and larger layout size. The LF parameters are almost ideal for wideband supply modulation as shown in Fig. 6.9b. The equivalent capacitance is 0 pF (actually slightly inductive).

6.3.2B SHUNT PARALLEL LC RESONATOR

The shunt LC implementation aimed to bypass the difficulty of creating a resonator with a high-Q by showing a short circuit to the RF while passing the low frequencies. The equivalent circuit of the resonator is shown in Fig. 6.8a.

The performance shows better than 30 dB of isolation in a fairly wide bandwidth from 8.5 GHz to 13.5 GHz (Fig. 6.9a). The low frequency performance also is slightly degraded compared to the series LC resonator. The effective capacitance is 1.84 pF across the 1 GHz of low frequency bandwidth as shown in Fig. 6.9b. With just one EM simulation iteration (and no space optimization), the performance and size gives promising results for a practical implementation on-chip.

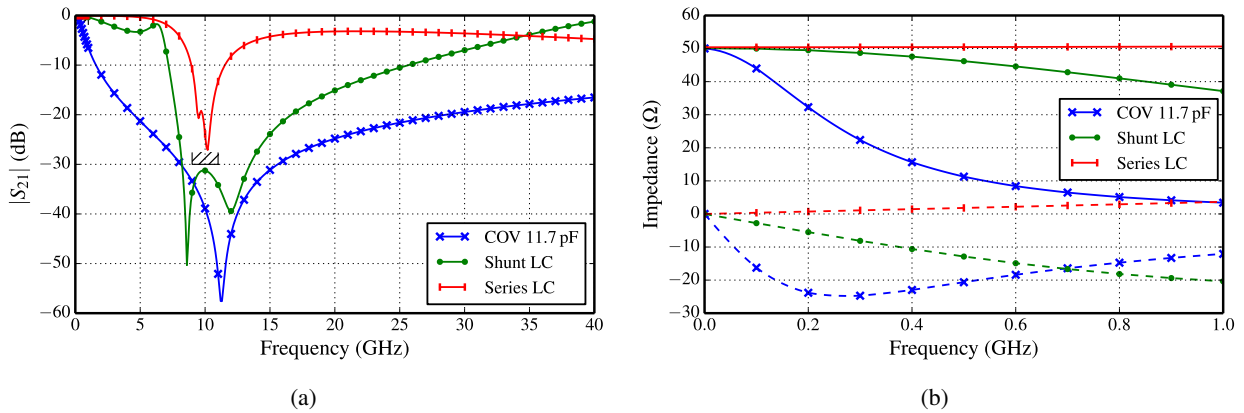


Figure 6.9: Performance of a parallel shunt LC , parallel series LC , and traditional capacitor-over-via (COV) bias networks. (a) Isolation ($|S_{21}|$) of the bias network. (b) Input impedance into the RF choke network in a $50\ \Omega$ system. Dotted lines are the imaginary part of the impedance.

6.3.2C COMPARISON TO TRADITIONAL BIAS NETWORK

The series LC resonator is compared to traditional capacitor-over-via (COV) RF choke networks. The COV size of $11.7\ \text{pF}$ was chosen to give good RF isolation at $10\ \text{GHz}$, comparable to the series LC case. The performance is shown in Fig. 6.9. While the RF isolation is good, the LF impedance variation is large with the real part only being a few ohms at $1\ \text{GHz}$.

Other bias networks were simulated, including a reduced length $\lambda/4$ line (with compensating capacitors). However, while the length of transmission line could be reduced, the capacitance needed greatly degrades the low frequency input match. Even with a shortened line of $2000\ \mu\text{m}$ (compared to a full $\lambda/4 = 3000\ \mu\text{m}$ at $10\ \text{GHz}$), the length of line for adequate isolation is far too large to be practical on a MMIC.

6.3.2D MR4 BIAS NETWORK IMPEDANCE

For EG0666, the novel shunt resonant bias line was used on the first and second stage of the PA. Fig. 6.10 annotates the first and second stage bias areas. The dotted line highlights the parallel shunt resonator with the two series capacitors and the COV (blueish polygon with red circle). The first stage only requires about $200\ \text{mA}$ of current maximum so the lines are sized appropriately. Similarly, the second stage will draw a maximum of about $1.2\ \text{A}$ of current which requires the width of the line to be considerably wider.

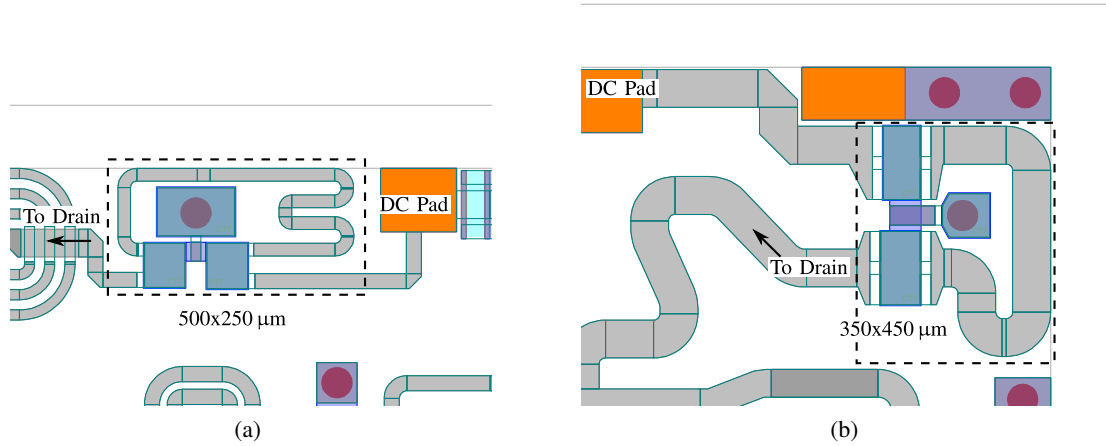


Figure 6.10: (a) First and (b) second stage resonant bias network to short the RF while inducing small distortion at low frequencies. The thickness of the bias lines are determined by the expected dc current through the network.

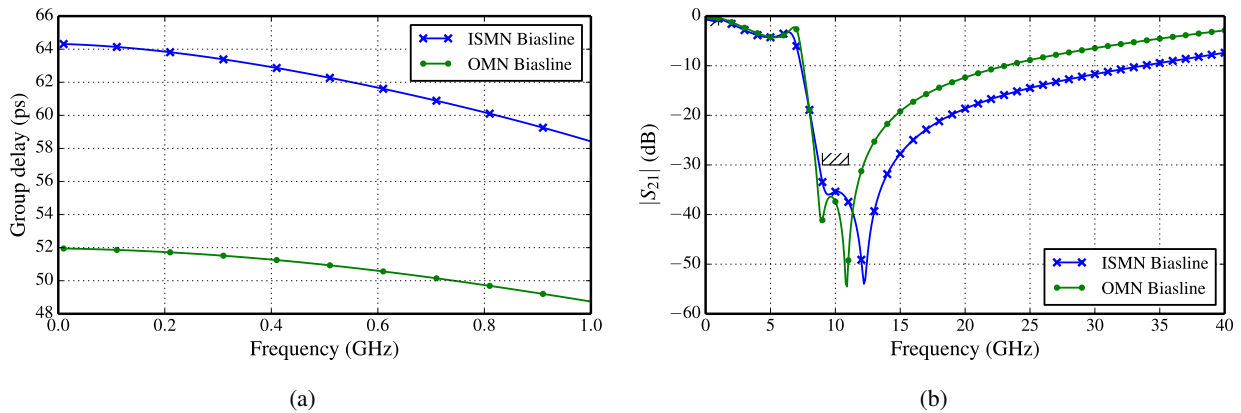


Figure 6.11: Performance of the drain bias networks on EG0666. (a) Group delay variation over 1 GHz of bandwidth at low frequency. (b) Isolation at RF frequencies.

Both implementations are fairly compact taking up 0.125 mm^2 and 0.158 mm^2 for the first and second stage respectively. For comparison, a 15 pF capacitor takes up 0.05 mm^2 of space for a density of 300 pF/mm^2 . Fig. 6.11 shows the simulated bias network performance of the areas in Fig. 6.10. The group delay variation is 5.9 ps and 3.2 ps for the first and second stage drain bias networks and the equivalent capacitance is 2.06 pF and 1.78 pF respectively. Both networks have isolation in excess of 35 dB in a 1 GHz bandwidth for a center frequency of 10 GHz .

The impedance looking into the PA from the bias pad is simulated for the output network similar to

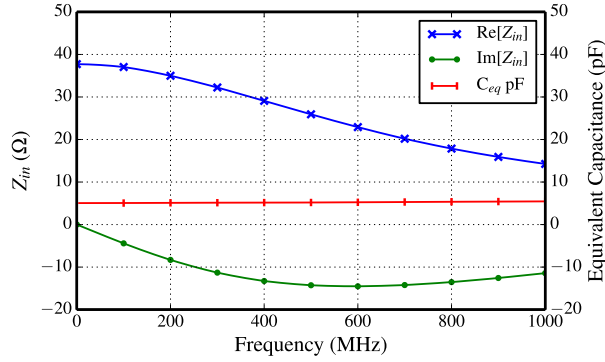


Figure 6.12: Simulated network impedance as seen from the dc bias pad on the EG0666 MMIC with extracted capacitance. The capacitance is constant which means that there is no resonances in the network up to 1 GHz.

Fig. 6.9. The impedance of the output transistors were set to a constant resistance of $150\ \Omega$ to give a dc impedance of approximately $30\ \Omega$ as seen in measurements with a LF VNA. The impedance is shown in Fig. 6.12. The equivalent parallel capacitance is also shown and is a constant $5\ \text{pF}$ across the frequency range to 1 GHz. The extra capacitance (in comparison of the $1.78\ \text{pF}$ stated in the previous paragraph) is due to the RF matching and blocking capacitance in the output matching network.

However as the LF and RF performance is good for supply modulation, there are potential unintended consequences that arise when one opens up the LF bandwidth for modulation through the bias line. The most important is stability of the amplifier. Traditionally, large capacitances are used on the biasline specifically for stability. Considering Fig. 6.9, the COV has greater than 10 dB of isolation at approximately 2 GHz onward. The shunt *LC* resonator however, has less than 3 dB of attenuation through the network up to 7 GHz. Any off-chip elements can potentially resonate with on-chip capacitors to give high-Q tanks ripe for oscillation conditions. This means that at bandwidths above the modulation bandwidth up to the carrier frequency bandwidth ($500\ \text{MHz} < f < 9\ \text{GHz}$) need adequate attenuation on the bias line or precise impedance terminations off-chip. Stability is analyzed in the next section.

6.4 FUTURE WORK

While a large number of measurements have been performed for supply modulation with wide bandwidth signals, there is still a long way to go before a comprehensive model for design and simulation of supply

modulated transmitters is available. Specifically related to modeling for supply modulation, some possible future directions are listed below:

- (1) Full characterization of trapping effects are necessary to distinguish from the other low frequency effects seen in this thesis. This thesis focused on characterization under large-signal at multiple frequencies. How does trapping effect the measurements performed and can the effect be decoupled? There is a significant amount of literature that has focused on methods and measurement of trapping effects, all of which require specialized instrumentation or custom circuits [30, 31, 38, 115].
- (2) Thermal effects were ignored as controlled temperature measurements could not be made. Investigation of temperature dependence of the mixing transfer functions may be necessary for increased modeling/simulation accuracy in design.
- (3) Modeling investigation for supply modulation. One area that was not covered in this thesis is the required modifications that would be needed to a nonlinear model (Angelov or otherwise) to enable accurate supply modulation simulations. This is an immense problem that extends from modeling the physical phenomena of the effects shown in this thesis to how the harmonic balance simulators operate and how envelope simulations work in the commercial simulators.

The versatility of the setup allows for the LF couplers to be place within another measurement system, as is done in this thesis with RF and LF paths, or used as an independent instrument. For example, the bidirectional couplers with the oscilloscope can be used to create a complete LSNA for measurement of time domain wave parameters from 10 kHz up to 1 GHz. Some applications for a LF LSNA are measurement of UHF (ultra high frequency) amplifiers [116, 117] or characterization of supply modulators within a transmitter [95]. However, the setup can be improved for more advanced and specialized measurements:

- (1) Integration of RF LSNA for full vector measurements of RF signals. The ability to measure the phase of the RF allows better modeling of the mixing transfer functions. While a customized RF LSNA can be created [61], the hardware and calibration is complex.
- (2) Optimization of current measurement setup components. For example, the oscilloscope can handle

up to 5 V pk-pk which is considerably more than what is being presented currently (closer to 100 mV pk-pk). The couplers coupling could be decreased to give larger signal-to-noise ratios, especially on the gate where the input signals are necessarily smaller to prevent the device from drawing too much current.

- (3) Pulsed measurements. This is related to (1) and (2) of the previous list on modeling as pulsing is sometimes required for characterizing trapping and thermal effects. However, there are specific applications that used pulsed signals, such as radar. Investigating wide bandwidth RF pulses was one of the original goals of the DARPA Microscale Power Conversion (MPC) project that this thesis was funded on.

Describing functions (DF) were introduced and developed to analyze a very specific large-signal phenomena seen in measurement. The DF method developed, however, is very general and can be used for any nonlinear phenomena, not necessarily FET devices or even electronic circuits. Some potential future directions for DF are:

- (1) Extending DF to allow incorporation of linear, reactive, and potentially other nonlinear elements. As presented in this thesis, only the nonlinear current source of a FET was modeled. Extending the theory to incorporate linear and/or additional nonlinear elements would allow analysis of entire circuits which would be useful for describing how load impedances affect the nonlinearity as well.
- (2) Application of DF to wide bandwidth signals. As signals increase in bandwidth, it would be useful to be able to describe the nonlinearity in terms of such a signal. This may involve either: adding many tones within the bandwidth of the signal (as is done with multisine signals to simulate high PAR signals); or using the DF for Gaussian noise and limiting the PAR to 11 dB (which is the approximate PAR of modern communication modulation standards).
- (3) Application of DF to advanced transmitter topologies such as harmonic injection [118], outphasing [119], or other frequency conversion applications such as wireless powering [71, 120–122].

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APPENDIX A

COAXIAL CALIBRATION VERIFICATION

Since a probe station calibration verification is difficult to perform without instruments that can measure absolute power and/or phase of on a probed element as stated in Chapter 2, additional measurements are given here for a 2-port coaxial calibration. A coaxial calibration is considerably easier to validate considering most measurement instruments, including power meters, oscilloscopes, and spectrum analyzers have coaxial input ports.

Some 2-port relative measurements are compared to a commercial PNA measurement and lastly a generated harmonic waveform is measured and captured at the calibration plane with an oscilloscope.

A.1 RELATIVE CALIBRATION VALIDATION WITH PNA E8364C

The two test networks shown in Fig. A.1 are a $150\ \Omega$ 1-port load and a low-pass filter (LPF) designed as part of a LF bias network. The calibrated measurements of S-parameters from the LFNVA and the PNA are shown in Figs. A.2 and A.3 for the $150\ \Omega$ load and the LPF respectively.

The PNA regardless of the measurement or how carefully calibrated always had a spike in its S-parameters at 13 MHz. These measured points by the PNA are suspect. However, the agreement between the PNA and custom LFNVA is good as shown by the error in Fig. A.4. The error is defined by

$$\Delta_{ij} = 20 \log_{10} |S_{ij}^A - S_{ij}^B|. \quad (\text{A.1})$$

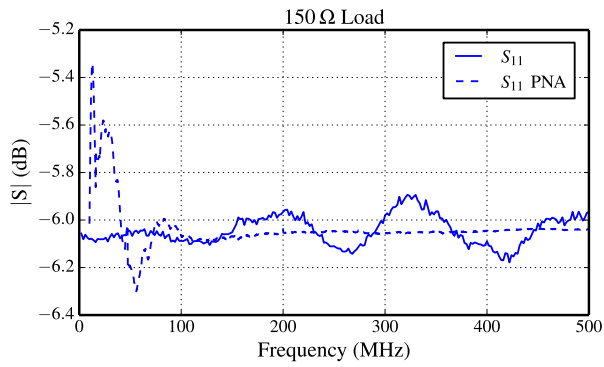


(a) 150 Ω load

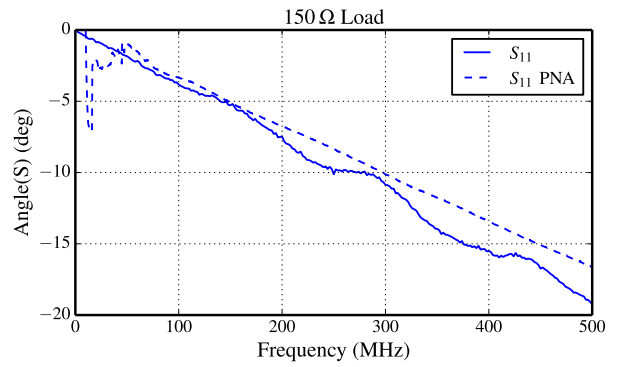


(b) Low pass filter

Figure A.1: Photographs of the test networks used to validate the relative calibration of the LFNVA.



(a)



(b)

Figure A.2: Comparison of the S-parameters of the 150 Ω load between the LFNVA and commercial PNA. (a) Magnitude in dB and (b) phase of the input reflection coefficient.

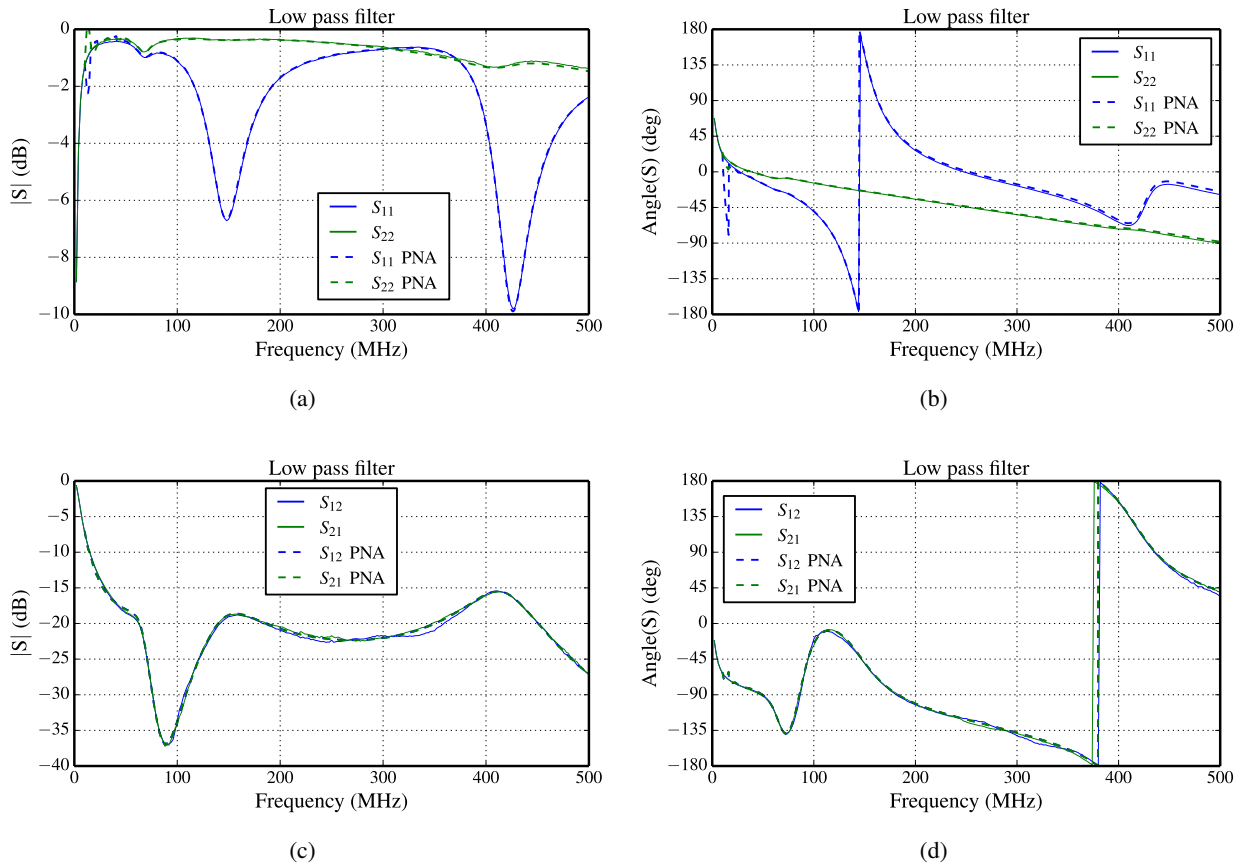


Figure A.3: Comparison of the S-parameters of the 150 Ω load the LFFVNA and commercial PNA. (a),(c) Magnitude in dB and (b),(d) phase of the S-parameters.

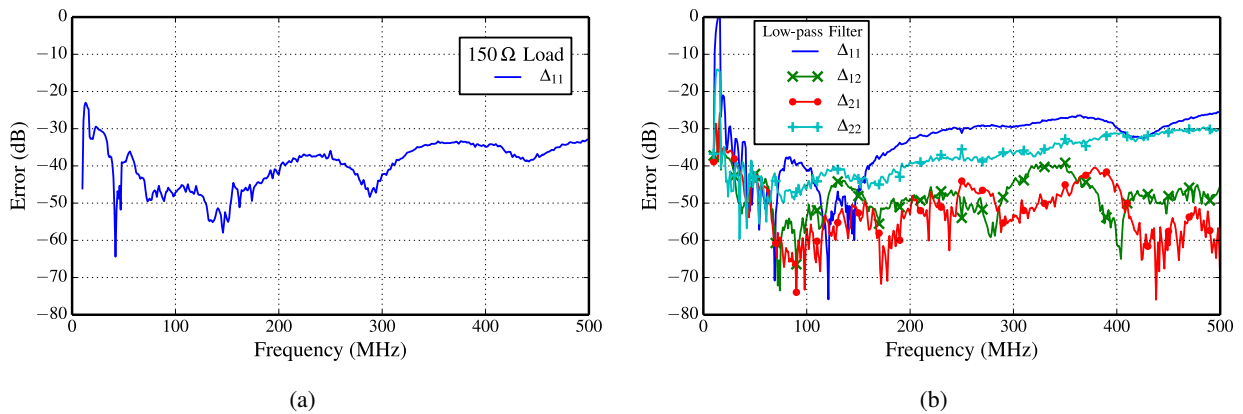


Figure A.4: Error between the individual S-parameters of the (a) 150 Ω and (b) LFFVNA test networks. There is very good agreement of >30 dB for most of the frequencies except at low frequencies where the commercial PNA's accuracy is suspect.

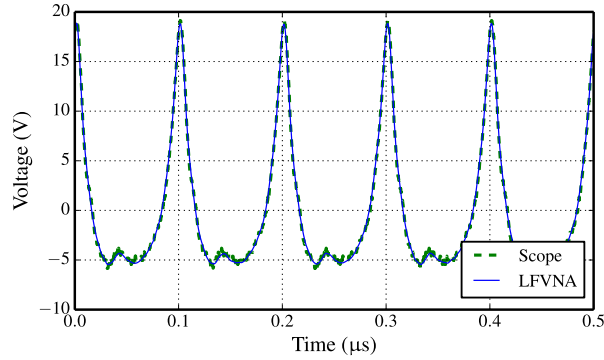


Figure A.5: Comparison of calibrated waveform from LFBNA and oscilloscope measurement for 2-tone RF excitation of a GaN FET. The RF $\Delta f = 10$ MHz giving a harmonic waveform at LF with fundamental of 10 MHz.

A.2 ABSOLUTE CALIBRATION VALIDATION WITH OSCILLOSCOPE

Verification of the absolute calibration was performed by measuring the waveform at the reference plane with a bench top oscilloscope. A multi-harmonic waveform was generated at LF by a two-tone excitation of a GaN FET at 10 GHz. The mixing products down to LF create a highly nonlinear waveform that was measured with the LFBNA and an oscilloscope. The time-aligned waveforms are shown in Fig. A.5. The agreement is exceedingly good with the waveforms overlaying each other almost identically.

APPENDIX B

ACTIVE LOADPULL

Originally proposed by [123], an impedance can be synthesized by modifying the reflected waveform at a particular reference plane. The waveform modification is performed by injecting power effectively changing the reflection coefficient seen by a device. There are numerous papers detailing active loadpull systems [124–131]. However, few outline the theory for required power and angle of the injection source. Of note, [132] derives the required power for a DUT under a matched load. Here, a complete formula to present an arbitrary impedance at a reference plane with a real reference impedance will be derived.

B.1 THEORY

The reference impedance, denoted here by Z_{ref} , of the waves will be of great importance. Many previous papers use only one reference impedance, usually $50\ \Omega$, to derive power relationships. Here, two reference impedances are used, one for the device under test with $Z_{ref} = Z_D$, and the other for the generator (and measurement devices) of $Z_{ref} = Z_0$. From Fig. B.1, a_D and b_D will be have $Z_{ref} = Z_D$ while a_S^0 and b_S^0 will have $Z_{ref} = Z_0$. The reflection coefficient seen by a DUT with characteristic impedance of Z_D is

$$\Gamma_D = \frac{a_D}{b_D} \tag{B.1}$$

with the variables and directions detailed in Fig. B.1. In the active loadpull case, the available wave, b_D , and reflection seen by the device, Γ_D , are known or given while the injected wave, a_S^0 , is the desired parameter.

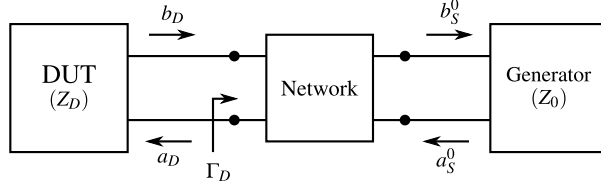


Figure B.1: Flow chart diagram for power injection to synthesize an impedance at the DUT.

The wave b_D can be computed from the available output power wave of the device. In contrast, the total output power is given by

$$P_D = \frac{1}{2}|b_D|^2 - \frac{1}{2}|a_D|^2 \quad (\text{B.2})$$

which may change depending on the reflection coefficient seen (the reflected wave a_D).¹ Considering Fig. B.1, the network is an ideal dummy network that will facilitate the conversion of power waves² from one reference impedance to another. Using T-parameters and the same reference impedance on both sides of the network:

$$\begin{pmatrix} a_D \\ b_D \end{pmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{pmatrix} a_S^D \\ b_S^D \end{pmatrix}, \quad (\text{B.3})$$

where a_S^D and b_S^D are the generator waves converted to a reference impedance of Z_D . The network is ideal (no loss and perfect match) only when the reference impedance for the wave parameters are the same on each port of the network. Port 2 of the network (right side) can now be converted to power waves with reference impedance of Z_0 with

$$\mathbf{P}^{nm} = \frac{1}{2\sqrt{\text{Re}[Z_m]\text{Re}[Z_n]}} \begin{bmatrix} Z_m^* + Z_n & Z_m - Z_n \\ Z_m^* - Z_n^* & Z_m + Z_n^* \end{bmatrix}. \quad (\text{B.4})$$

So converting the generator waves to the device waves:

$$\begin{pmatrix} a_S^D \\ b_S^D \end{pmatrix} = \mathbf{P}^{D0} \begin{pmatrix} a_S \\ b_S \end{pmatrix} \quad (\text{B.5})$$

¹ This is an important difference between this derivation and the one in [132] where they set P_D without regard to the reflected power, forcing their derivation to be for a DUT with a matched load on the output.

² Power waves [133] are used here to allow easy comparison to popular commercial harmonic balance simulators (all of which use power waves). The same derivation procedure can be used with pseudo-waves using equation (79) from [59] instead of the power wave reference impedance conversion in (B.4).

and applying to (B.3),

$$\begin{pmatrix} a_D \\ b_D \end{pmatrix} = \frac{1}{2\sqrt{\text{Re}[Z_0] \text{Re}[Z_D]}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} Z_0^* + Z_D & Z_0 - Z_D \\ Z_0^* - Z_D^* & Z_0 + Z_D^* \end{bmatrix} \begin{pmatrix} a_S \\ b_S \end{pmatrix}. \quad (\text{B.6})$$

The previous equation relates the waves at an interface with different reference impedances. This can easily be checked by setting $Z_D = Z_0$. From here on, the system reference impedance, Z_0 , is assumed to be real.

The equation for b_D is now solved for b_S which is then substituted into the equation for a_D ,

$$a_D = \frac{2a_S Z_0 \text{Re}[Z_D] + b_D (Z_0 - Z_D) \sqrt{Z_0 \text{Re}[Z_D]}}{(Z_0 + Z_D^*) \sqrt{Z_0 \text{Re}[Z_D]}}, \quad (\text{B.7})$$

which is then solved for the injected wave a_S ,

$$a_S = \frac{1}{2\sqrt{Z_0 \text{Re}[Z_D]}} \left[a_D (Z_0 + Z_D^*) + b_D (Z_D - Z_0) \right]. \quad (\text{B.8})$$

Equation (B.1) is used to eliminate a_D .

$$a_S = \frac{b_D}{2\sqrt{Z_0 \text{Re}[Z_D]}} \left[\Gamma_D (Z_0 + Z_D^*) + (Z_D - Z_0) \right]. \quad (\text{B.9})$$

Equation (B.9) is the required injected wave to present a reflection coefficient of Γ_D to the DUT with a characteristic impedance of Z_D and an available output power wave of b_D . For an open and short circuit with a real Z_D :

$$a_S \Big|_{\Gamma_D=1} = b_D \sqrt{\frac{Z_D}{Z_0}}, \quad (\text{B.10})$$

$$a_S \Big|_{\Gamma_D=-1} = -b_D \sqrt{\frac{Z_0}{Z_D}}. \quad (\text{B.11})$$

Of note is Γ_D is the reflection coefficient with characteristic impedance of Z_D , whereas the impedance may be more useful in the system impedance. From [59], the reflection coefficient conversion to Z_0 with a real Z_D is

$$\Gamma_D^0 = \frac{\Gamma_{0D} + \Gamma_D}{1 + \Gamma_{0D} \Gamma_D}, \quad (\text{B.12})$$

where

$$\Gamma_{0D} = \frac{Z_D - Z_0}{Z_D + Z_0}. \quad (\text{B.13})$$

Substituting the previous equation into (B.9) (assuming a real Z_D) gives

$$a_S = \frac{2b_D \Gamma_0^D \sqrt{Z_0 Z_D}}{(Z_0 + Z_D) + \Gamma_0^D (Z_0 - Z_D)} \quad (\text{B.14})$$

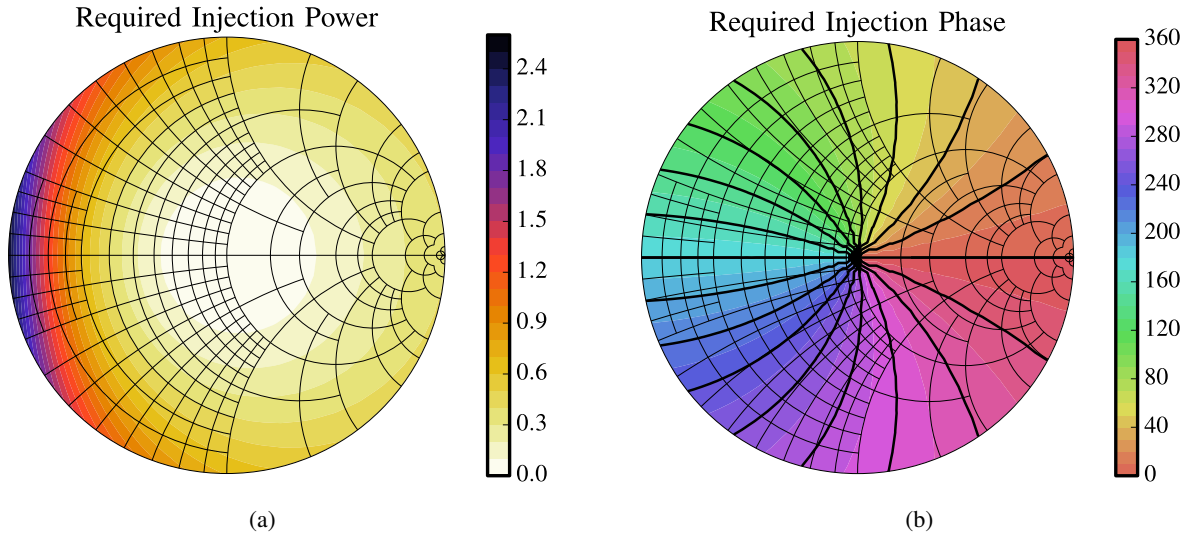


Figure B.2: Required injected (a) power and (b) phase to present a particular reflection coefficient. The Smith charts are normalized to the device impedance, $Z_D = 20 \Omega$.

B.2 EXAMPLES

B.2.1 $Z_D = 20 \Omega$

Fig. B.2 shows the power and phase of what would be required to present a particular load with a DUT impedance of 20Ω and available power of 1 W. Fig. B.2a illustrates the increasing amount of power needed to achieve a small increase in reflection coefficient (system impedance with $Z_{ref} = Z_0$) when approaching a short circuit active impedance. To go from $\Gamma = 0.6 \angle 180^\circ$ to a short circuit requires an additional 2 W of power while a majority of the impedances to the right of $\Gamma = 0.6 \angle 180^\circ$ can be reached with less than 0.6 W total injected power. Fig. B.2b shows that by increasing the injection power, the measured impedance trajectory will be curved depending on the initial injected phase.

B.2.2 $Z_D = 1 \Omega$

For a transistor with an available output power of 100 W ($b_D = \sqrt{200}$), $Z_D = 1 \Omega$, and $\Gamma_D = 0$, the required power of the injection is

$$a_S = \frac{\sqrt{200}}{2(1)} \sqrt{\frac{1}{50}} [-(50 - 1)] = -49 \quad (\text{B.15})$$

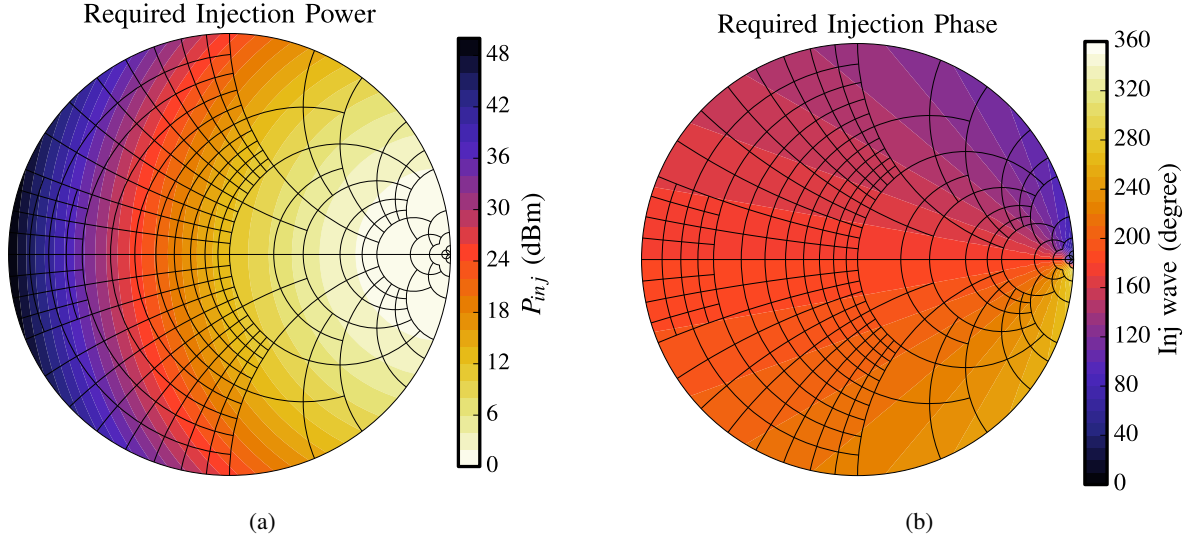


Figure B.3: Required injected (a) power and (b) phase to present a particular reflection coefficient. The Smith charts are normalized to the device impedance, $Z_D = 1 \Omega$.

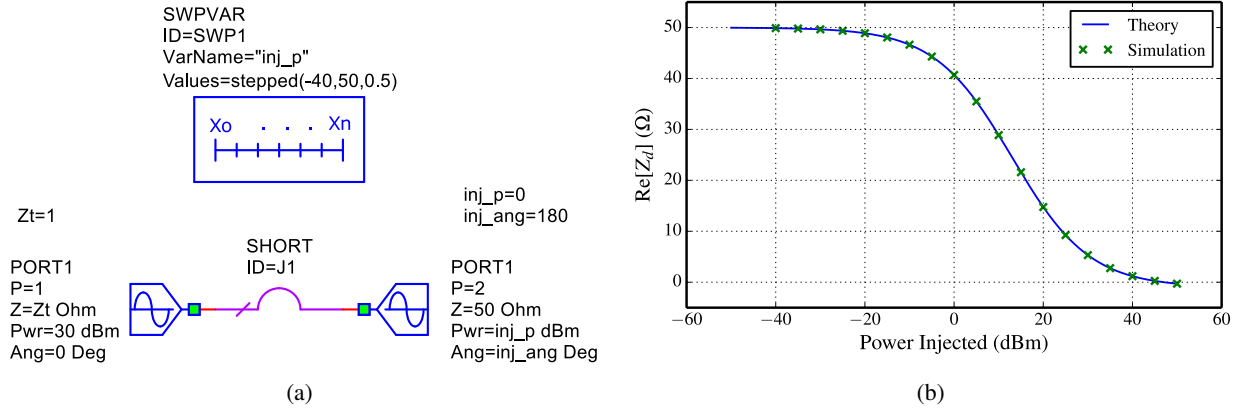


Figure B.4: (a) Schematic of active loadpull simulation in AWR. (b) Simulation and theory of the real axis of Fig. B.3a in terms of real impedance that the device sees. Note that the x-axis is in log power (dBm).

$$P_{inj} = \frac{1}{2} |a_S|^2 = 1200.5 \text{ W} \quad (\text{B.16})$$

with a phase of 180° relative to b_D . This is the same result as given in [132].

The power and phase required of the injection source to cover the entire Smith chart with a DUT available power of 1 W is shown in Fig. B.3. The results make sense as the required power is zero to present 50Ω (on the right side of the 1Ω Smith chart). Of note are the phases of the injection source range from 110° to 250° . Anything out side that range requires a very small amount of injected power, otherwise $\Gamma > 1$. A

cross-section of Fig. B.3a is shown in Fig. B.4 in terms of the power needed (with phase 180°) to reach a particular impedance. The theoretical result from (B.9) is compared to simulation as shown in Fig. B.4a and the results agree exactly.

APPENDIX C

ANGELOV NONLINEAR MODEL

The Angelov nonlinear model is a compact model for FET devices which dates back to 1992 for HEMTs on GaAs [134]. Recently, it has been extensively developed by the group at Chalmers University of Technology and by Ilcho Angelov himself [98–100, 135–137]. The extraction is based on modeling the I - V curves, $I_{ds}(V_{gs}, V_{ds})$, and the conductance, $g_m(V_{gs})$. As the development has been open and has spanned multiple decades, there are many formulations to account for various effects that have been encountered over the years, including low frequency dispersion, thermal effects, and various process types including CMOS and FINFET devices. The formulation used in this thesis for simulation and modeling in Chapter 5 is covered here. The particular formulation is the “Idsmod=0”, “Igmmod=1”, and “Capmod=1”, which follows the implementations in the National Instruments AWR and Keysight ADS software suites documentations. The significant differences from the documentation of AWR/ADS is the backgate modeling and the diode breakdown current.

C.1 COMPACT MODEL SCHEMATIC

Fig. C.1 shows the topology of the Angelov compact nonlinear model.

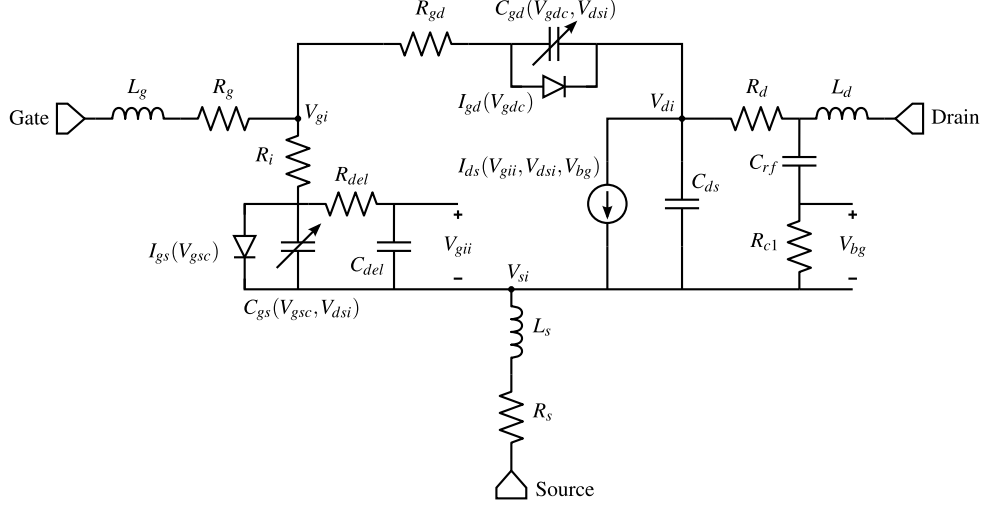


Figure C.1: Schematic for Angelov nonlinear FET model. There are three nonlinear elements; C_{gs} , C_{gd} , and I_{ds} . In addition there are two breakdown diodes; I_{gs} and I_{gd} . Of importance to the Angelov model is the inclusion of the back-gate voltage, V_{bg} , and the dependence of the current source on this voltage.

C.1.1 NONLINEAR ELEMENT EQUATIONS

Equations for the nonlinear current source (“Idsmod=0”) are given as:

$$P1m = P1(1 + B1/\cosh(B2 * V_{dsi})^2) \quad (C.1)$$

$$Vpkm = Vpks - Dvpks + Dvpks * \text{dhyp}(\alpha_S V_{dsi}) - Vsb2 (V_{dgi} - Vtr)^2 - Vbg \quad (C.2)$$

$$\psi = P1m (V_{gii} - Vpkm) + P2 (V_{gii} - Vpkm)^2 + P3 (V_{gii} - Vpkm)^3 \quad (C.3)$$

$$\alpha = \alpha_R + \alpha_S (1 + \text{dhyp}(\psi)) \quad (C.4)$$

$$I_{ds}(V_{gii}, V_{dsi}, V_{bg}) = Ip k0 (1 + \text{dhyp}(\psi)) \text{dhyp}(\alpha V_{dsi}) (1 + \lambda V_{dsi} + Lsb0 \exp_{soft}(V_{dgi} - Vtr)) \quad (C.5)$$

where

$$\text{dhyp}(x) = \frac{x}{\sqrt{1 + x^2}}. \quad (C.6)$$

The exponential function is modified to prevent overflow during convergence calculations:

$$\exp_{soft}(x) = \text{if}(x < \ln(1E99)) \text{ then } \exp(x) \text{ else } (x - \ln(1E99) + 1) \times 1E99 \quad (C.7)$$

The model parameters used for simulations in Chapter 5 are listed in Table C.2.

The nonlinear diode equations (“I_{gmod}=0”) are given as:

$$I_{gs1} = \exp_{soft}(Pbdg(-V_{gdc} - Vbdgs)) - \exp_{soft}(-Pbdg * Vbdgs) \quad (C.8)$$

$$I_{gs}(V_{gsc}) = Ij(\exp_{soft}(Pg(V_{gdc} - Vjg)) - (1E-6 * Kbdgate * I_{gs1}) - \exp_{soft}(-Pg * Vjg)) \quad (C.9)$$

$$I_{gd1} = \exp_{soft}(Pbdg(-V_{gdc} - Vbdgd)) - \exp_{soft}(-Pbdg * Vbdgd) \quad (C.10)$$

$$I_{gd}(V_{gdc}) = Ij(\exp_{soft}(Pg(V_{gdc} - Vjg)) - (1E-6 * Kbdgate * I_{gd1}) - \exp_{soft}(-Pg * Vjg)) \quad (C.11)$$

where V_{gdc} and V_{gsc} are the voltages across the gate-drain, and gate-source capacitances respectively. The diode model parameters used are listed in Table C.3.

The nonlinear capacitor equations for “Capmod=1” are:

$$Tanh1 = 1 + dhyp(P10 + P11 V_{gsc} + P111 V_{dsi}) \quad (C.12)$$

$$Tanh2 = 1 + dhyp(P20 + P21 V_{dsi}) \quad (C.13)$$

$$Tanh3 = 1 + dhyp(P30 - P31 V_{dsi}) - P111 \quad (C.14)$$

$$Tanh4 = 1 + dhyp(P40 + P41 V_{gdc} - P111 V_{dsi}) \quad (C.15)$$

$$C_{gs}(V_{gsc}, V_{dsi}) = C_{gs0} Tanh1 Tanh2 \quad (C.16)$$

$$C_{gd}(V_{gdc}, V_{dsi}) = C_{gd0} (Tanh3 Tanh4 + 2P111) \quad (C.17)$$

where V_{gdc} and V_{gsc} are the voltages across the gate-drain, and gate-source capacitances respectively. C_{gs} and C_{gd} is the instantaneous capacitance as a function of the control voltages. To calculate the current through the capacitors, the derivative of the voltage across the capacitor is needed:

$$i = C(v) \frac{dv}{dt}. \quad (C.18)$$

The voltage derivative is not straight forward to implement in a HB simulator. For ADS, the correct implementation is shown in Fig. C.2. The implementation uses a symbolically defined device (SDD) where port 1 of the SSD (P1, P2) is the capacitor terminals and port 2 (P3, P4) is the V_{dsi} control voltage. The voltages on the SDD ports are accessed by the $_vi$ variables. The F on port 3 of the SSD denotes that the current on that port is an implicit equation. This means that the lines $F[3,0]+F[3,1]=0$. The derivative of the capacitor terminal voltage ($F[3,1]=V_{gdc}/1e9$) is set as part of the equation while the port current

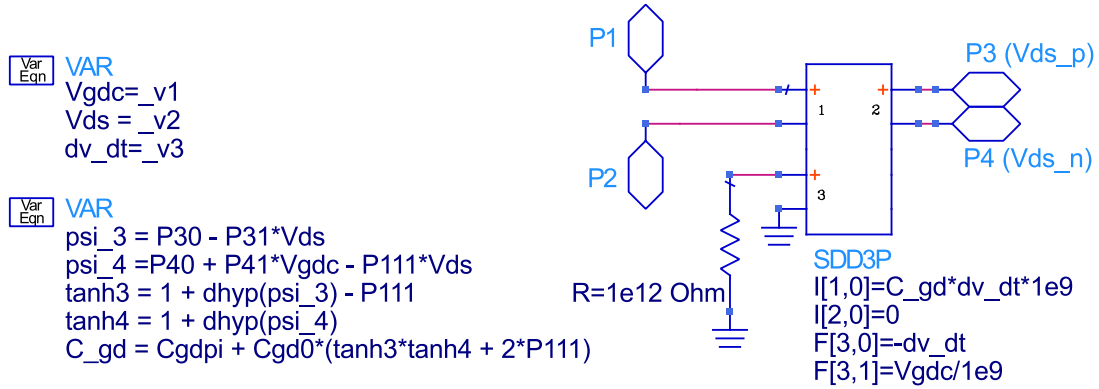


Figure C.2: Schematic for Angelov nonlinear capacitances built in ADS with a symbolically defined device (SDD) element. Shown is the C_{gd} model. The C_{gs} model would be very similar, but with modified equations. The ports 1 and 2 are the access points to the capacitor while ports 3 and 4 is the V_{dsi} control voltage (no current through that terminal).

($F[3,0] = -dv_dt$) is set as the voltage at that port. To avoid unnecessarily high voltages, currents, and also for numerical purposes, the voltage derivative is divided by a scaling parameter (in this case $1E9$). Finally, the current through port 1 of the SDD is given by $I[1,0]$ which is the capacitance multiplied by the rescaled voltage derivative.

The capacitor model parameters used are listed in Table C.4.

The other intrinsic and extrinsic lumped element parameters are given in Table C.5. The extremely low resistance and capacitance on the source were due to modeled end vias that were added on externally to the model. Two end vias were added in parallel on the source with values $L_{via} = 0.032$ nH and $R_{via} = 0.02$ Ω .

C.1.2 BACK-GATE MODEL

Of particular interest is use of the simple dispersion model, C_{rf} and R_c with the back-gate voltage, V_{bg} . The simple model comes from extensive GaAs MESFET research in the 80's and 90's [138–140]. The two element network is used to differentiate the output impedance seen at dc and at RF frequencies (>1 MHz) as can be seen in Fig. C.3 [33].

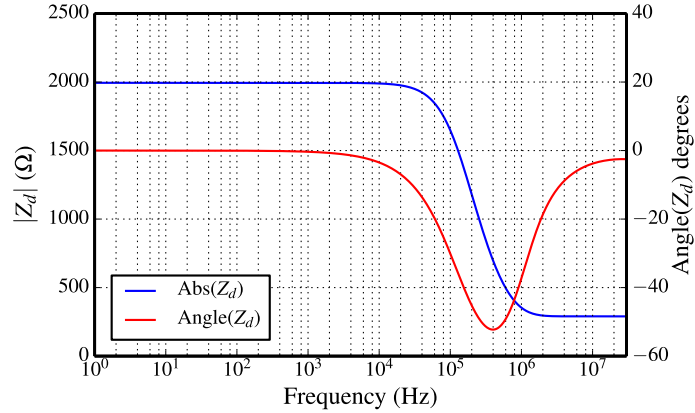


Figure C.3: Simulation of an Angelov model with the *RC* back-gate dispersion model. The impedance at dc is high (which is seen directly in the *I-V* curves) and after the frequency dispersion cutoff, the impedance is more than a factor of 4 lower.

C.2 USAGE OF DHYP, TANH, AND ERF

Implementation in CAD software commonly uses the dhyp function defined in (C.6) instead of the tanh function. Originally, Angelov has stated that ideally the solution of I_{ds} as a function of V_{gs} should be an, erf, or error type function [136]. The erf, tanh, and dhyp functions are plotted in Fig. C.4. One can observe that the erf converges the quickest to 1 while tanh is next and dhyp has the softest convergence. Evaluation of the three functions to 6 decimal places at $x = 4.0$ is shown in Table C.1. The erf function is not commonly implemented in CAD software and, in addition to tanh, is expensive to compute. The time to compute the function 10000 times in python is given in Table C.1. dhyp is the most commonly used function in lieu of erf and is the fastest to evaluate with a division, one multiplication, and one square root operation.

Table C.1: Evaluation of dhyp, tanh, and erf functions.

	f(4.0)	Time (s) (10000 evaluations)
erf(x)	1.000000	0.649334
tanh(x)	0.999329	0.796014
dhyp(x)	0.970143	0.193113

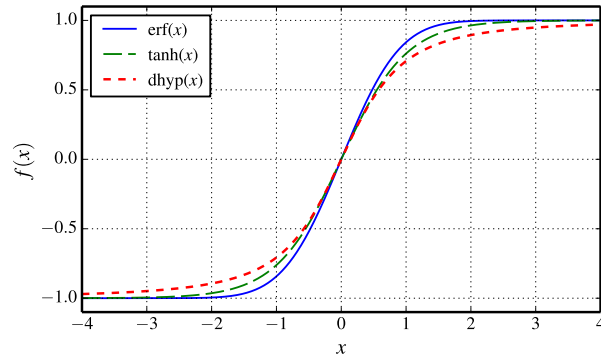


Figure C.4: Comparison between the sigmoid functions $\text{erf}(x)$, $\text{tanh}(x)$, and $\text{dhyp}(x)$.

Table C.2: Angelov Current Source Model Parameters

Parameter	Value	Description
P1	0.51950172	Polynomial coefficient for channel current
P2	-0.09897110	Polynomial coefficient for channel current
P3	0.15309860	Polynomial coefficient for channel current
B1	1.88139390	Unsaturation coefficient for P1
B2	2.28616997	Unsaturation coefficient for P2
Vpks	-1.15318600	Gate voltage for maximum transconductance
Dvpks	0.10999550	Delta gate voltage at peak Gm
Vtr	214	Threshold voltage for breakdown
Ipk0	0.50088391	Current for maximum transconductance
Lsb0	0	Soft breakdown model parameter
Vsb2	0	Surface breakdown model parameter
λ	0.00876546	Channel length modulation parameter
α_R	0.00720404	Saturation parameter
α_S	0.63120904	Saturation parameter

Table C.3: Angelov Breakdown Diode Model Parameters

Parameter	Value	Description
Ij	100E-15	Gate fwd saturation current
Pg	10	Gate dc current parameter
Kbdgate	0	Gate breakdown parameter
Pbdg	0.5	Gate breakdown exponent
Vbdgs	0	Gate source breakdown voltage
Vbdgd	0	Gate drain breakdown voltage
Vjg	0.741756	Gate dc current parameter

Table C.4: Angelov Capacitor Model Parameters

Parameter	Value	Description
P10	4.572156	Polynomial coefficient for capacitance
P11	2.308503	Polynomial coefficient for capacitance
P20	-2.508868	Polynomial coefficient for capacitance
P21	0.543319	Polynomial coefficient for capacitance
P30	2.221333	Polynomial coefficient for capacitance
P31	-0.145244	Polynomial coefficient for capacitance
P40	2.936259	Polynomial coefficient for capacitance
P41	0.161441	Polynomial coefficient for capacitance
P111	0.059387	Polynomial coefficient for capacitance
Cgspi	0.969388 pF	Gate-source pinch-off capacitance
Cgdpi	0.039153 pF	Gate-drain pinch-off capacitance
Cgs0	0.141233 pF	Gate-source capacitance
Cgs0	0.024685 pF	Gate-drain capacitance

Table C.5: Angelov Intrinsic and Extrinsic Element Model Parameters

Parameter	Value	Description
Ri	2.936259	Gate-source resistance
Rdel	109.2847	Frequency dependent gate control and delay
Cdel	0.004128 pF	Frequency dependent gate control and delay
Rgd	0	Gate-drain resistance
Cds	0.220127 pF	Drain-source capacitance
Rc1	1872.568	R for frequency dependent output conductance
Crf	39.77664 pF	C for frequency dependent output conductance
tau	1.597 ps	Internal time delay
Lg	7.913729 pH	Gate inductance
Ld	3.745041 pH	Drain inductance
Ls	0.174891 fH	Source inductance
Rg	0.121556	Gate resistance
Rd	0.227806	Drain resistance
Rs	0.000012	Source resistance

APPENDIX D

MULTIPLE EXCITATION OF NETWORKS FOR EVEN/ODD MODE ANALYSIS

Even and odd mode S-parameters are useful for understanding combining and divider networks and how a network responds to two or more applied simultaneous signals. Even and odd mode network parameters can be computed for simple circuits that are fully defined (i.e. Wilkinson combiner) by subdividing the circuit and applying open and short circuits on the symmetry line. However, generating the even and odd mode S-parameters from arbitrary S-parameters is not straight forward especially when considering 4-way or larger combiners/dividers. To put in much more general terms, what does a network look like when certain ports are driven at a particular phase? The basic idea was first outlined in [141]. This paper will use S-parameter techniques to find network behavior when excited by multiple sources allowing one to find even/odd mode parameters of arbitrary networks. First, a simple 3-port example will be developed. Then the most general case will be explored.

D.1 ARBITRARILY DRIVEN S-PARAMETER NETWORKS

Excitation of multiple ports reduces the number of ports a network has. For example, a 3-port power combiner (with 2 ports excited simultaneously) will be reduced to a 2-port by way of equal excitation (even mode) or

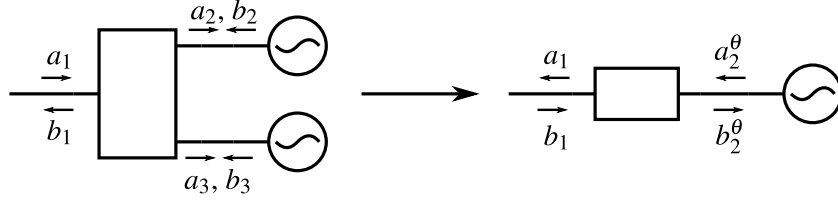


Figure D.1: Reduction of 3-port to 2-port by simultaneous excitation of two ports. The network could be a power combiner or power divider. The wave parameters a_2^θ and b_2^θ denote the simultaneous excitation of multiple ports with phase difference θ between them.

anti-phase excitation (odd mode) as shown in Fig. D.1. This follows the general definition of S-parameters

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k=0 \text{ for } k \neq j}, \quad (\text{D.1})$$

where one port is excited, a_j , and the remaining ports are terminated in the reference impedance. The voltage waves are measured at all the ports for each port excitation to generate the full S-parameter matrix; if there are 3 ports, three independent port excitation are needed to characterize the network for standard S-parameters. For multiple excitations, we will define a “port group”. Each set of ports (one or more) that are to be driven at the same time are considered a single port group. For example in Fig. D.1, the 3-port has 2 port groups: the first only has port 1; the second has ports 2 and 3. By exciting and measuring concurrently at each port group, a different type of network parameter can be defined and will be denoted in this paper as

M :

$$M_{kl} = \left. \frac{b_k^\theta}{a_l^\theta} \right|_{a_n=0 \text{ for } n \neq l}, \quad (\text{D.2})$$

where k and l now represent port groups, and the θ represents a set of driven or measured phases for each port in the port group.

D.2 SYMMETRIC THREE-PORT EXAMPLE

Consider the S-parameter matrix for a three port network:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}. \quad (\text{D.3})$$

Ports 2 and 3 will be considered as the driving ports while port 1 will be the power combined port as in Fig. D.1. For the even mode, the network is excited with two equal signals on ports 2 and 3:

$$a_2 = a_3 \equiv a_2^e \quad \text{and} \quad a_1 = 0 \quad (\text{D.4})$$

which gives,

$$\begin{aligned} b_1 &= a_2^e S_{12} + a_2^e S_{13} \\ b_2 &= a_2^e S_{22} + a_2^e S_{23} \cdot \\ b_3 &= a_2^e S_{32} + a_2^e S_{33} \end{aligned} \quad (\text{D.5})$$

If the network is symmetric ($S_{23}=S_{32}$) and both driven ports have the same input reflection coefficient ($S_{22}=S_{33}$), the second two equations in (D.5) are identical, effectively reducing the 3-port network to a 2-port. The even mode reflection coefficient, M_{22}^e , and through network parameter, M_{12}^e , are then

$$M_{22}^e = \frac{b_2}{a_2^e} = \frac{b_3}{a_2^e} = S_{22} + S_{23} = S_{32} + S_{33} \quad (\text{D.6})$$

$$M_{12}^e = \frac{b_1}{a_2^e} = S_{12} + S_{13} \quad (\text{D.7})$$

Now the combined port is excited and the remaining parameters found,

$$a_2 = a_3 = 0, \quad (\text{D.8})$$

$$b_1 = a_1 S_{11}$$

$$b_2 = a_1 S_{21} \cdot \quad (\text{D.9})$$

$$b_3 = a_1 S_{31}$$

which are merely the normal S-parameters for the port 1 reflection coefficient. However, for the through parameter, both waves from ports 2 and 3 must be considered at the combined port: the voltage waves are added. The even mode combined port reflection coefficient, M_{11}^e , and through network parameter, M_{21}^e , are then

$$M_{11}^e = \frac{b_1}{a_1} = S_{11} \quad (\text{D.10})$$

$$M_{21}^e = \frac{b_2}{a_1} = S_{21} + S_{31} \quad (\text{D.11})$$

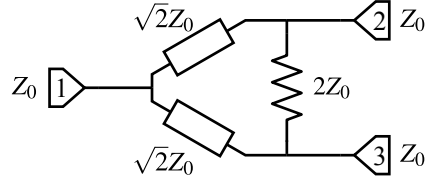


Figure D.2: Reduction of 3-port to 2-port by simultaneous excitation of two ports. The 3-port could be a power combiner or power divider.

The even mode network parameters become

$$\begin{bmatrix} M_{11}^e & M_{12}^e \\ M_{21}^e & M_{22}^e \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} + S_{13} \\ S_{21} + S_{31} & S_{22} + S_{23} \end{bmatrix} \quad (\text{D.12})$$

The careful reader will notice that the matrix is inconsistent with typical S-parameters as some of the parameters may be greater than 1. The port powers need to be re-normalized. Ports 2 and 3 were combined as one port so the power going to or from the combined port must be reduced by half:

$$\begin{bmatrix} M_{11}^e & M_{12}^e \\ M_{21}^e & M_{22}^e \end{bmatrix} = \begin{bmatrix} S_{11} & \frac{S_{12}+S_{13}}{\sqrt{2}} \\ \frac{S_{21}+S_{31}}{\sqrt{2}} & S_{22} + S_{23} \end{bmatrix} \quad (\text{D.13})$$

Similarly, the odd mode parameters can be found by changing (D.4) to $a_2 = -a_3$ and going through the same process:

$$\begin{bmatrix} M_{11}^o & M_{12}^o \\ M_{21}^o & M_{22}^o \end{bmatrix} = \begin{bmatrix} S_{11} & \frac{S_{12}-S_{13}}{\sqrt{2}} \\ \frac{S_{21}-S_{31}}{\sqrt{2}} & S_{22} - S_{23} \end{bmatrix} \quad (\text{D.14})$$

D.2.1 EXAMPLE: WILKINSON COMBINER

The S-parameters for a Wilkinson network (as shown in Fig. D.2) are well known as

$$[S] = -\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & j \\ j & 0 & 0 \\ j & 0 & 0 \end{bmatrix}. \quad (\text{D.15})$$

The even mode matrix from (D.13) becomes

$$[M^e] = \begin{bmatrix} 0 & -j \\ -j & 0 \end{bmatrix}. \quad (\text{D.16})$$

This makes sense because when the Wilkinson network is driven on ports 1 and 2, the inputs are matched, and all the power passes from the input to the combined port with a 90° phase shift and vice versa from ports 2 to 1. The odd mode from (D.14) becomes

$$[M^o] = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad (\text{D.17})$$

which also makes sense as any power driven into the network is lost. The astute reader might question that this is not a true odd mode network matrix as the combined port, M_{11}^o , is not a -1 or a virtual short. However, these network parameters are not based on subdivision of the network and applying virtual opens and shorts; the parameters are how the network behaves *in entirety*, two of the ports in the Wilkinson are driven synchronously and the last port is a traditional S-parameter. To inspect the odd mode network parameters more closely, both ports are matched (same as a Wilkinson network). M_{21}^o is zero meaning that if port 1 is driven, it there is no *odd mode* power at port 2. Similarly, M_{12}^o is zero meaning that if port 2 is driven in the *odd mode*, it there is no power at port 1.

In general, however, symmetry of the S-parameter matrix and identical input reflection coefficients are not true (ie in a planar 4-way combiner). The method here is generalized to do away with these assumptions in the next section.

D.3 NON-SYMMETRIC N-PORT NETWORKS

The basic example in the previous section can be generalized for arbitrary networks:

$$M_{ij}^\theta = \frac{1}{\sqrt{N_i N_j}} \sum_{m=g[i]} \sum_{n=g[j]} S_{mn} e^{j(\theta_n - \theta_m)}, \quad (\text{D.18})$$

where $g[i]$ is the i -th output group of port indices that are measured, $g[j]$ is the j -th input group of ports indices that are driven synchronously, θ_x is the driven (measured) phase of the individual ports in group x , and N_x are the number of ports in group $g[x]$. In words, the ij -th driven network parameter is the sum of all S-parameters in the port group $g[i]$ and $g[j]$, each port multiplied by a phasor representing the port phase, multiplied by a power normalization factor. The power is normalized by dividing by the product of

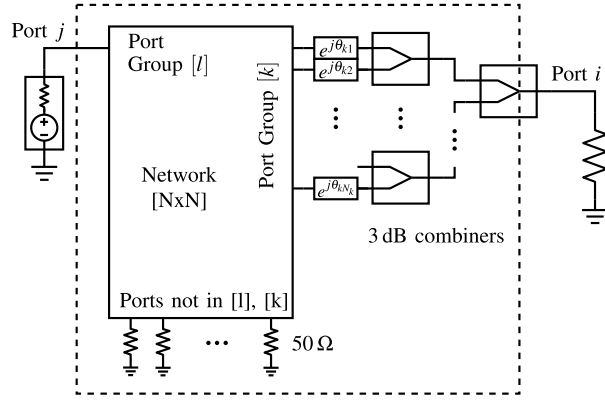


Figure D.3: Equivalent schematic for calculating M_{ij} in (D.18) where port group $[k]$ contains multiple S-parameter ports and has relative phase shifts $e^{j\theta_{ki}}$ on each port.

the number of ports in each group. The quantity g is an array of all the port groups each containing a vector of indices for that particular port group. For example, the Wilkinson in the previous section would have

$$g = [[1], [2, 3]] \quad (\text{D.19})$$

containing two port groups with the second group containing two ports.

Equation (D.18) is equivalent to the schematic in Fig. D.3. A port group, $[l]$, is driven and the resulting wave is measured at port group $[k]$. If the port group consists of multiple S-parameter ports, they are combined with ideal 3 dB combiners/dividers. The remaining ports are terminated in they system impedance (50Ω in the figure).

D.3.1 INDIVIDUAL PORT MULTI-EXCITATION PARAMETERS

The combined port parameters of a port group may not be entirely useful as there is little correlation in the physical world: it is impossible to collect and measure the combined signal at multiple ports without measuring each individual port (or some network that combines the signals at the ports) without loss of information. Combined port parameters can be used as a performance metric of a network but has little significance other than that. It is relevant to expand the previous section to find the multi-excitation parameters for *individual* ports in a port group. Instead of summing over all of the output ports as done in (D.18), only

a single output is considered. So the only S-parameters that are summed are in the excitation port group:

$$M_{ij}^{\theta} = \sum_{n=g[j]} S_{in} e^{j(\theta_n - \theta_i)}. \quad (\text{D.20})$$

There is no longer a power normalization because we are measuring waves at individual ports now and interested in the performance of the network with particular excitations. The power exiting the network, $P = |b_i|^2 - |a_i|^2$, gives information that otherwise may have been obscured if the parameters were normalized. For example, if an individual port in a port group has a greater return power than input, it means that the other ports are overcoming and driving power out through that particular port. For most cases, this would be undesirable.

To complete the Wilkinson example before, the individual reflection coefficient at port 2 and port 3 are calculated as

$$\Gamma_2^{\theta} = S_{22} + S_{23} e^{j\theta}, \quad (\text{D.21})$$

$$\Gamma_3^{\theta} = S_{32} e^{-j\theta} + S_{33} \quad (\text{D.22})$$

D.4 OTHER APPLICATIONS/EXAMPLES

There are numerous applications for such a formulation of S-parameters. First and foremost, as was used in this thesis, multi-excitation S-parameters are used as a tool for even/odd mode analysis for combiner networks in a MMIC. This method allows numerical calculation for non-symmetric networks over frequency of impedances presented to the FET devices to determine the match and for stability analysis [142]. Arbitrary excitation phases are also easy to evaluate. For example, Chireix combiner networks can be analyzed in a linear simulator instead of relying on harmonic balance [119]. Here a combiner network is used to demonstrate the versatility of the derivation in the previous section.

D.4.1 EXAMPLE: INTERSTAGE MATCHING NETWORK

The primary use of this theory in this thesis is an analysis method for non-symmetric combiners or dividers. An interstage matching network shown in Fig. D.4a is vertically symmetric. However, it is impossible to

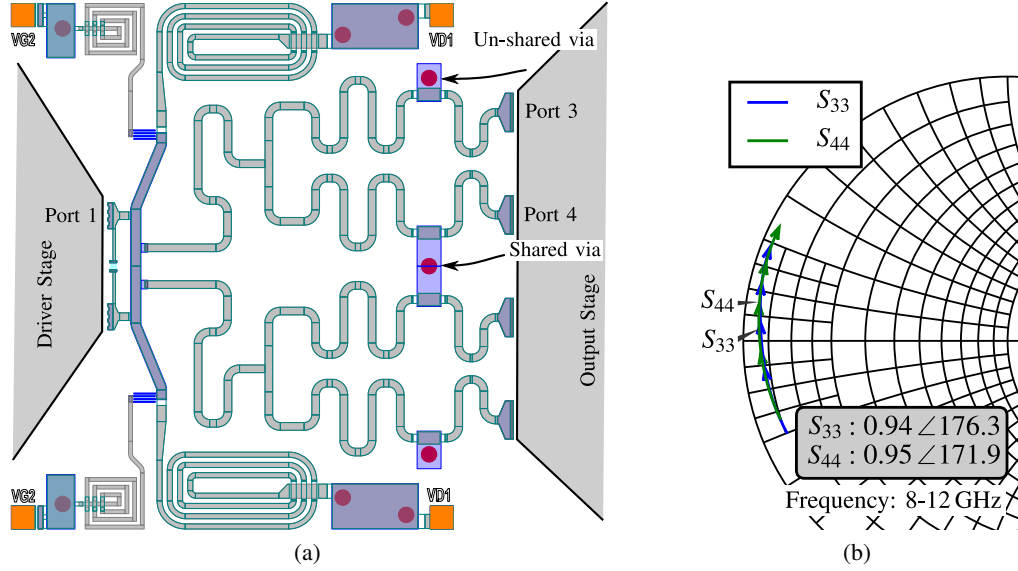


Figure D.4: (a) Interstage matching network from MPC MMIC run #2. There are two FETs in the first stage driving 4 output stage FETs. The network is a 2-input, 4-output divider. (b) Interstage matching network S-parameters of port 3 and port 4. There is a small phase difference of 4 degrees as seen by 50 Ω S-parameters.

achieve a symmetric planar 4-way divider when requiring the output ports to be horizontally aligned; the inner division will necessarily be shorter than the outside arms. Analyzing this network just by considering the S-parameters of the network is incorrect because S-parameters are defined for only one port being driven. Fig. D.4b shows the S-parameters for ports 3 and 4, the gate match on the output stage with the driver stage drain ports (ports 1,2) terminated in the expected impedance of the FET, $\Gamma_{drain} = 0.501 \angle -60.9$. There is a difference of 4 degrees between the two ports which was deemed small enough and adequate for the design at the time (the other two ports on the gate of the output stage have the same phase difference because of the vertical symmetry).

Considering the versatility of (D.20), analyzing a multi-way divider is straight forward. The phase between all the ports is ideally 0 degrees. The port groups are defined as

$$g = [[1, 2], [3, 4, 5, 6]]. \quad (D.23)$$

The individual port reflection coefficient for the match presented to the gate of the output stage FETs are

$$\Gamma_i = S_{i3} + S_{i4} + S_{i5} + S_{i6} \quad (D.24)$$

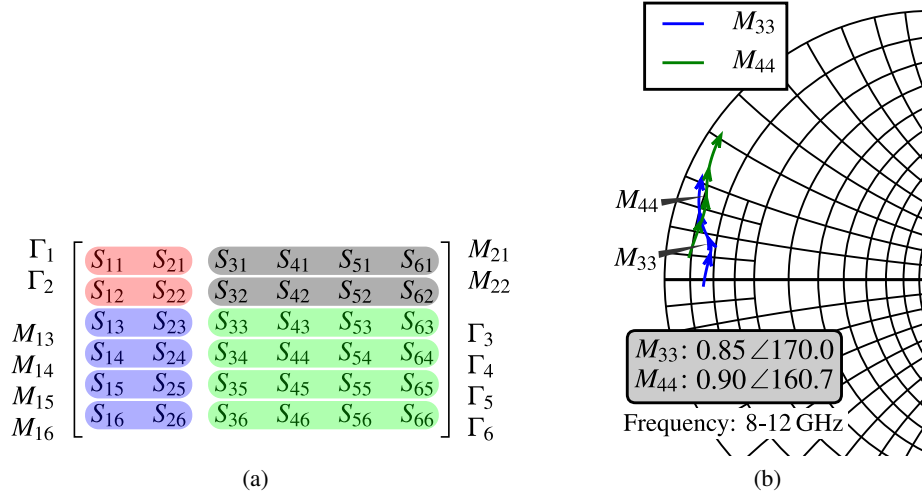


Figure D.5: (a) Method to visualize the use of (D.20) for the interstage network. The parameters in the same shaded color would have all been summed in (D.18), but here, the response of each port is kept separate. (b) Multi-excitation parameters for the same layout shown in Fig. D.4a. Compared to the S-parameters in Fig. D.4b, the shape, phase, and magnitude of the reflection coefficient is very different.

where i is the port number 3-6. Fig D.5b shows the multi-excitation reflection coefficient for port 3 and 4. The difference between Fig. D.4b and D.5b is quite large. Not only is the phase difference between the ports twice as large as the S-parameters give (now 9 degrees), the shape of the reflection coefficient over frequency is different. The multi-excitation parameters show a small resonance for both M_{33} and M_{44} at 10 GHz, but a larger one for M_{33} decreasing the magnitude to 0.85 compared to 0.95 for the S-parameter case in Fig. D.4b. This error in design is doubly pernicious because of wasted power in odd-mode resistors and the increased potential for odd-mode oscillations. Any differences in phase and amplitude are damped by the odd-mode resistors. Extra power is dissipated unnecessarily because of the difference in 10 degrees between the top two (and bottom two) adjacent FETs. Additionally, large phase differences between adjacent FETs may increase the likelihood of odd-mode oscillations which is when two FETs in a combiner are 180 degrees out-of-phase. While the phase difference is only 10 degrees at 10 GHz, higher frequencies are more likely to odd-mode oscillate as the phase difference between the FETs becomes closer to 180 degrees.

The primary cause of the phase shift is from the shared via between the two inner arms of the divider as shown in Fig. D.4a. The inductance of the capacitor-over-via (COV) for the two inner arms is double the inductance of the outer arm COVs because it has twice the RF current going through it. This was rectified

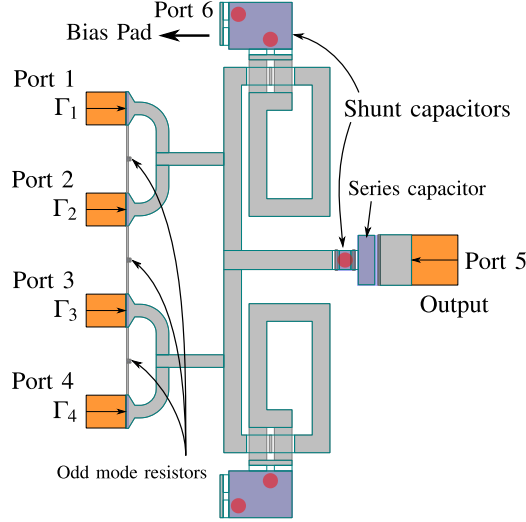


Figure D.6: Output combiner network of a MMIC. Ports 1-4 are where the FET devices are placed. Port 5 is the output bondpad of the MMIC. The orange boxes represent the de-embedding applied to the drawn geometry. Blue shading represents capacitors while the red circles are substrate vias to ground. The network was used in the MPC program and was designed by Chuck Campbell.

in subsequent designs which had unshared vias for all four arms.

D.4.2 EXAMPLE: EVEN/ODD MODE ANALYSIS

An example is presented here for even/odd mode analysis of a 4-way combiner for the output matching network of a MMIC (Fig. D.6). There are only two port groups, ports 1-4 at the drain of the FETs, and port 5 for the output of the network:

$$g = [[1, 2, 3, 4], [5]]. \quad (\text{D.25})$$

The individual port reflection coefficient for the match presented to the FETs (even mode) are

$$\Gamma_i = S_{i1} + S_{i2} + S_{i3} + S_{i4} \quad (\text{D.26})$$

where i is the port number 1-4. The odd mode reflection coefficient can be computed by flipping the sign of the S-parameters corresponding to the ports that are 180 degrees out-of-phase.

Regarding the odd mode of a combiner/divider network, little guidance is given in literature in the method of analysis and modes that might exist. This might be because the measurement of odd modes is difficult; by definition there is no power that escapes the output of the network as the symmetry line is a virtual short

Table D.1: Unique 4-way combiner modes assuming half symmetry. The ‘+’ and ‘-’ relate to the relative phase between the ports, where ‘-’ is 180 degrees out of phase from ‘+’.

Mode	1	2	3	4	5	6
Port 1	+	+	+	+	+	+
Port 2	+	+	-	-	-	-
Port 3	+	-	-	+	+	-
Port 4	+	-	+	-	+	-

circuit. Additionally, the modes that exist depend on the physical implementation of the network. For the 4-way combiner, as a simple example, Table D.1 gives all the possible half, quarter, and hybrid modes that may exist in the combiner network. Assuming the network is symmetric for the half mode, the negative modes of those listed are omitted. The first column is the even mode as all the ports are driven in-phase. The second column is the traditional concept of the odd mode: the elements on opposite sides of the symmetry line are out of phase by 180 degrees. The next two are quarter mode oscillations and the last two are hybrid which combine even and quarter modes on the opposite halves of the network. All of the modes are possible, but which is the “right” one? In the general case, all are correct and all modes must be analyzed for a holistic view of the network. However, not all modes are realistic. For example, the hybrid modes in Table D.1 are very unlikely because the network is symmetric vertically and would require a grossly mis-designed interstage network. In addition, the reflection coefficient is greater than 1 for most frequencies for the hybrid modes. This means that power is being *driven into the drain* of the FET, and it is unlikely to be a stable mode of operation. It is pertinent to remind the reader that the method presented here *assumes* that the network is driven in a particular way. In a physical implementation, the FETs will *not* be perfectly out of phase for odd modes or in-phase for the even mode.

In practice, it is cumbersome to generate reflection coefficients for all possible modes (and all phases!) for a network. It may be enough to assume a virtual short along half and quarter lines, as some literature suggests [141]. An important distinction of the derivation here from [141] is that the ports 1-4 are being excited at the same time, whereas in the paper, only 2 ports (image pairs) are excited at a time. This gives a network with ports only on one side symmetry line which can be used for further analysis; i.e. the network can be used in a loop gain stability analysis [142]. The reduced network driven in even mode gives mode

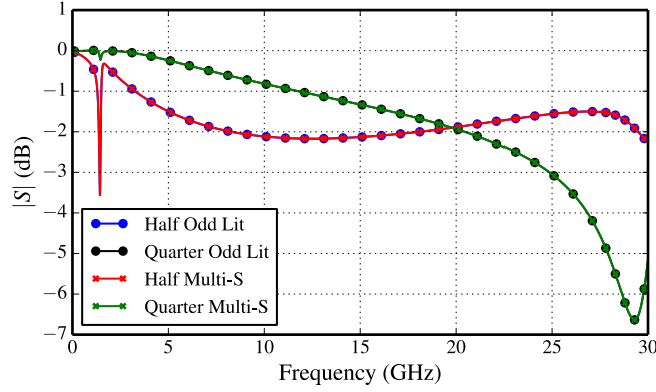


Figure D.7: Comparison of the port 1 reflection coefficient using published literature (Lit), and with multi-excitation S-parameters developed in this appendix (Multi-S).

2 in Table D.1 while driven in the odd mode gives mode 4 in Table D.1 (mode 3 cannot be generated from the method used in the paper). Fig. D.7 illustrates that generating the reflection coefficient with the method in [141] and directly via (D.20) are identical.

Assuming a reduced network (half of network assuming symmetry line is perfect short or open) is desired using the generalized theory in this appendix for loop gain analysis, the excitation vector g can be written as:

$$g = [[1, -4], [2, -3], [5], [6]] \quad (\text{D.27})$$

for an odd symmetry line. Note that this network includes the bias pad (port 6) for off-chip components and supply voltages. Running (D.27) through (D.20) gives a 4-port network that can be used in a simulator with linear (or nonlinear) models to analyze loop gain where the first two ports are the device drains, the third port is the RF output, and the last port is the bias pad port.

APPENDIX E

SELECTED CODE

This appendix contains selected code used within this thesis. All programming code is written in Python version 2.7. Installation, thorough documentation, and tutorials can be found at <https://www.python.org/>. The default installation of Python will not have the required libraries to run the listings below. A complete list of libraries is given in Table E.1. To include a library for the following listings to work, the top of the script merely needs to have

```
import libName
```

Listing E.1: Importing Python Libraries

for each library to be imported, where `libName` is replaced by a name in Table E.1. The only exception is the `numpy` library is always imported as

```
import numpy as np
```

Listing E.2: Importing Numpy Library

Version numbers are given in the table in case future versions of libraries have non-reverse-compatible code. If the “Version” column states “Python 2.7” the library is included in the default installation but still needs to be imported into the script. There are fully packaged Python installations that will also include a majority of the libraries listed below: WinPython¹ packaged installer was used for running and developing the code listed in this thesis; Python(x,y)² is another popular packaged Python installer.

¹ Located at <http://winpython.sourceforge.net/>

² Located at <http://python-xy.github.io/>

Table E.1: Python Libraries Used in Thesis

Name	Version	Link
itertools	Python 2.7	–
numpy	1.8.1	http://www.numpy.org/

The code sections that have triple quotes, `"""`, denote document strings that describe the operation of a function or class. The document string uses the markup language reStructuredText³ to allow the Python package sphinx⁴ to automatically create formatted documentation in Python integrated development environments (IDE).

Porting the code to Python 3.x should be straight forward: the major difference is changing the call of `print` to `print()`. There are other major differences between 2.7 and 3.x, however, there are no complex or high-level code cited here where other major porting changes would be necessary.

E.1 MIXING PRODUCT ORDER FOR FREQUENCY

For the describing function method described in Chapter 5,

```
def generate_mixing_orders(farr, freq, max_order=5):
    """`generate_mixing_orders(farr, freq, max_order=5)`

    Generate mixing orders from input frequency array for a particular
    frequency.

    Parameters
    -----
    farr : array
        Input frequency array.
    freq : float
        Desired mixing frequency.
    max_order : int
        Maximum allowed mixing order.
    """
    n = len(farr)
    r = [range(-max_order+1, max_order+1)]*n
    mp_all = itertools.product(*r) # generate all combinations
    l = []
    # eliminate all mixing orders > max_order
    for mp in mp_all:
        if (sum([abs(i) for i in mp]) <= max_order):
```

³ <http://docutils.sourceforge.net/rst.html>

⁴ This library is not required to run any of the code listings. The package is located at <http://sphinx-doc.org/>

```

        l.append(mp)
l = np.array(l)
w = farr*l # create mixing product frequency
o = np.sum(w,axis=1)
# pick out mixing vectors that land on desired frequency
o1 = l[np.isclose(o,freq)]

# eliminate duplicates: o == -o
mp = np.zeros((0,n))
for p in o1[:: -1]:
    if (not np.any([np.all(-p == a) for a in mp])):
        mp = np.concatenate((mp,[p]),axis=0)
return np.array(mp)[:: -1]

```

Listing E.3: Generate mixing order from vector of frequencies.

E.2 DESCRIBING FUNCTIONS FOR ANGELOV MODEL

Equations for nonlinear Angelov current source of a FET device. The constants are defined globally and the values used are listed in Appendix C.

```

def dhyp(x):
    return x/(np.sqrt(1+x*x))

def angelov_Ids(Vgs, Vds, Vbg):
    Vdg = Vds-Vgs

    P1m = P1*(1+B1/np.cosh(B2*Vds)**2)
    Vpkm = Vpks-Dvpks+Dvpks*dhyp(alphaS*Vds)-Vsb2*(Vdg-Vtr)**2-Vbg
    psi = P1m*(Vgs-Vpkm) + P2*(Vgs-Vpkm)**2 + P3*(Vgs-Vpkm)**3
    alpha = alphaR+alphaS*(1+dhyp(psi))
    ids = Ipk0*(1+dhyp(psi))*dhyp(alpha*Vds)*(1+l*Vds+Lsb0*np.exp(Vdg-Vtr))
    return ids

```

Listing E.4: Nonlinear current source of Angelov FET model.

For the numerical integration, a function is needed to construct the multi-sinusoidal input with all the correct amplitudes and phases. The total input is then fed into the Angelov current function in the above listing. The below code is specific to the Cubature⁵ python library where the function accepts a vector of inputs of length n_{pt} . The argument, ϕ_i , contains the integration parameter, or the phases of the sinusoids. The additional arguments ($*args$) contain the amplitudes and phases of the particular surface that is being integrated over and the mixing order, \vec{k} . The function arguments are required to be in this format to be used

⁵ C code for the library is at <http://ab-initio.mit.edu/wiki/index.php/Cubature>. A Python wrapper can be found at <https://github.com/saullocaastro/cubature>.

as a Cubature integration function. The return value is an equally sized vector with the real and complex parts returned separately.

```
def angelov_DF_cubature_vectorize(phi_n, npt, *args):
    """`ids = angelov_DF_cubature_vectorize(phi_n, npt, *args)`

    Function to construct the input sinusoids and return the complex current.

    Parameters
    -----
    phi_n : float
        Integration parameters.
    npt : int
        Number of points passed in ``phi_n``.
    vn_vgs : list
        Amplitudes of Vgs input sinusoids. ``[v0..vn]``
    vn_vds : list
        Amplitudes of Vds input sinusoids. ``[v0..vn]``
    vn_vbg : list
        Amplitudes of Vbg input sinusoids. ``[v0..vn]``
    order : list
        Harmonic of input sinusoids. ``[o1..on]``
    arg_link : list
        Links integration parameters across control parameters.

    Returns
    -----
    ids : array
        Real and imaginary parts of current.
    """
    vgs_vn = args[0]
    vds_vn = args[1]
    vbg_vn = args[2]
    order = args[3]
    arg_link = args[4]
    n = len(order)
    vgs_n = len(vgs_vn)
    vds_n = len(vds_vn)
    vbg_n = len(vds_vn)

    phi = np.reshape(phi_n, (npt, n))

    vgs_arg = np.array([phi[:,i] for i in arg_link[0]]).T
    vds_arg = np.array([phi[:,i] for i in arg_link[1]]).T
    vbg_arg = np.array([phi[:,i] for i in arg_link[2]]).T
    vgs_ang = vgs_vn[1:,1] + vgs_arg
    vds_ang = vds_vn[1:,1] + vds_arg
    vbg_ang = vbg_vn[1:,1] + vbg_arg

    Vgs = vgs_vn[0,0] + 0.5*np.sum([vgs_vn[i+1,0]*(np.exp(1j*vgs_ang[:,i])
    + np.exp(-1j*vgs_ang[:,i])) for i in range(0, vgs_n-1)], axis=0)
    Vds = vds_vn[0,0] + 0.5*np.sum([vds_vn[i+1,0]*(np.exp(1j*vds_ang[:,i])
    + np.exp(-1j*vds_ang[:,i])) for i in range(0, vds_n-1)], axis=0)
```

```

Vbg = vbg_vn[0,0] + 0.5*np.sum([vbg_vn[i+1,0]*(np.exp(1j*vbg_ang[:,i])
+ np.exp(-1j*vbg_ang[:,i])) for i in range(0,vbg_n-1)],axis=0)

ids = angelov_Ids(Vgs, Vds, Vbg) * np.exp(1j*np.sum(order*phi, axis=1))
rval = np.array([np.real(ids),np.imag(ids)]).T.flatten()
return rval

```

Listing E.5: Vectorized integration function for the Angelov current source.

The total mixing product result is calculated with the function below. This takes a particular set of tones and computes all the mixing products that land on the specified output frequency. So this function can compute the total nonlinear response for a single point, for example, at one input power or drain voltage.

```

def angelov_harm(vgs, vds, vbg, freq, orders=[], max_order=5):
    """mp, comp, err = angelov_harm(vgs, vds, freq, max_order=5)"""

    Compute the total response of a nonlinear element at the output frequency
    ``freq``.

    Parameters
    -----
    vgs : list
        List of harmonic input components for control voltage ``Vgs``:
        ``[ freq, mag, phase ]``. ``freq=0`` for DC bias. Phase in radians.
    vds : list
        List of harmonic input components for control voltage ``Vds``:
        ``[ freq, mag, phase ]``. ``freq=0`` for DC bias. Phase in radians.
    vbg : list
        List of harmonic input components for control voltage ``Vbg``:
        ``[ freq, mag, phase ]``. ``freq=0`` for DC bias. Phase in radians.
    freq : float
        Desired nonlinear block output frequency.
    max_order : int
        Maximum mixing order.

    Returns
    -----
    mp : array
        Mixing products ingrated to get a frequency of ``freq``.
    comp : list
        List of output products that reside at ``freq``.
    err : list
        Integration errors.
    """

    # construct amplitde and phase arrays
    c_vgs = np.array(vgs)
    c_vds = np.array(vds)
    c_vbg = np.array(vbg)
    f_vgs = c_vgs[:,0]
    f_vds = c_vds[:,0]
    f_vbg = c_vbg[:,0]
    ixfv = np.argsort(f_vgs)

```

```

ixfvd = np.argsort(f_vds)
ixfvb = np.argsort(f_vbg)

f_vgs = c_vgs[ixfv,0]
vgs_vn = c_vgs[ixfv,1:]
f_vds = c_vds[ixfvd,0]
vds_vn = c_vds[ixfvd,1:]
f_vbg = c_vbg[ixfvd,0]
vbg_vn = c_vbg[ixfvd,1:]

# find all mixing products that land on a particular frequency
fall = np.unique(list(f_vgs)+list(f_vds)+list(f_vbg))
m = np.ones(fall.shape, dtype=bool)
m[np.where(np.isclose(fall,0))] = 0
arg_link = [[np.where(np.isclose(f,fall[m]))[0][0] for f in f_vgs[1:]],
            [np.where(np.isclose(f,fall[m]))[0][0] for f in f_vds[1:]],
            [np.where(np.isclose(f,fall[m]))[0][0] for f in f_vbg[1:]]]
mp = generate_mixing_orders(fall[m], freq, max_order=max_order)
n = sum(m)
ranges = [[-np.pi, np.pi]]*n

# for each mixing product, integrate the Angelov current source for a
# particular set of input tones (defined by vgs, vds, and vbg)
comp = np.zeros((len(mp),2))
err = np.zeros((len(mp),2))
for i in range(0, len(mp)):
    order = mp[i]
    print 'Integrating ({}:d)/({}:d): {}:s'.format(i+1, len(mp), str(order))
    if (np.all(order==0)):
        intgr_period = 1/(2*np.pi)**n
    else:
        intgr_period = 2/(2*np.pi)**n

    h, err[i]= cubature.cubature(n, angelov_DF_cubature_vectorize,
                               np.array(ranges)[: ,0], np.array(ranges)[: ,1],
                               args=(vgs_vn, vds_vn, vbg_vn, order, arg_link),
                               abserr=1e-5, relerr=1e-5,
                               adaptive='p', norm=1, vectorized=True)

    comp[i] = intgr_period*h
return mp, comp, err

```

Listing E.6: Computes total harmonic response by integrating all mixing orders that land on a defined output frequency.

The above function can be used in a top level sweep over input power as demonstrated below and as used in Chapter 5. The `rfFile` function, `filterIndices`, is a custom function to take a large dataset and select a subset based on known independent parameters. In this case, the dataset is being filtered by the low frequency power injected into the drain and the RF input power (which is known and contained in `rf1`).

It returns a dictionary that contains the harmonic balance simulated complex harmonic component at the control nodes (Vgs, Vds, and Vbg). Any method that grabs the harmonic balance tone information and places it into the in_... variables will be valid.

```

freq_in = [0, 10e6, 9.99e9, 10e9, 10.01e9]
freq_out = 10e6
max_order = 3
lf_power = -10

# create arrays for input power sweep
harm_all = [] # all mixing products
err_all = [] # error for integrations
hb_ids = [] # harmonic balance simulated current result
hb_vds = [] # harmonic balance simulated drain voltage
df_ids = [] # total summed mixing products of describing function integration
rfin = [] # RF input power

for i in range(0, len(rf1)):
    print 'RF Power {:.0f}'.format(rf1[i])
    fd = rfFile.filterIndices({'rf_power': rf1[i], 'lf_power': lf_power}, d,
retDict=1)

    # gather input tones to nonlinearity (amplitude and phase)
    # use only frequencies defined by freq_in
    ixf = [np.where(np.isclose(f, fd['freq']))[0][0] for f in freq_in]
    ixfout = np.where(np.isclose(freq_out, fd['freq']))[0][0]
    in_vgs = [[fd['freq'][j], np.abs(fd['complex(Vgs)'][j]),
                np.angle(fd['complex(Vgs)'][j])] for j in ixf]
    in_vds = [[fd['freq'][j], np.abs(fd['complex(Vds)'][j]),
                np.angle(fd['complex(Vds)'][j])] for j in ixf]
    in_vbg = [[fd['freq'][j], np.abs(fd['complex(Vbg)'][j]),
                np.angle(fd['complex(Vbg)'][j])] for j in ixf]
    in_vgs[0][1] = -np.abs(in_vgs[0][1])

    # compute the total response at freq_out
    mp, harm, err = angelov_harm(in_vgs, in_vds, in_vbg, freq_out,
max_order=max_order)

    rfin.append(rf1[i])
    harm_all.append([hr+1j*hi for hr, hi in harm])
    err_all.append(err)
    df_ids.append(np.sum(harm_all[-1]))
    hb_ids.append(fd['complex(Ids)'][ixfout])
    hb_vds.append(fd['complex(Vds)'][ixfout])

```

Listing E.7: Top level script to compute a input power sweep of a nonlinear element.

The final nonlinear drain current over input power, df_ids, can be plotted versus rfin and the drain impedance calculated by hb_vds/df_ids.